Embedded pitch adapters: a high-yield interconnection solution for strip sensors

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on behalf of the ATLAS ITk Strip Sensor Collaboration

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FRAMEWORK

Interconnection in next generation HEP experiments

- Larger sensors
- Smaller electronics
- More channels in both
- Direct wire-bonding preferred
- Production time constrains
- Bonding yield and reliability is critical

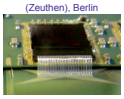
ATLAS case:
- Wafers: 6 inches to 8 inches
- ~5000-10000 channels per sensor
- 250 channels per chip
- Total: ~120 million channels (ITk)
- 3 years production
- 15 assembly sites
- ~8000 wire-bonds per site per day

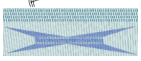
Proposal

- Second metal to implement fan-ins built in the detector
- Solution to large bonding angle without the drawbacks of external PAs
- Increase production speed and yield
- "Basic" design already implemented in the EC ITk prototype sensors

MOTIVATION

Standard and Embedded modules from DESY (Zeuthen), Berlin



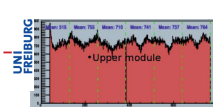


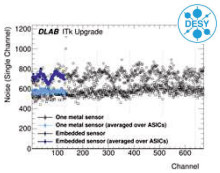
POSSIBLE DRAWBACKS

- **Cross-Talk**: signal transmitted between metal1 and metal2 tracks
- **Pick-up**: charge induced in the second metal tracks directly from the bulk
- **Noise**: due to increased inter-strip capacitance (C_{int})
- **Efficiency**: Loss in charge in the hit channel
- **Yield**: reduced sensor yield

Observed issues

- Noise
  - General increase
  - Disuniformity



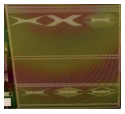


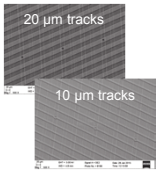
NEW EMBEDDED PITCH ADAPTERS

NEW BATCH

A batch of sensors has been fabricated:

- New designs
  - 4 New Embedded PA designs (plus "Basic" design)
- New technology improvements
  - 2 different track widths: 20 µm and 10 µm
  - 4 different inter-metal oxide thicknesses: 1, 2, 3 and 4 µm
- Full tests
  - Cint including all neighbor channels
  - Noise in module
  - Test beam
  - Irradiations





Aims:

- Reduce interstrip capacitance (Cint) ➔ noise
- "Equalize" Cint
- Keep low area fill ratio
- Reduce total coupling (with 1st metal & with bulk)
  - Signal cross-talk
  - Signal Pick-up

DESIGNS

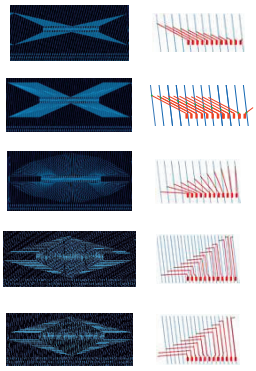
1) **BASIC** design

2) **EQUALIZE**: Current design but enlarge all tracks for same length (to equalize the noise)

3) **VARYING**: varying angle of tracks

4) **RECTANGULAR-A**: Rectangular to strips in between them (on top of p-stop)

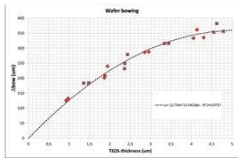
5) **RECTANGULAR-B**: Rectangular to strips on top of them

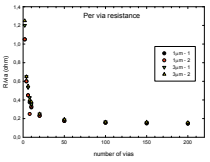


TECHNOLOGY

Wafer bowing:

- Wafers suffer stress due to the TEOS deposition ➔ limit to the the inter-metal oxide thickness





Inter-metal via:

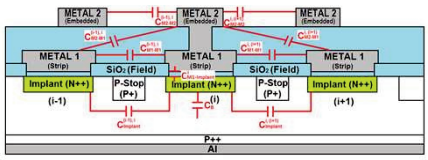
- Daisy chain test structure
- Up to 200 via contacts tested
- No fail seen ➔ **good yield**
- Average via resistance: $R_{via} = 0.151 \pm 0.005\ \Omega$

- Problem detected in via etching in center of wafer for thick oxides
- No yield problem but fabrication problem ➔ New batch

TESTS & RESULTS

INTER-STRIP CAPACITANCE

Capacitances for a double-metal strip sensor:



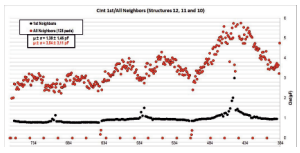
$$C^i_{int}\big|^{All}_{STD} \cong C^i_{int}\big|^{1st}_{STD} = C_B + \sum_{j-1}^{j+1} C^j_{Implant} + \sum_{j-1}^{j+1} C^j_{M1-Implant} + \sum_{j-1}^{j+1} C^j_{M1-M1}$$

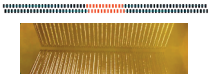
$$C^i_{int}\big|^{All}_{M2} \cong C^i_{int}\big|^{1st}_{M2} = \sum_{j-1}^{j+1} C^j_{M2-M2} \qquad C^i_{int}\big|^{1st}_{M2-M1} < C^i_{int}\big|^{All}_{M2-M1} = \sum_{j=1}^{128} C^j_{M1-M2}$$

$$C^i_{int}\big|^{All} = C^i_{int}\big|^{1st}_{STD} + C^i_{int}\big|^{1st}_{M2} + C^i_{int}\big|^{All}_{M2-M1}$$

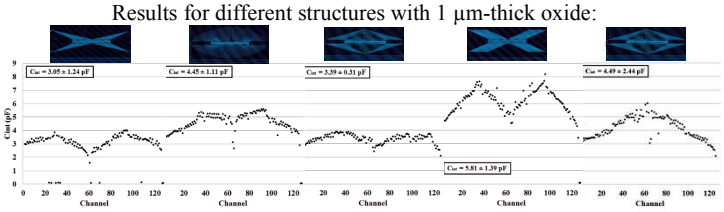
Need to evaluate interstrip capacitance (Cint) with "all-neighbours":

- 128-probes probe card to test Cint in every channel with all others grounded

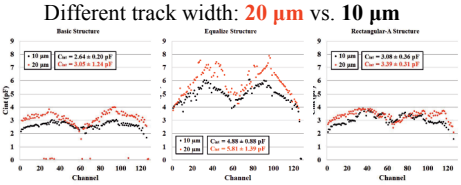




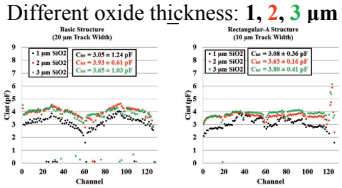
Results for different structures with 1 µm-thick oxide:



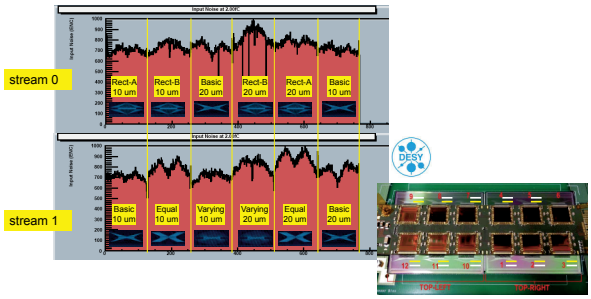
Different track width: **20 µm** vs. **10 µm**



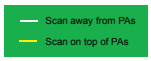
Different oxide thickness: **1**, **2**, **3 µm**



NOISE ON MODULE



DIAMOND TEST BEAM



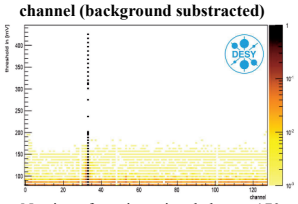
Target:

- One quarter of each structure
- Hit every other channel
- 16 strips scanned of each structure

Scans:

- Scan each row twice
  - **On** second metal layer
  - **Away** from second metal layer
- 3500 triggers per strip and per threshold
- Efficiency ~60 % ➔ ~2000 events/strip

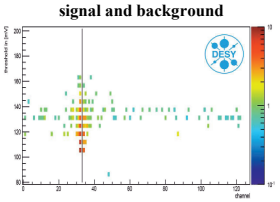
Channel signal ratio with respect to hit channel (background substracted)



No sign of spurious signal above ~170 mV threshold

- < 1% above 100 mV

Error-weighted relative difference of signal and background



No signal above threshold larger than error above ~150 mV threshold

- Charge sharing at low thresholds

CONCLUSION

- New designs and technology options are proposed to improve the Embedded Pitch Adapters
- Interstrip capacitance tests with all neighbors considered:
  - Coherent results
  - Comparison of different structures: Rectangular-A appears as best option
  - Good improvements reducing 2nd-metal track width
  - Low to no improvements with inter-metal oxide thickness (?)
- Noise results in agreement with Cint tests
- Noise problem reduced with new designs
- Test beam shows no indication of pick-up or cross-talk (pre-irrad)

Future work:

- New batch with selected designs and thick oxide thickness
- More test beams with tracking for fine efficiency tests
- Irradiations

10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Xi'an, China. 25-29 September 2015