Prototypes and system test stands for the Phase 1 upgrade of the CMS pixel detector

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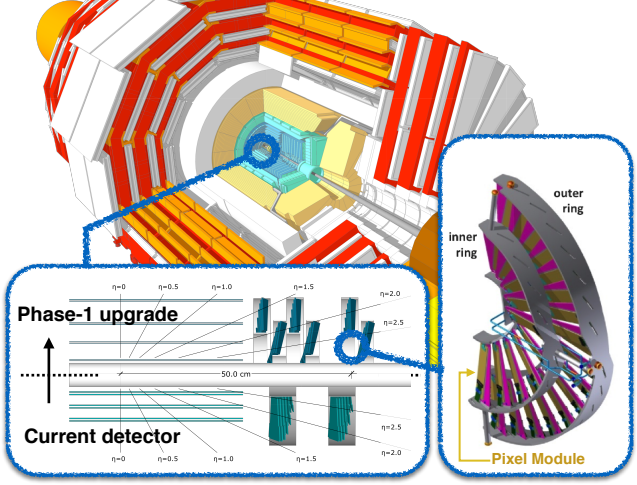


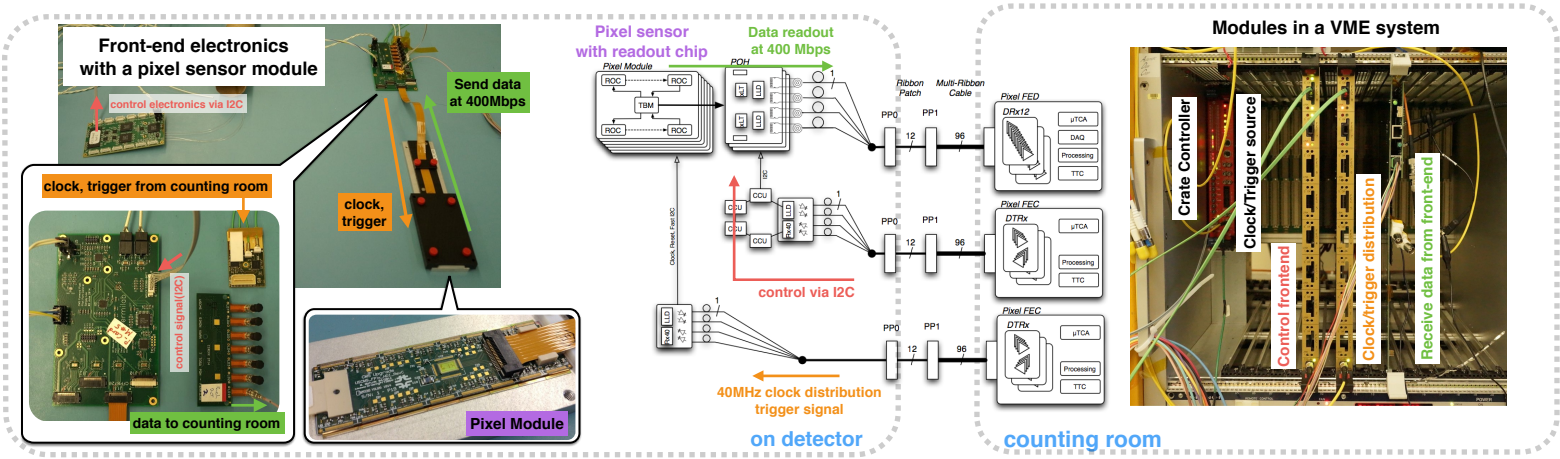
Phase-1 upgrade project of forward pixel detector (FPIX)

The CMS experiment explores the fundamental laws governing the elementary particles by studying proton-proton collisions at a center-of-mass energy of 13 TeV at the LHC at CERN in Geneva, Switzerland. The innermost part of CMS is a silicon pixel detector which allows for high precision tracking close to the interaction point. The pixel detector covers pseudo rapidities up to 2.4 and is divided in a barrel pixel detector (BPIX) and a forward pixel detector (FPIX), and detects charged particles emerging from beam collisions. As the luminosity of the colliding beams is increased to 1.5×10^{34}cm^{-2}sec^{-1} in 2017, the bandwidth of the FPIX readout reaches its limitations. The FPIX detector will be replaced by an upgraded detector with three disks of sensor modules with improved readout chips and faster readout electronics during the extended year-end technical stop of 2016/17, the so-called "FPIX phase-1 upgrade".

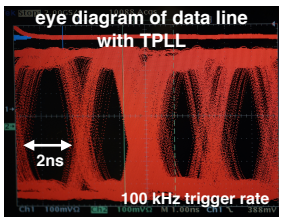
Prototypes of new electronics have been developed. Performance evaluation in an integrated system built with actual components is needed. In addition, the new FPIX detector, assembled at Fermi National Accelerator Laboratory (FNAL), needs to be fully tested and calibrated before it is shipped to CERN.

Establishment of a full readout chain equivalent to the current FPIX system

We launched a test stand at FNAL, which consists of either the same hardware as used in the current CMS pixel detector or the latest prototypes of upgrade electronics. In addition, the test stand adopts the same data acquisition system as the current detector. Therefore we can test the functionality of prototypes in a realistic environment and comprehensive evaluation is possible.

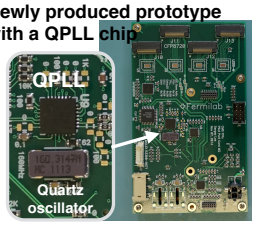


Jitter issue in the data transfer line in upgraded system and additional special PLL as the solution

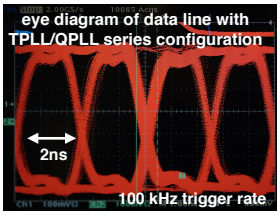


The test stand allows to evaluate the jitter of the clock distribution system. The top left oscilloscope wave form shows an eye diagram of the data signal received by the readout VME module with random trigger rate of 100kHz. The bad quality of the eye diagram is found to be caused by the clock and trigger distribution mechanism. In CMS the trigger is encoded into the clock signal (top right figure) as a deficit of one rising edge. The front-end system recovers clock and trigger from this signal using an IC chip based on a phase-locked-loop (PLL), named Tracker-PLL (TPLL). It is found that jitter arising from the PLL disturbance by missing edges (encoded trigger signals) cannot be ignored in the upgrade FPIX system where data is transferred at a rate of 400Mbps — ten times faster than in the current system.

Newly produced prototype with a QPLL chip



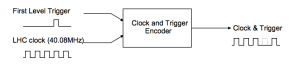
In order to mitigate the jitter, a PLL based on a voltage controlled quartz crystal oscillator (QPLL), which works as jitter filter, is inserted in the clock distribution system. The left picture shows a modified prototype electronics board with an extra QPLL chip and a quartz oscillator. The bottom left oscilloscope picture shows the eye diagram obtained using this new electronics. The right middle plot summarizes the jitter as a function of trigger rate. Two possible configurations —as shown on the right, "parallel" or "series"— are investigated, and it is found that both of them perform better than previous prototype electronics, and that the performance is stable with respect to the trigger rate. The jitter of data line with two optical receivers, namely Zarlink and Fitel (the latter is going to be used in the upgrade detector system) is also measured. The results are shown in the same figure, and we confirm that the system in total performs stably with respect to the trigger rate.



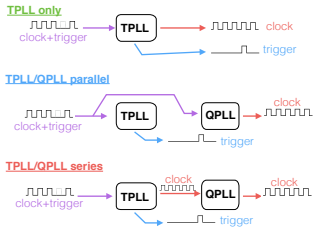
The quartz oscillator of the QPLL system is guaranteed by the manufacturer to perform down to 0 °C, while the detector is cooled to -20 °C. The board where the oscillator resides is not directly cooled but is located close to the cooling system, and will thus be at similar temperature. The functionality of the QPLLs on five cards is tested in a refrigerator. The right bottom plot shows the measured jitter as a function of temperature, relative to the jitter measured at room temperature (20 °C). This measurement confirms that the quartz oscillator works at -20 °C and even lower, and the performance is not degraded.

Given the results, a new prototype has been produced, which has a QPLL chip and fits into the detector geometry. The functionality and performance are currently being evaluated.

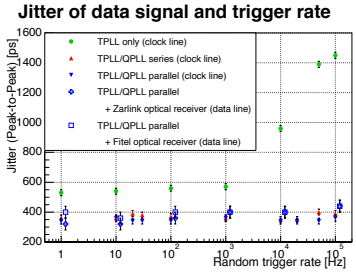
Encoding of clock and trigger signal



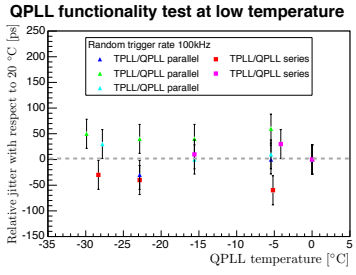
Decoding at front-end



Jitter of data signal and trigger rate



QPLL functionality test at low temperature



Toward the installation in 2017

We have established a test stand for the full pixel detector readout chain. It already allows to give valuable feedback for the produced prototypes. The development of the electronics are converging toward the production stage and installation during the extended year-end technical stop of 2016/17. In parallel to this work, we will expand this test stand system to the one used to qualify the assembled detector.