Investigation of HV/HR-CMOS technology for the ATLAS Phase-II Strip Tracker Upgrade

V. Fadeyev
SCIPP / UCSC

On behalf of Strip CMOS Collaboration:

A. Affolder[0], K.Arndt[1], R. Bates[2], A. Blue[2], D. Bortoletto[1], C. Buttar[2], P. Caragiulo[3], D. Das[4], J. Dopke[4], A. Dragone[3], F. Ehrler[5], V. Fadeyev[6], Z Galloway[6], H. Grabas[6], I. M. Gregor[7], P. Grenier[3], A. Grillo[6], L. B. A. Hommels[8], T. Huffman[1], J. John[1], K. Kanisauskas[1,2], C. Kenney[3], J. Kramberger[9], Z. Liang[6], I. Mandic[9], D. Maneuski[2], S. McMahon[1,4], M. Mikuz[9,10], D. Muenstermann[11], R. Nickerson[1], I. Peric[5], P. Phillips[1,4], R. Plackett[1], F. Rubbo[3], J. Segal[3], A. Seiden[6], I. Shipsey[1], W. Song[14], M. Stanitzki[7], D. Su[3], C. Tamma[3], R. Turchetta[4], L. Vigani[1], J. Volk[6], R. Wang[12], M. Warren[13], F. Wilson[4], S. Worm[4], Q. Xiu[14], J. Zhang[12], H. Zhu[14]

[12]Argonne National Laboratory, [8]Cambridge University, [7]Deutsches Elektronen-Synchrotron, [14]Institute of High Energy Physics, Beijing, [9]Jožef Stefan Institute, Ljubljana, Slovenia, [5]Karlsruhe Institute of Technology[1]University of Oxford, [4]Rutherford Appleton Laboratory, Didcot, United Kingdom, [3]SLAC National Accelerator Laboratory, [2]SUPA - School of Physics and Astronomy, University of Glasgow, Glasgow, United Kingdom, [11]Universite de Geneve, [6]University of California Santa Cruz, Santa Cruz Institute for Particle Physics (SCIPP), Santa Cruz, CA, United States of America, [13]University College, London, [0]University of Liverpool, [10]University of Ljubljana, Slovenia.

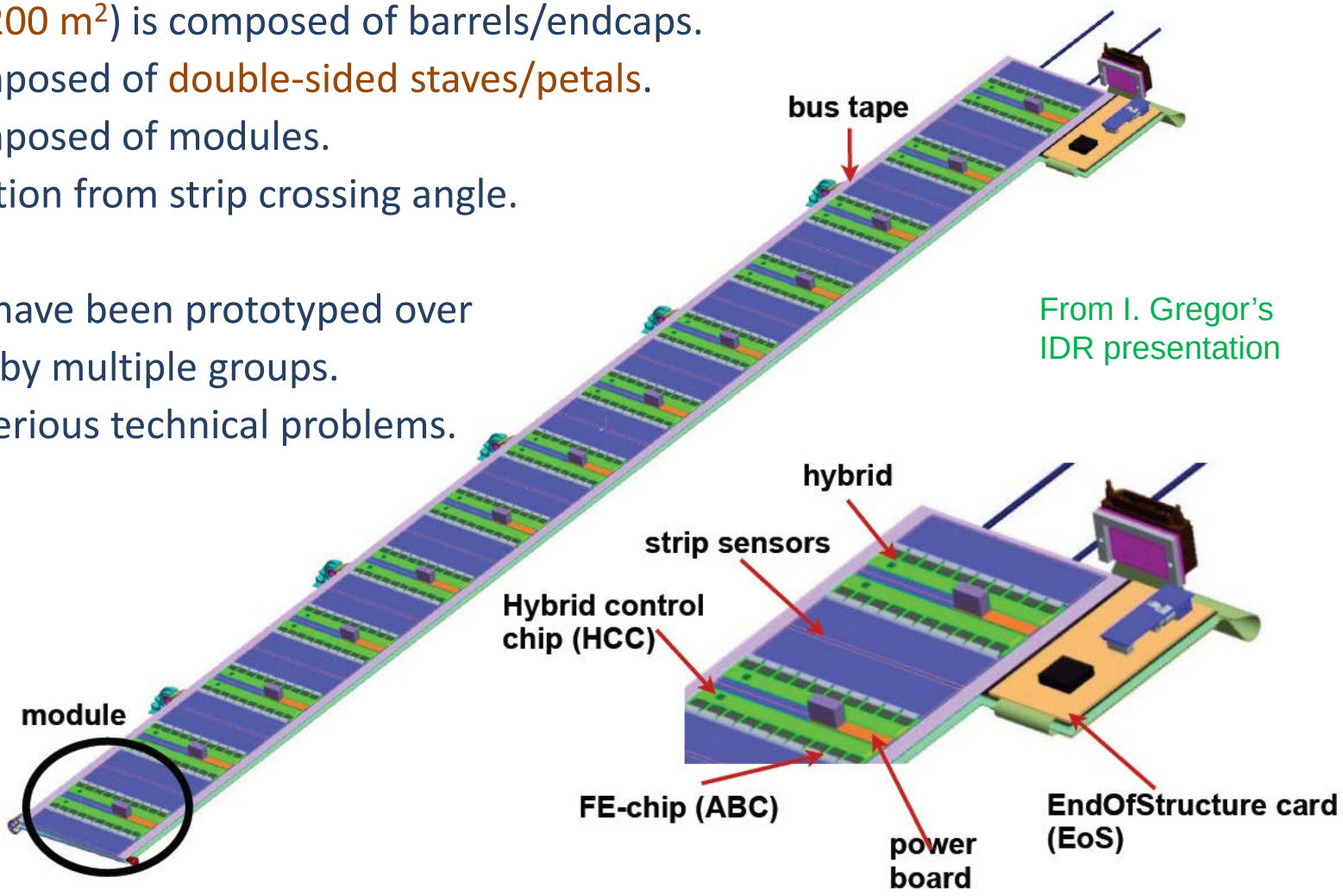
Outline

- Baseline ATLAS strips
- What is HV/HR CMOS
- Strip CMOS project
- Test Results
- Further work

Baseline ATLAS Strip Tracker

The tracker (~200 m^2) is composed of barrels/endcaps.
Which are composed of double-sided staves/petals.
Which are composed of modules.
3D hit information from strip crossing angle.

These objects have been prototyped over last >= 3 years by multiple groups.
There are no serious technical problems.



Baseline ATLAS Strip Module

A barrel module from last round of prototyping (with ABCN-250 chips).

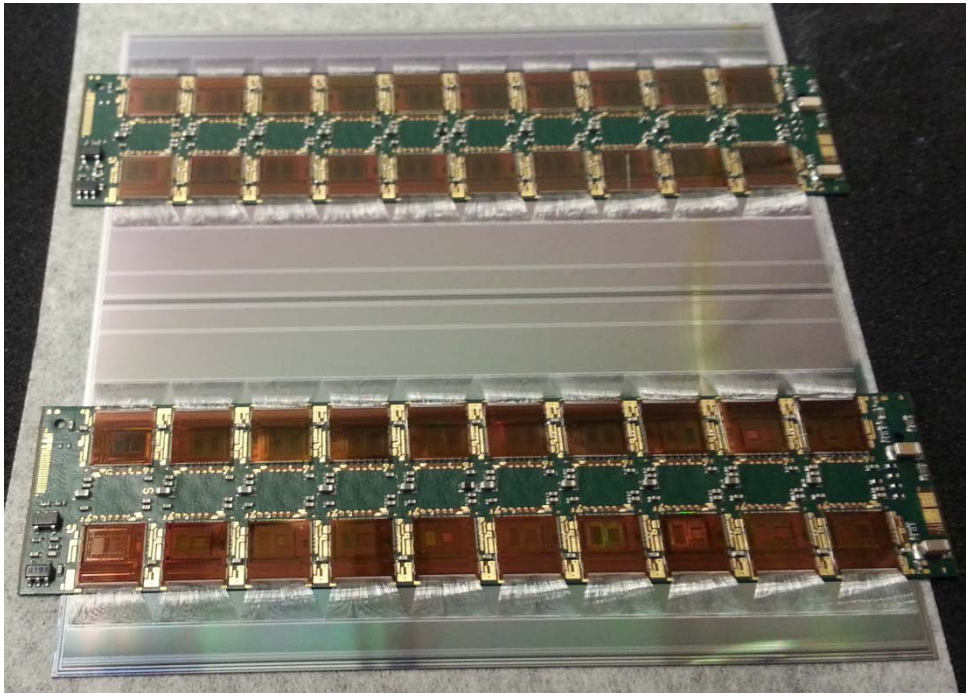
Traditional heterogeneous architecture:

- Separate sensors and readout ASICs.
- Precursor steps:
  - ASIC testing
  - Hybrid assembly and testing
  - Sensor testing.

Differences with current ATLAS SCT modules:

- n-on-p sensor as more rad-hard
- Single-sided module
- Single large sensor
- Direct gluing of hybrid on sensor
- More channels/module (and more modules in production)

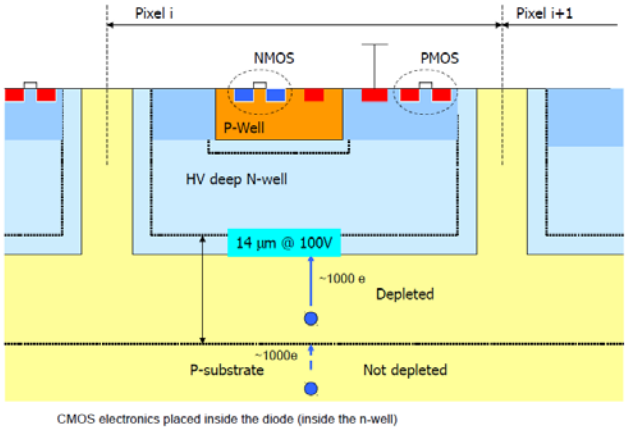
Next round of prototyping is on-going. It features new ASICs, ABC-130, with x2 channels/chip => half the chips and less hybrid area/material.



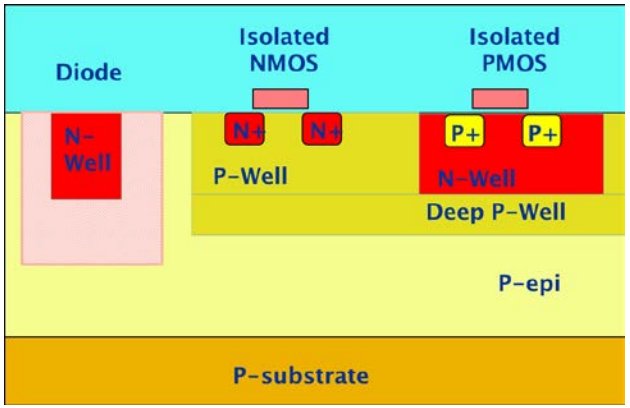
10x10 cm^2 sensor with 5120 channels; 40 ABCN-250 chips on 2 hybrids

What is HV/HR-CMOS

High-Voltage CMOS technology is a variation of standard CMOS process that is frequently used for power devices. Allows for higher-resistivity substrates and ~100 V bias.



High-Resistivity CMOS was developed for imaging applications. Features high-resistivity (1000 Ω cm) thin epi layers one can take advantage of.



Bottom line:

- *higher V(bias) and ρ than for commercial CMOS, although not as high as for what HEP is used to.*
- *Monolithic technology with analog FE and some digital circuits moved to "sensor"*

Projects within ATLAS

There are two main projects within ATLAS evaluating HV/HR CMOS technologies:

- Pixel demonstrator project {talks by B. Ristic, T. Hirono, Y. Zhang on Sat}
- Evaluation for strip sensor {this talk}

ATLAS agreed to explore the possible use of the technology for strip region, with 3-year plan:

- Year 1: Characterization of basic sensor/electronics properties and architecture
- Year 2: Fabricating and evaluating a large-scale device {we are here}
- Year 3: Full prototypes of sensors and ABCN' .

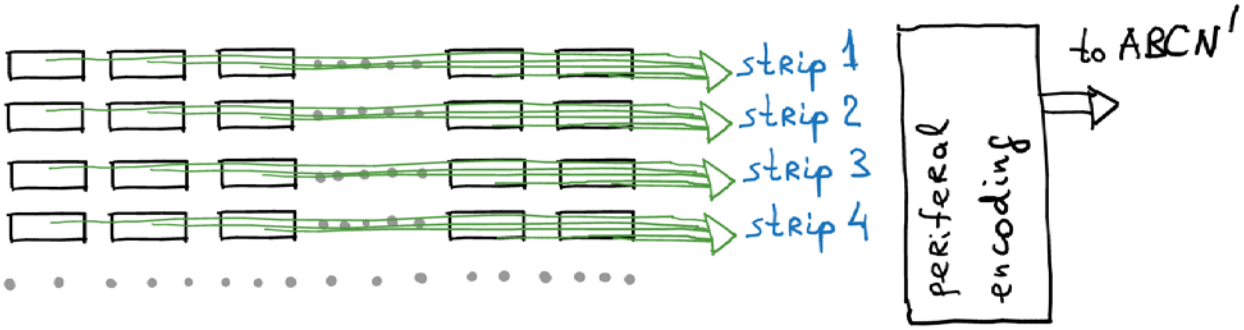
Possible improvements compared to the baseline:

- Cost savings due to x2 less area and less cost per area.
- Faster construction due to fewer wirebonds.
- Less material in the tracker.

CMOS Strips Introduction

Main motivations and parameters for what could work:

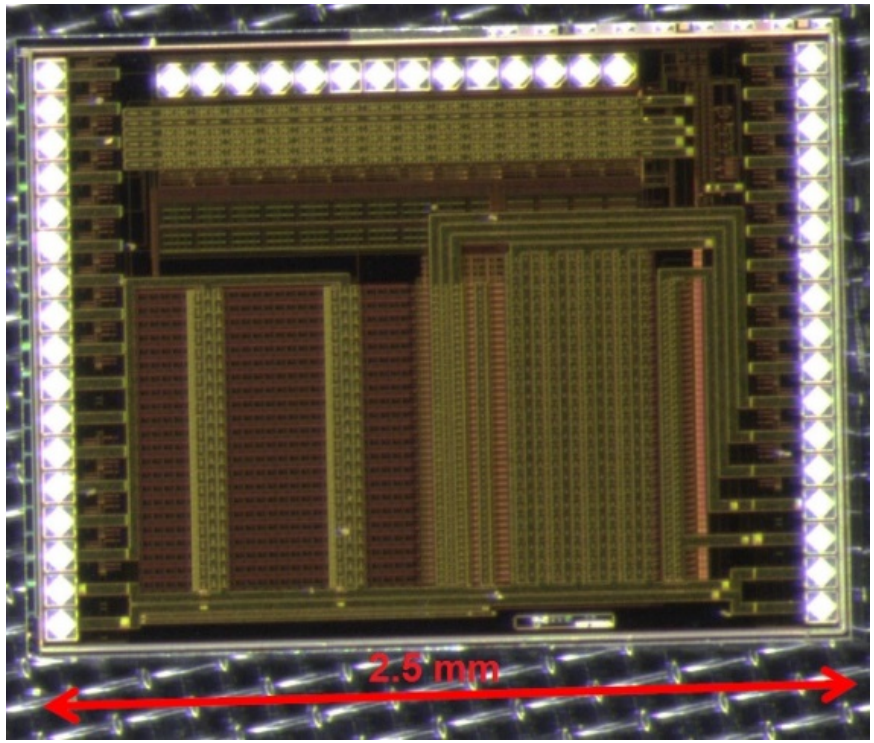
- Short time for development => match the architecture/design of the baseline program to the extend possible {staves/modules/sensors}
- Significantly smaller depletion region => "strip" is composed from pixels with individual readout {pixel detector with strip readout architecture}
- Analog FE + comparators on the sensors, with synchronous fast buses transferring data to digital chip with pipelining, and triggering.
- Single bunch crossing timing resolution.
- Similar readout chain: sensor -> ABCN' -> HCC'. But longer data packets due to longitudinal information.
- Looking at ~40 μm pitch and 720 μm length of pixels (better than 74.5 um baseline pitch and 40 mrad crossing angle).
- Max reticle sizes are ~2x2 cm^2 => Looking into rows of 4-5 chips as basic units (yield performance is critical here).
- R&D with two foundries is being pursued: AMS and TJ. (Pixel efforts have more, e.g. L-foundry.)



HVStripV1

The chip contains:

- 22x2 array of active pixels with size of 40x400 μm^2.
  - There are discriminators and a digital readout scheme.
  - There is feedback variation in amplifier feedback:
    - std linear transistors
    - Enclosed transistor
- Pixel test structures with analogue readout.
- Three MOSFET structures (NMOS-linear, NMOS-enclosed and PMOS-linear) with drain connections.



KIT

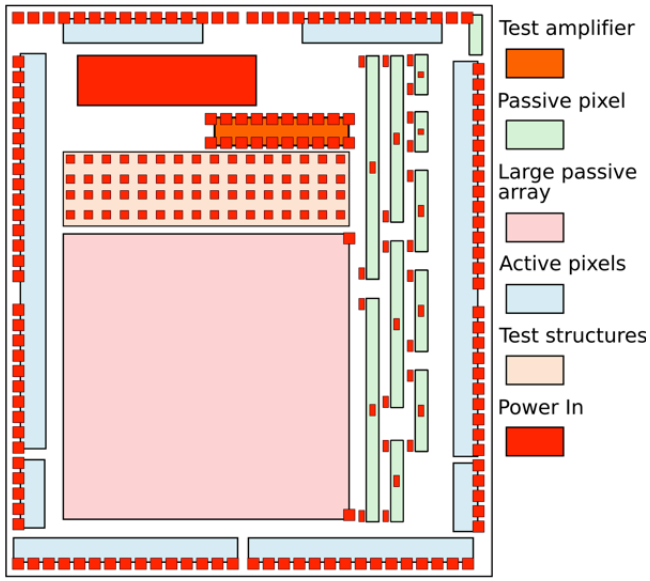
CHESS-1-AMS

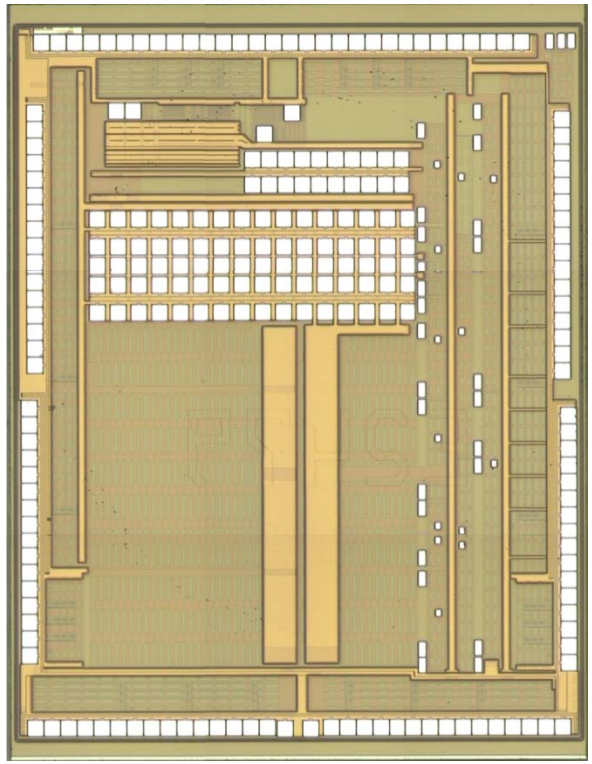
Same strategy of implementing amplifiers inside the collecting n-well was followed as for HVStripV1.

Design rules for 120 V bias were used.

The chip contains:

- Passive pixel structures
  - Length between 100 and 800 μm.
  - 30% and 50% active area fractions.
  - Mostly with guard rings; 1 structure without guard rings.
  - One structure near the ends for edge-TCT study.
  - One large array of 2 x 2 mm^2 .
- Active pixel structures.
- Isolated amplifiers.
- Transistors, Rs and C.





SLAC, UCSC

CHESS-1-TJ

TJ HR-CMOS 180 nm features a high-resistivity epi layer grown on a substrate. The collecting wells are n-type and the epi is p-type.

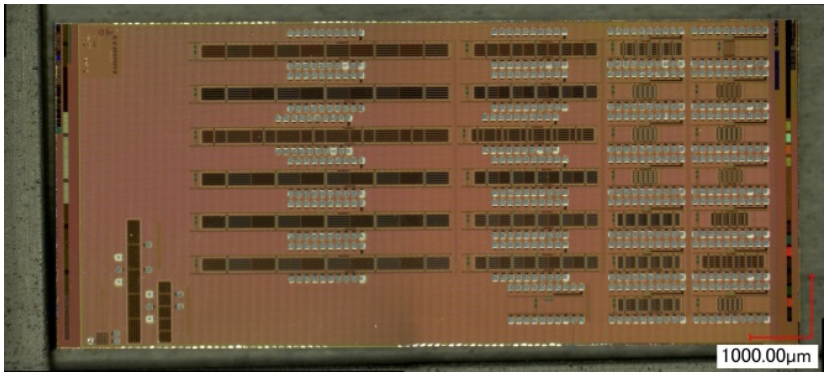
Design variations:

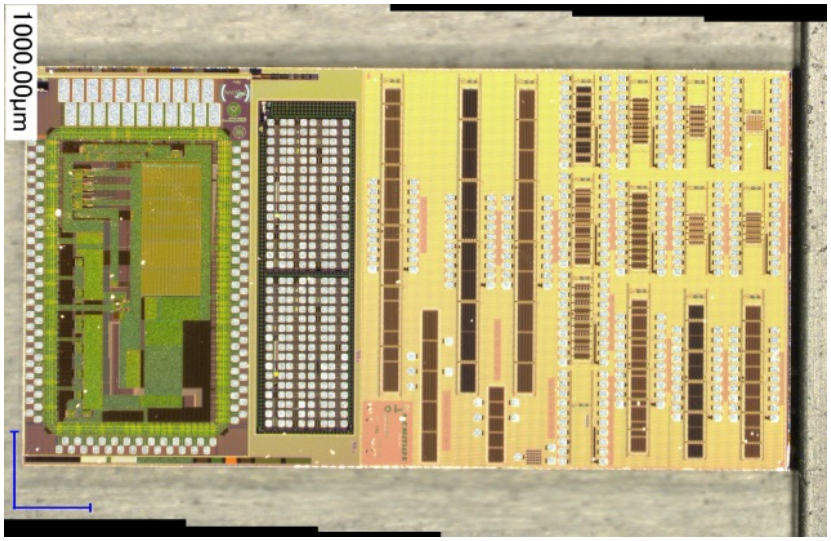
- p- and n- type substrates are being investigated.
- Epi thickness varies between 5 μm and 25 μm.
- Number and topology of the collecting n-wells.

The electronics design features the amplifier designed in the middle of the pixel area, separated from the collecting n-wells in the corners → small values of input capacitance.

The chip contains:

- Passive pixel arrays
- Active pixel arrays
- Transistor test structures





RAL

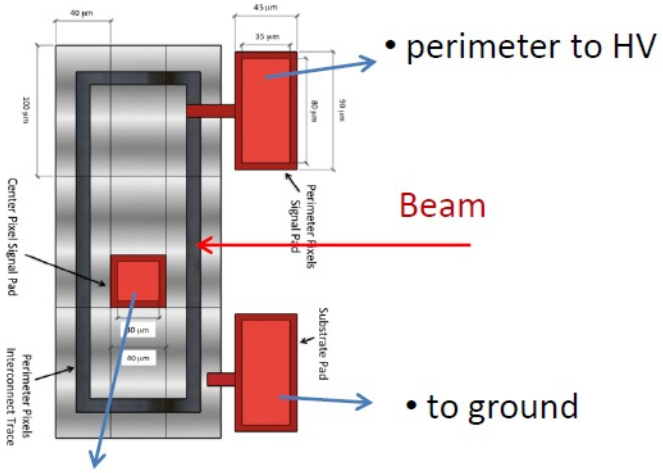
Edge-TCT Measurements

Insight into fields and depletion

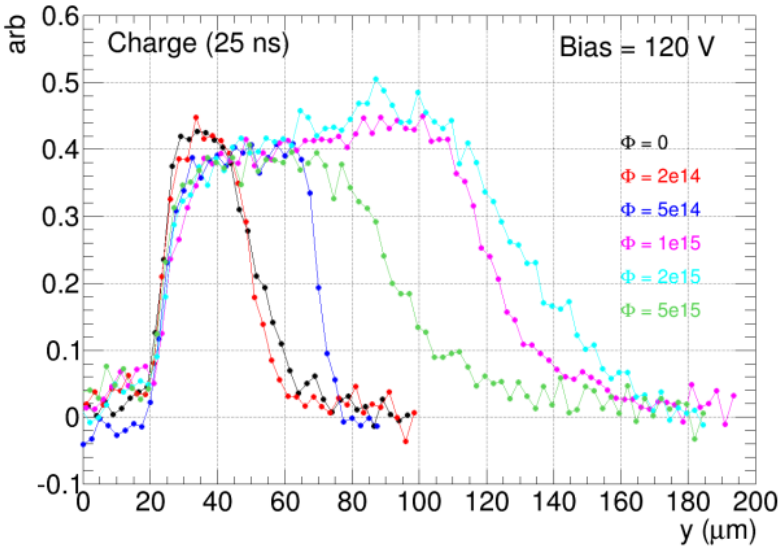
Specialized edge structure.

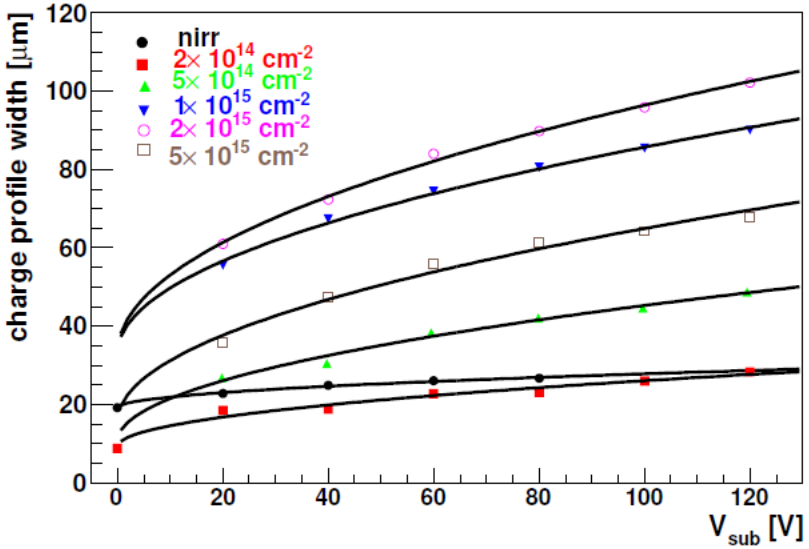
See initial growth of depletion with fluence

(for CHESS-1-AMS chip with default ρ = 20 Ω cm).



• signal to high voltage and readout (via Bias-T)





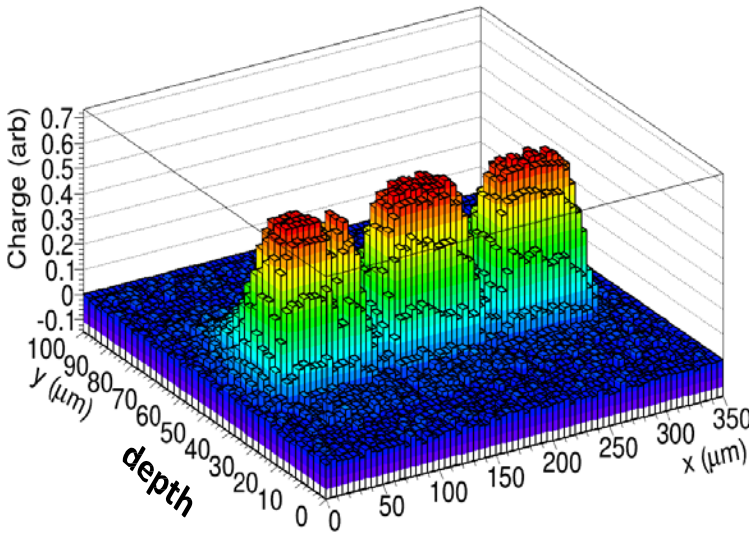
Edge-TCT, Cont

Edge-TCT scan of depth and pixel length:

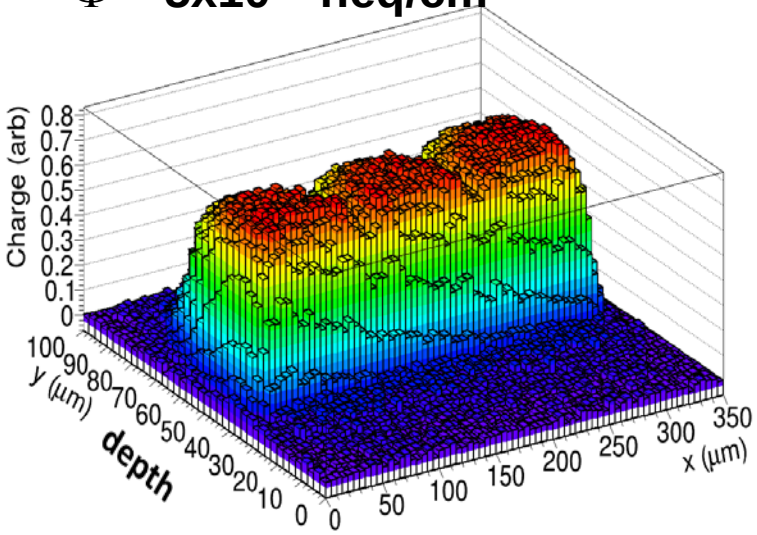
- Initial gaps of acceptance/signal between the pixel n-wells
- Disappear with fluence, consistent with higher depletion

(Should not be a problem for initial resistivity significantly higher than the default 20 Ω cm)

Φ = **0 neq/cm^2**



Φ = **5x10^{14} neq/cm^2**

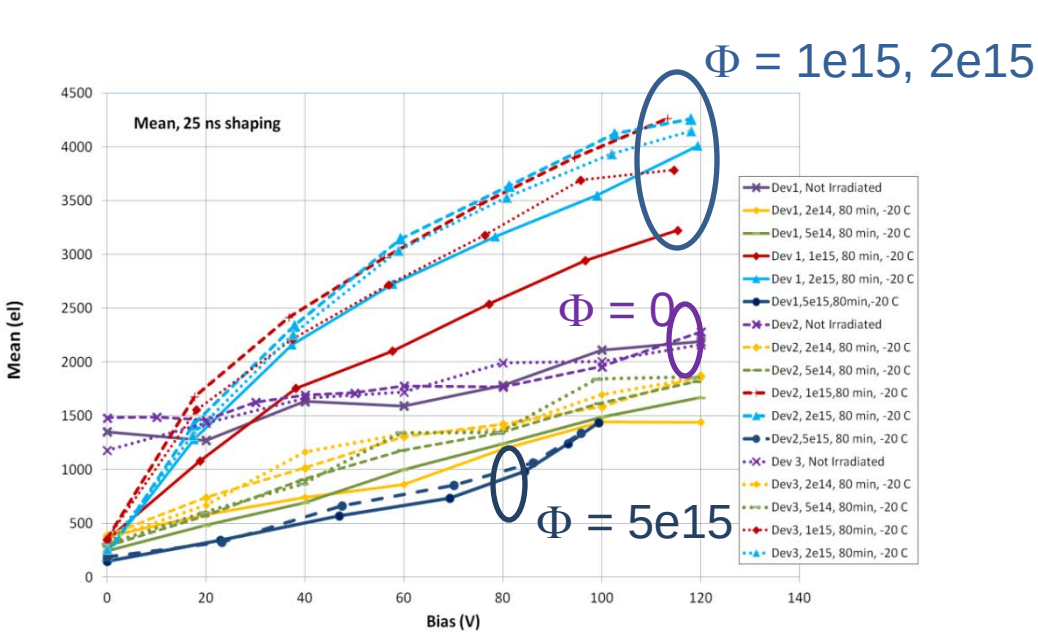


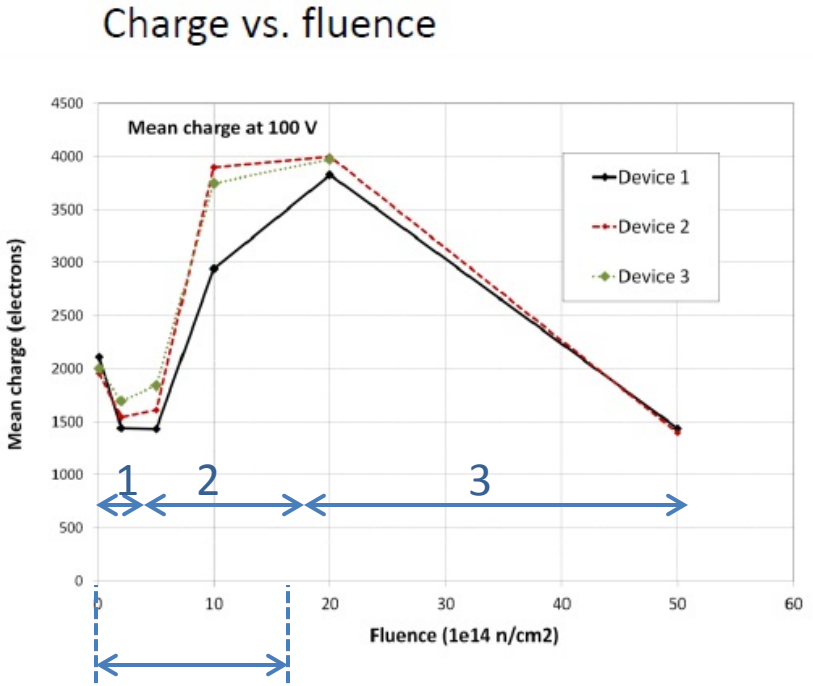
Ljubljana

Charge Collection

CCE studies on a large passive array as a function of neutron fluence:

1. Initial drop of signal due to reduction of diffusion contribution
2. Increase of signal due to larger depletion depth (acceptor removal)
3. Decrease of signal due to trapping.





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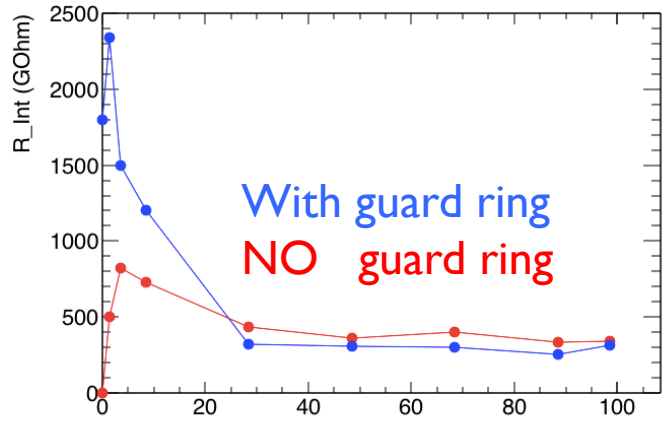
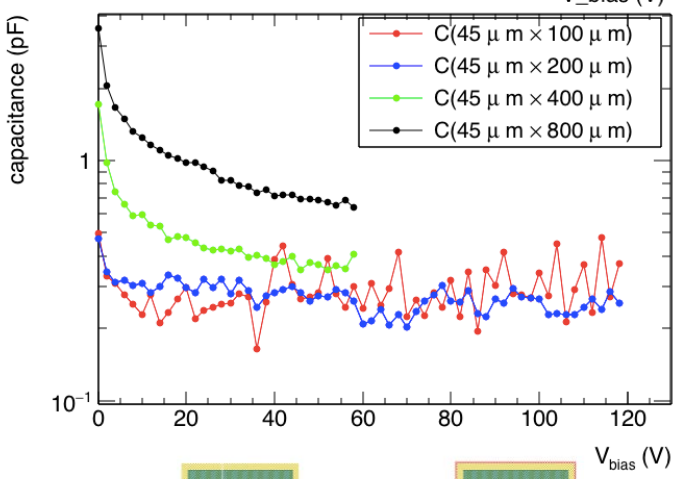
Expected range for strip tracker

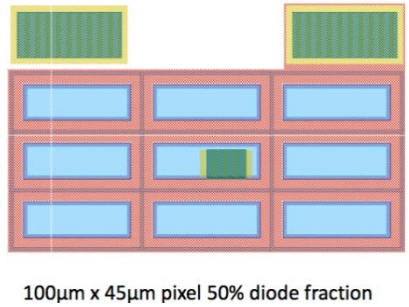
Passive Pixel Properties

We've measured several properties of passive pixels:

- Capacitances
- Inter-pixel isolation:
  - very high, even without guard rings
- Breakdown voltages:
  - Typically stay above 120 V design rule
  - Doesn't grow with fluence
  - Early breakdown for 30% active area fraction for gamma-irradiated devices







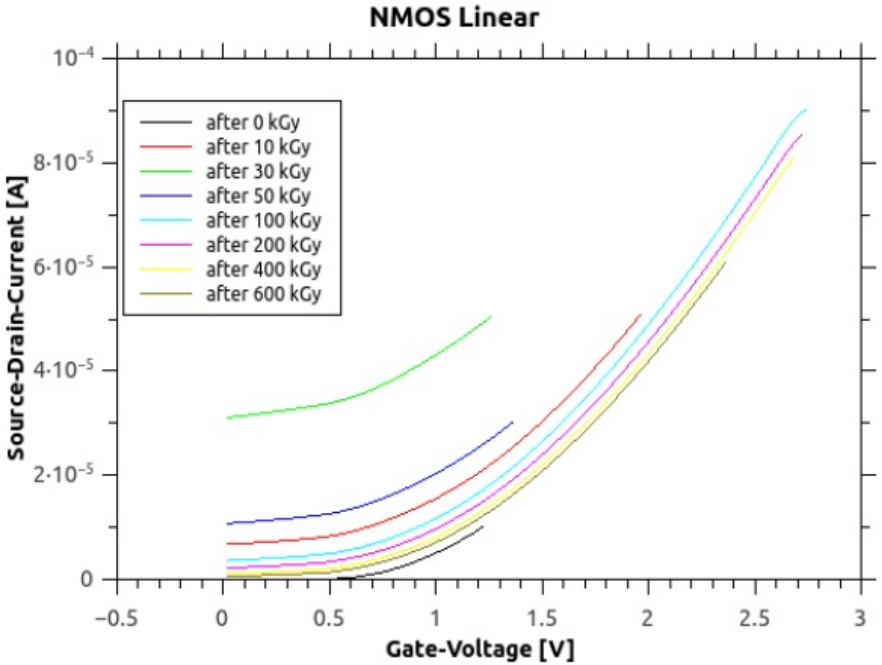
Cell capacitance simulations		
length (um)	60V	120V
100	6.29E-14	5.63E-14
200	1.17E-13	1.05E-13
400	2.27E-13	2.02E-13
800	4.45E-13	3.97E-13

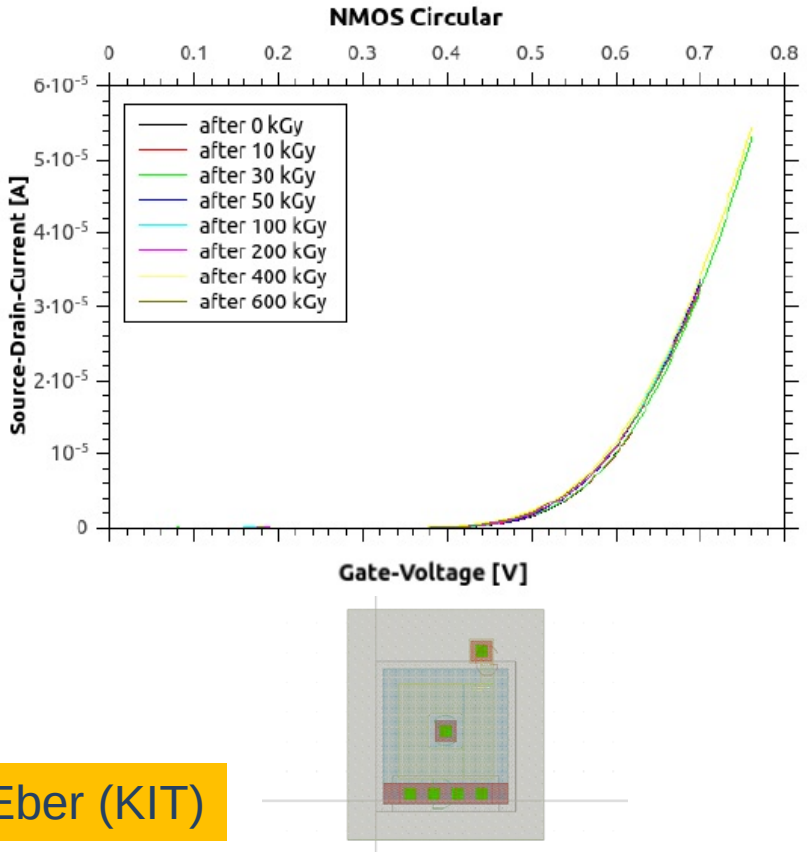
Cell capacitance measurements		
length (um)	60V	120V
100	1E-13	0.7E-13
200	2E-13	1.7E-13
400	2.5E-13	
800	4.5E-13	

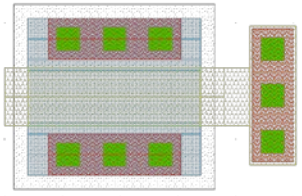
Transistors

Transistors have been looked as a function of ionizing dose (with gammas). As expected, the enclosed transistors are much more immune to radiation.

Transistor performance/simulation comparison looks good pre-rad(backup)





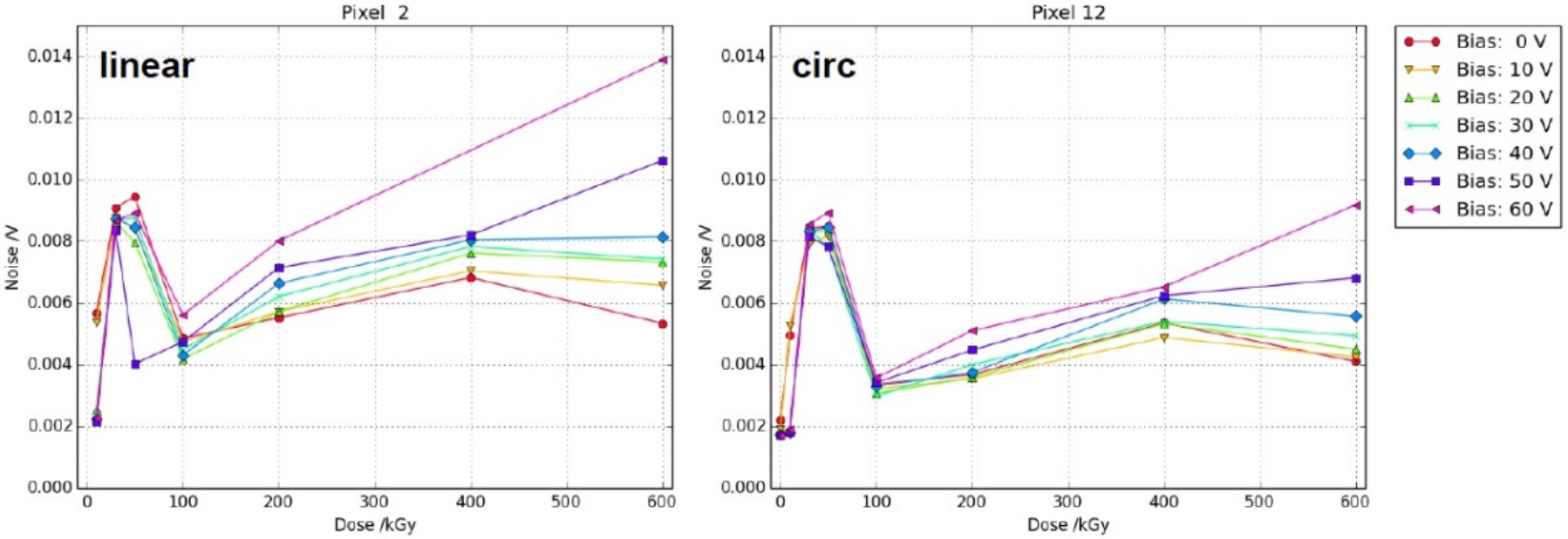


R. Eber (KIT)

Amplifier Noise

Amplifier noise was studied as a function of TID.

There is a peak at ~5 Mrad, that deserves further attention.



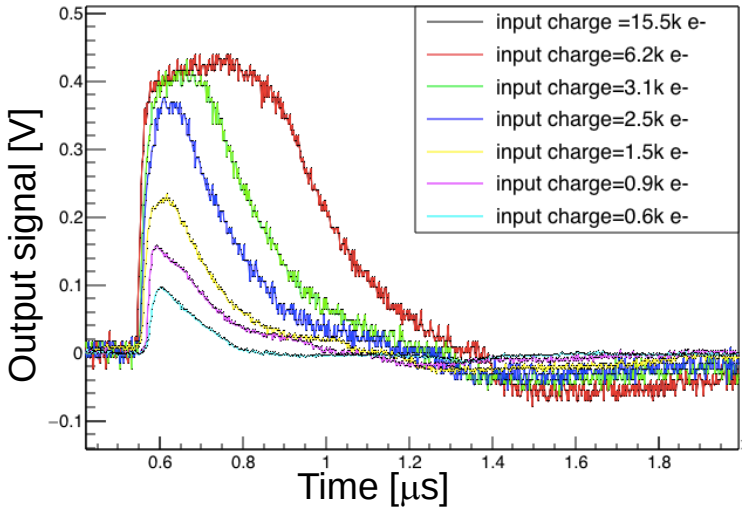
R. Eber (KIT)

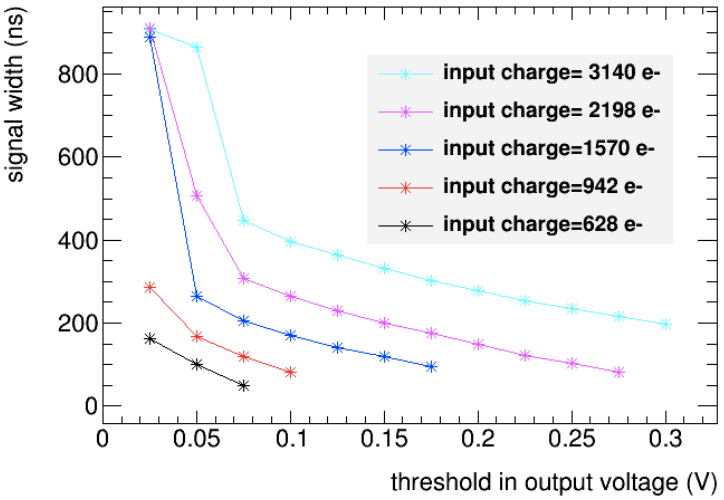
Amplifier Timing Properties

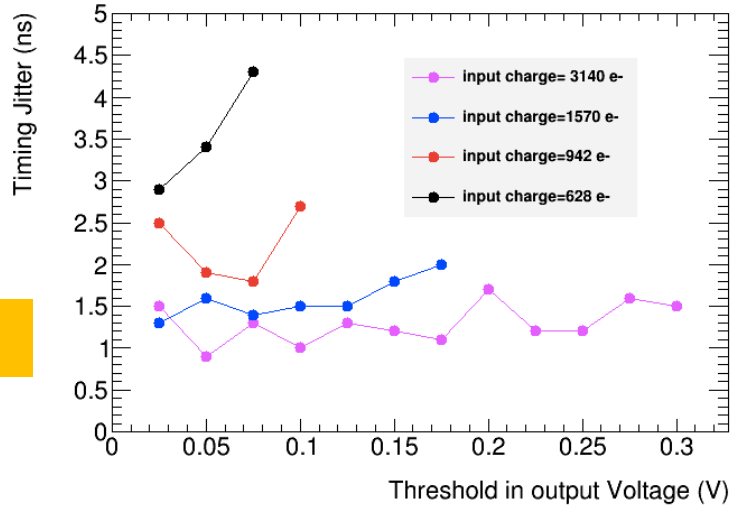
We looked at amplifier timing properties:

rise time, jitter, pulse width:

- Rise time < 25 ns
- For signal >= 1500 e- the jitter is < 2 ns (sigma)
- Signal width depends on the signal and threshold. Expected to be up to few 100 ns.







SCIPP

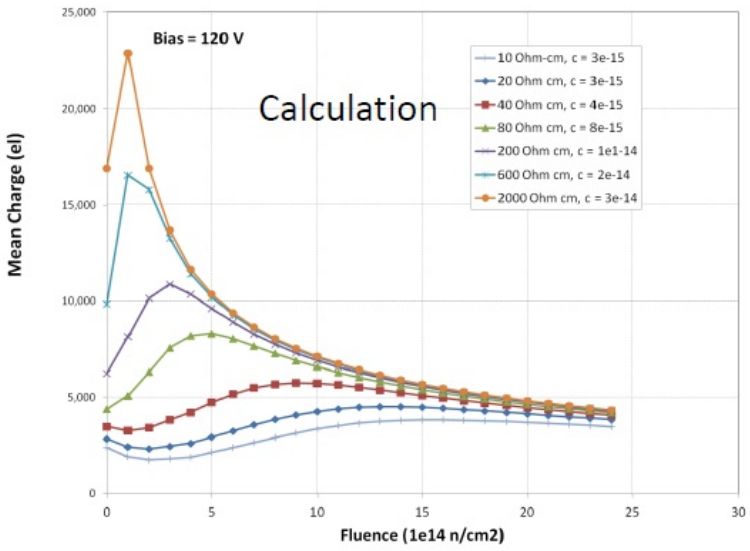
→ Amplifier performance is described in more details in Zhijun Liang's poster "*Study of built-in amplifier performance on HV-CMOS sensor for ATLAS Phase-II strip tracker upgrade*"

Optimal Resistivity

In HV-CMOS, we have worked with 20 Ωcm resistivity so far. This is very far from the standard (well studied) > 3000 Ωcm values.

Our projections indicate optimal region between 80 and 600 Ωcm based on charge collection estimates and field properties with top-level biasing.

Of course, this needs to be studied, which is one of the goals for CHESS-2-AMS.



ρ [Ω*cm]	Depletion [mm]
10	11
20	15
40	22
80	31
200	49
600	85
2000	154

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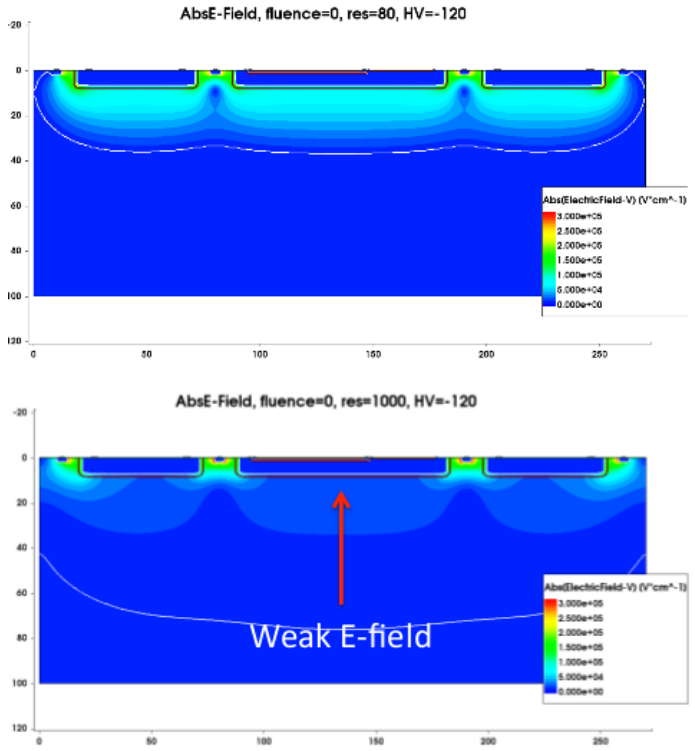


Liverpool/U.Geneva

S/N

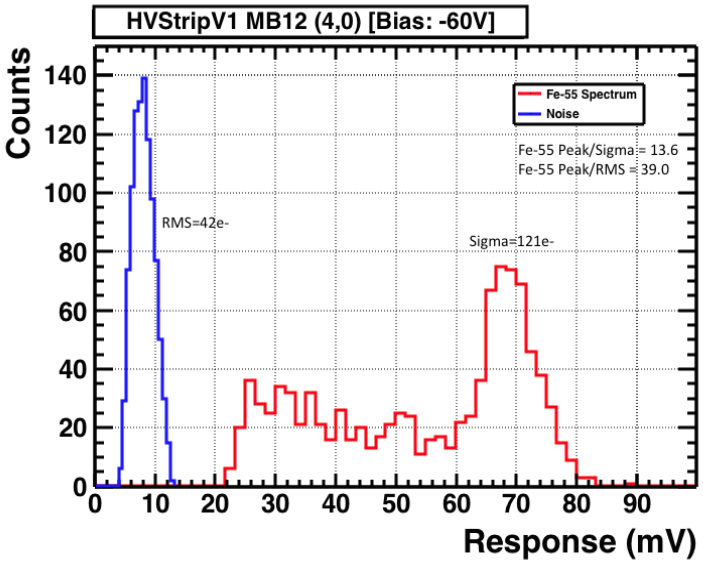
The most direct inference in the S/N was obtained with Fe-55 measurements on HVStripV1. The 1600 e- signal is similar to th minimum of 1500 e- we expect for 20 Ω cm material.

We see indications of S/N of 13 for noise of ~100 e-.

There are expectations of:

- Amplifier noise growth by x3 with dose.
- Signal grown by x3 with higher initial resistivity.

=> S/N of 13 may be a realistic factor unless we see common-mode noise.



Oxford/Glasgow

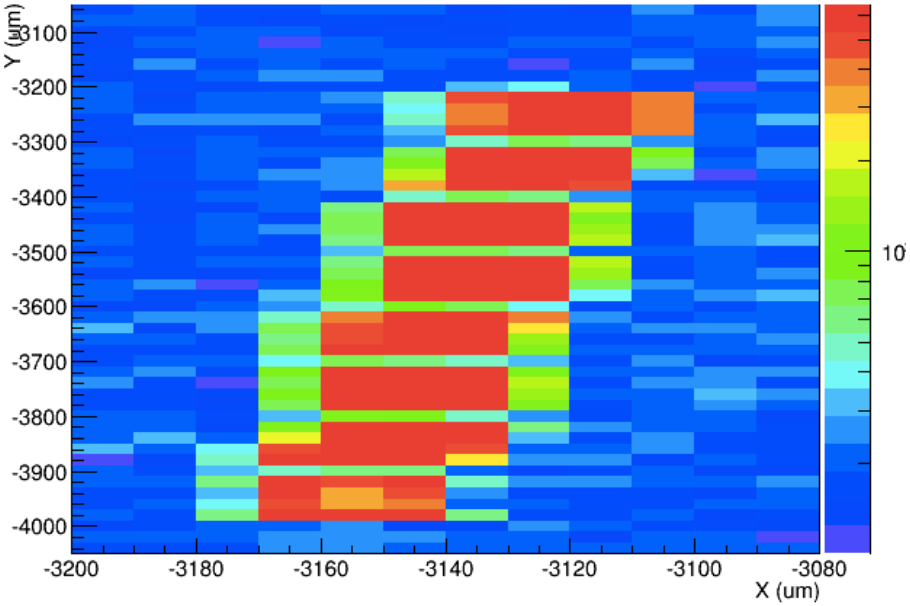
Further active pixels study

There are further on-going studies of active pixel response and properties. Of particular interest is a better evaluation of S/N with MIP level signals.

CHESS1: Top-side laser scan of 1 pixel composed of 8 n-wells.

→ Clearly see individual n-wells (there is a metal in-between).

→ Last well has less signal due to metal in the amplifier circuit.

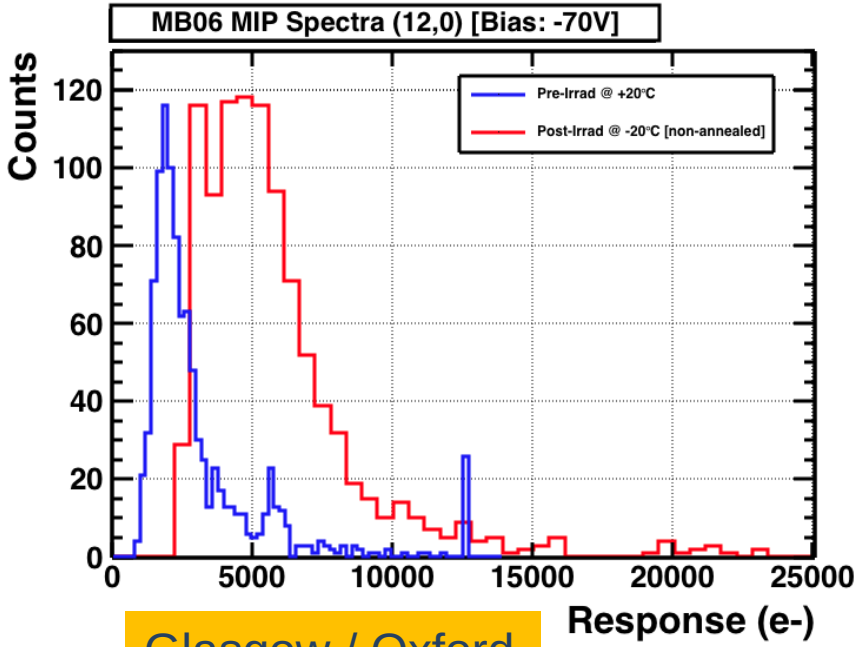


SCIPP

HVStripV1: Pre-rad and post-rad (1.23e15 neq/cm^2) MIP spectra for enclosed transistor design.

→ There is a clear signal, although with higher threshold after irradiation.

→ Higher post-rad signal, consistent with other studies.

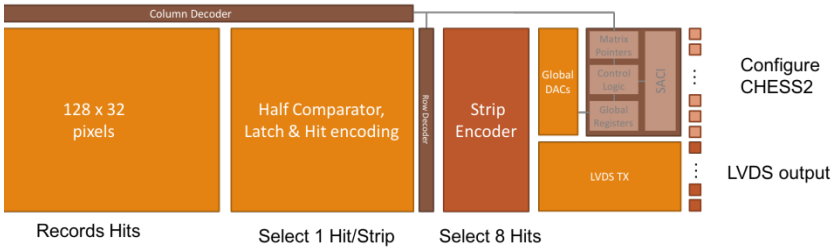


Glasgow / Oxford

Large-scale chips

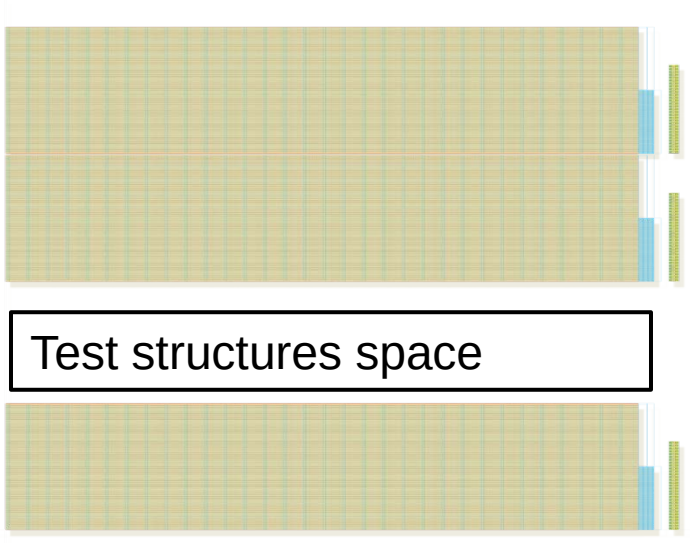
Current design efforts aim to fabricate large-area (full reticle) chips:

- Readout architecture capable of processing large number of channels with single-bunch timing resolution.
- High-speed I/O bus streaming hit information in a synchronous way from a large pixel area. Small number of I/O channels to help with the wire bonding as the limiting factor on the construction speed.
- To test for possible correlated noise effects.
- To investigate higher substrate resistivities (HV) and epi thicknesses (HR) as a boost for S/N.



Will include 3 arrays of 127 strips (strip = 32 pixels), and multiple test structures:

- Passive pixels
- Edge-TCT structure
- Large passive array
- Transitors
- LVDS transciever
- HV switch



The designs are well progressed. Had 2 design reviews (AMS version).

AMS: SLAC, UCSC, KIT
TJ: RAL

Conclusions

HV/HR-CMOS technologies are a very attractive form of monolithic sensors.

ATLAS commenced R&D efforts to evaluate them for tracking.

1st year of investigation yielded promising results and better understanding of essential technology features:

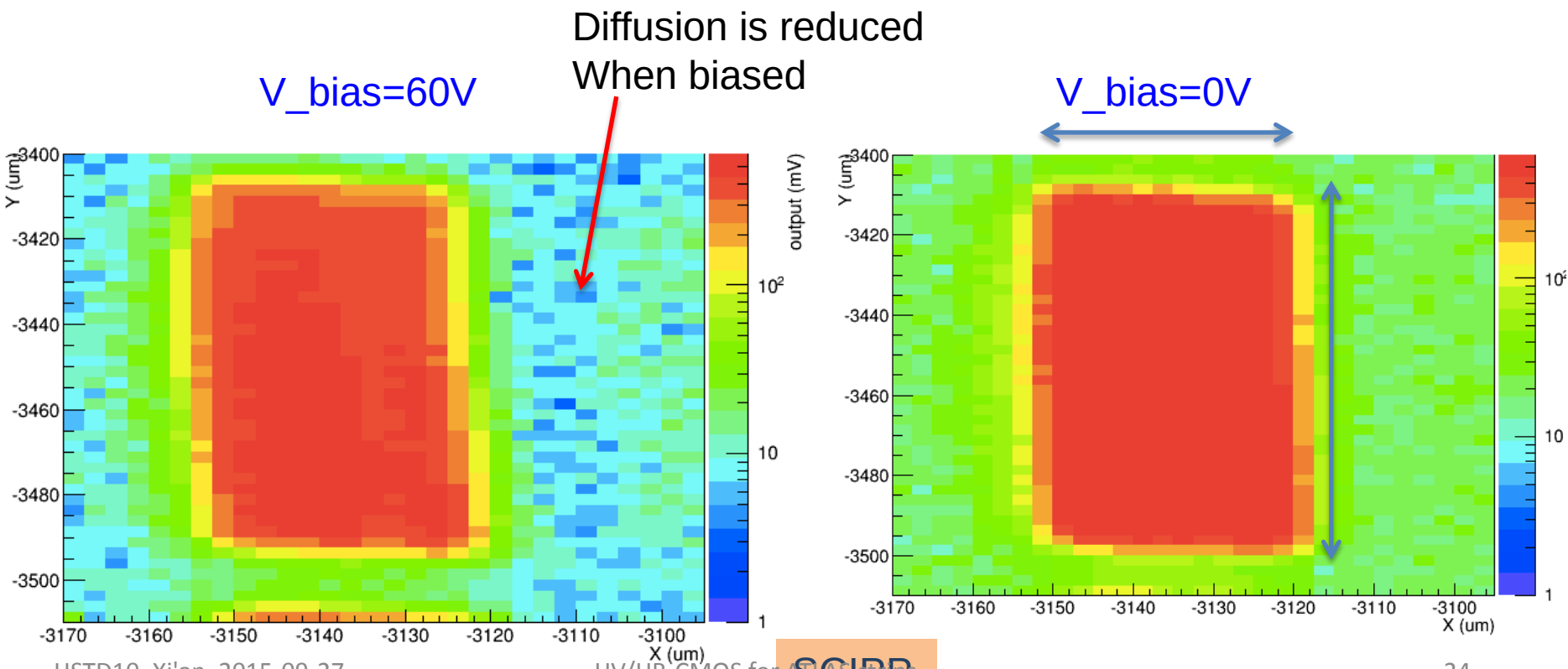
- Depletion and CCE for default resistivity
- Passive pixel properties
- Transistor and amplifier radiation resistance
- Timing properties
- Assessment of active pixel performance

Major goals for the 2nd year are design, fabrication and testing of large-area devices. The chip designs are well underway.

Backup

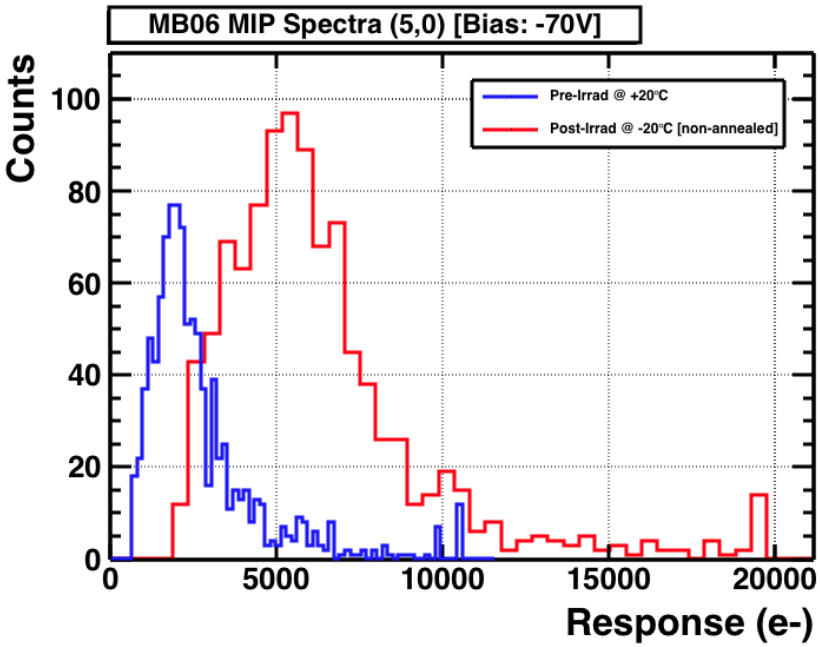
Zoom in one N-well

- Very good uniformity inside N-well

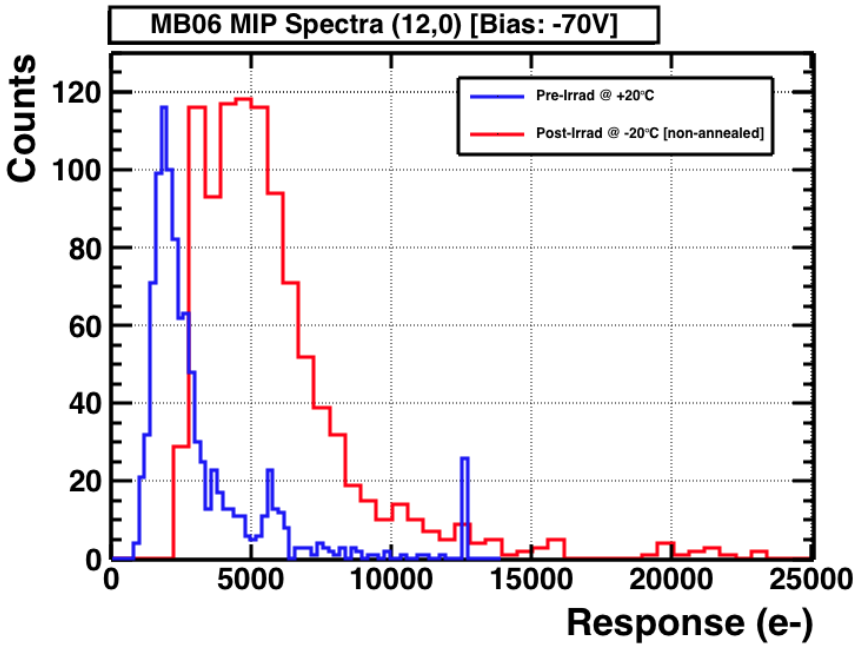


MIPS

Linear Trans. Pixel



Enclosed Trans. Pixel



- ➔ MIPS signal clearly observed after irradiation
  - Noise increase requires higher scope trigger threshold
- MIP spectra were obtained at several bias voltages before annealing
- The position of the peak after irradiation for linear pixel is higher
  - Consistent **with seeing improved signal performance**

The Properties of a CMOS Strip outer tracker

Parameter	Planar Sensor	StripCMOS Sensor
r-ϕ resolution	20 μm – 23 μm	11 μm
z-resolution	850 μm	280 μm
Two hit resolution in r-ϕ	160 μm-240 μm	80 μm
z-element length	2.5 cm	720 μm (2.4 cm / strip)
Fraction of two hit clusters	15% - 20%	2%-3%
Geometry inefficiency on stave	~0.7%	~1%
Radiation Lengths per stave	1.8%	1%
Insensitive crossings after a hit	1 BC	0.3 BC (1/32 of strip is dead for 10 bunch crossings)
Number of Signal Wire bonds	O(5100)	O(1100)

Planar values are mostly measured or engineering values

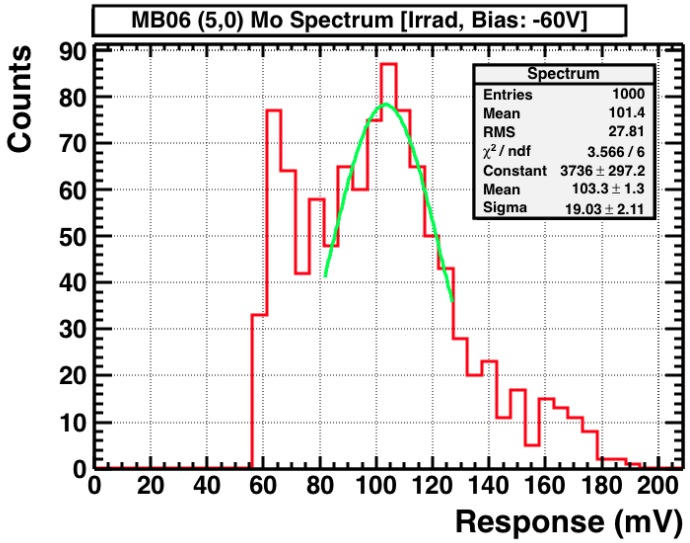
StripCMOS values are estimates – part of the R&D programme

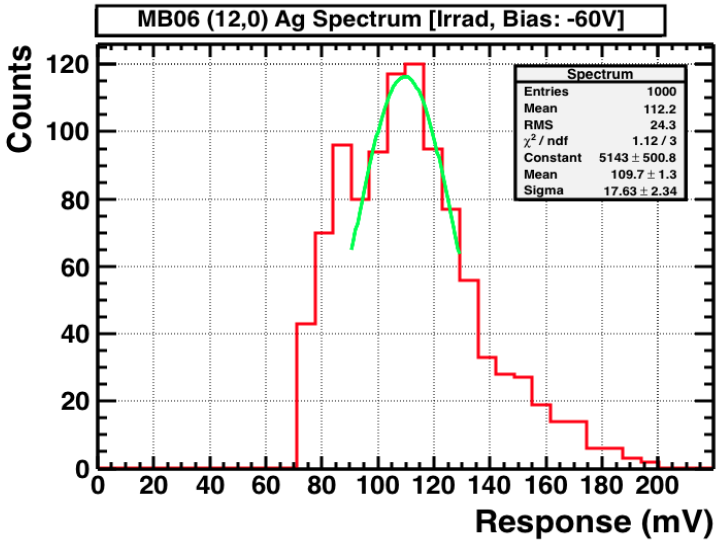
These strip sensors are pixel-like in resolution at 40x720μm.

CHESS2 Specifications

	Specs	Comments
Substrate resistivity	20 Ω cm to 1000 Ω cm	Minimal MIP From 1500-4000e-
Substrate high voltage bias	120V	40% more charge vs 60V
Pixel size	40µm x ~800µm	400fF det. capacitance
Number of pixel per strip	32	
Number of strips	128	Factor ~2 improvement in r-ϕ resol.
Timing resolution	25ns	
Maximum number of hits per strip	1 + flag	Flag = more pixels hit
Maximum number of hits per 128 strips	8	
Readout speed	320MHz	
Additional constraint	Rad-hard design	Periphery: inactive area - shorter strips

X-Ray Measurements (3)





- Mo and Ag spectra were acquired for (5,0) and (12,0) respectively at -60V bias
- Mo $K_\alpha \approx 17.5$ keV and Ag $K_\alpha \approx 22$keV lines correspond to $\approx 4860e^-$ and $\approx 6100e^-$
- The Gaussian fit was done in order to extract gain values (mV/fC) for (5,0)

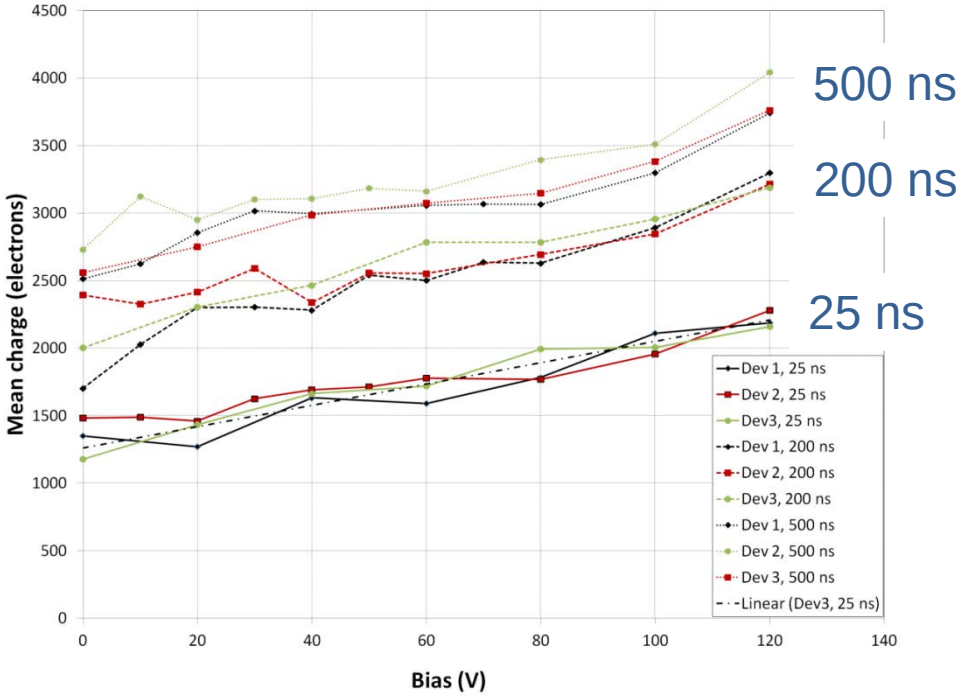
Oxford/Glasgow

Charge Collection, Pre-rad

Consistent pre-rad measurements on two different AMS-350 chips.

Significant signal at V(bias) = 0 V indicates the presence of signal from diffusion, even at 25 ns shaping time.

Shaping:

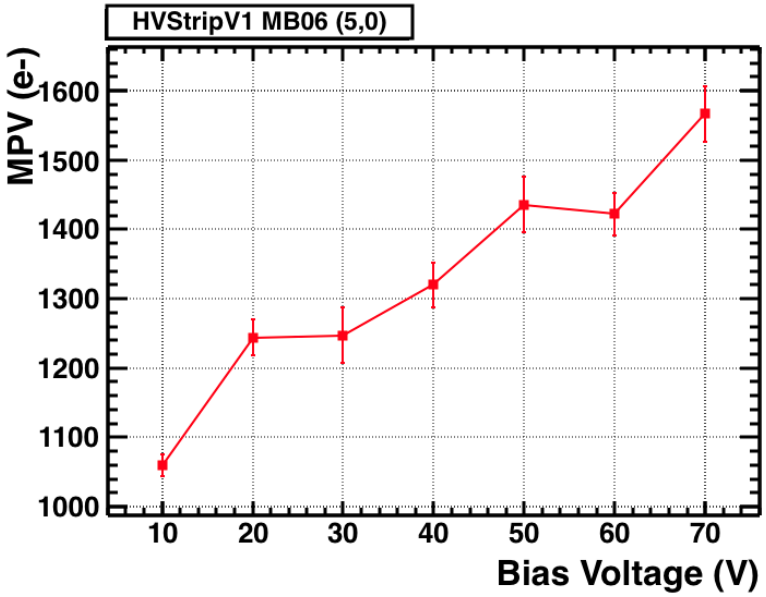


500 ns

200 ns

25 ns

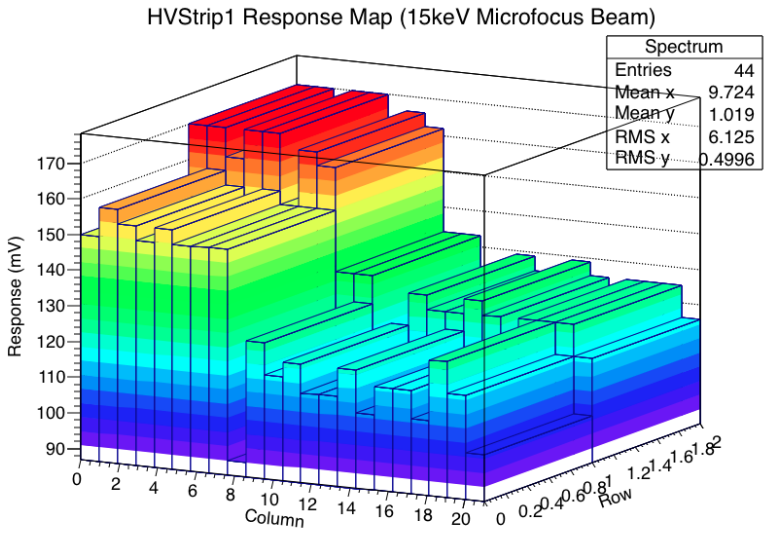
Ljubljana



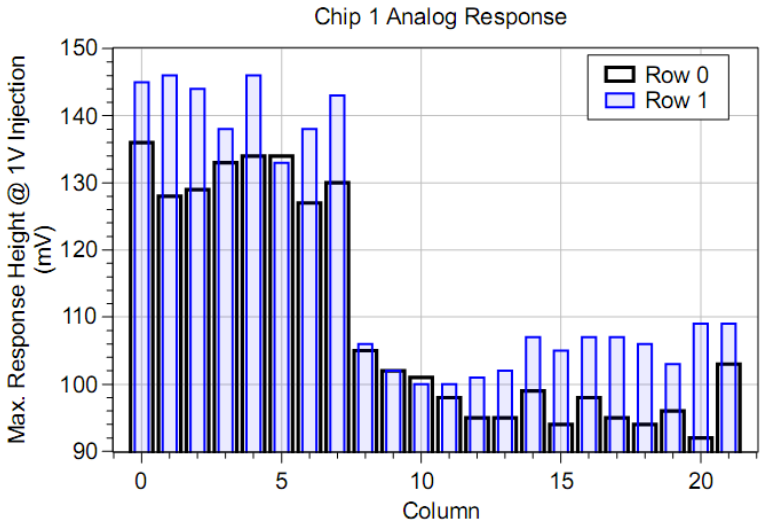
Oxford/Glasgow

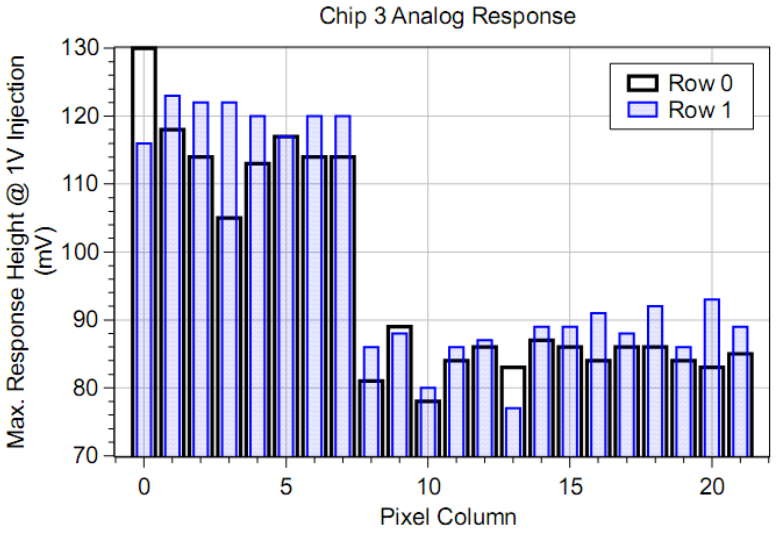
Signal Response Uniformity

Note that 1st 8 pixels have different gain due to linear transistors used.



RAL, Oxford, Glasgow, DESY

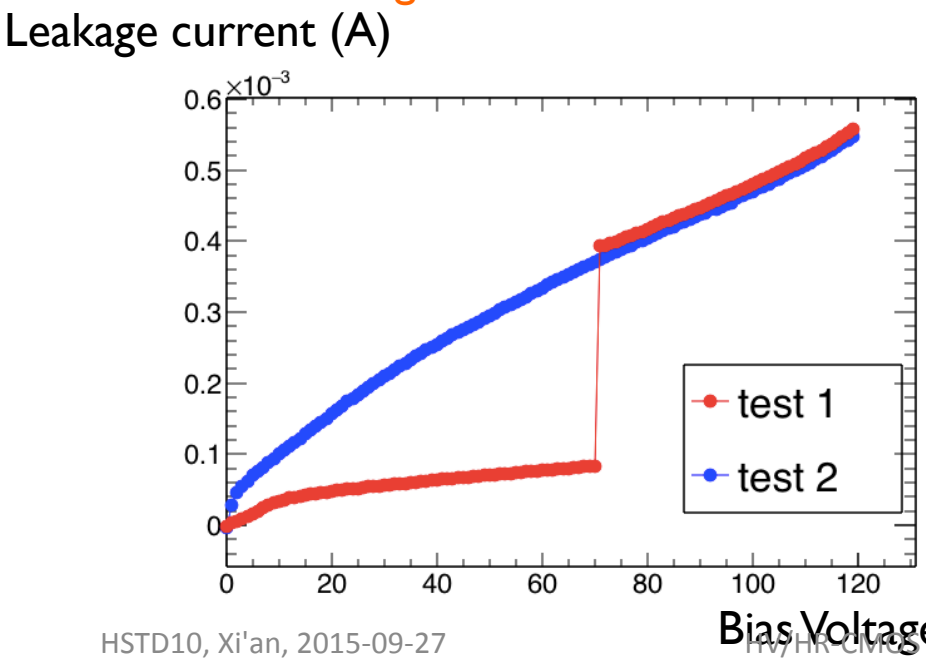




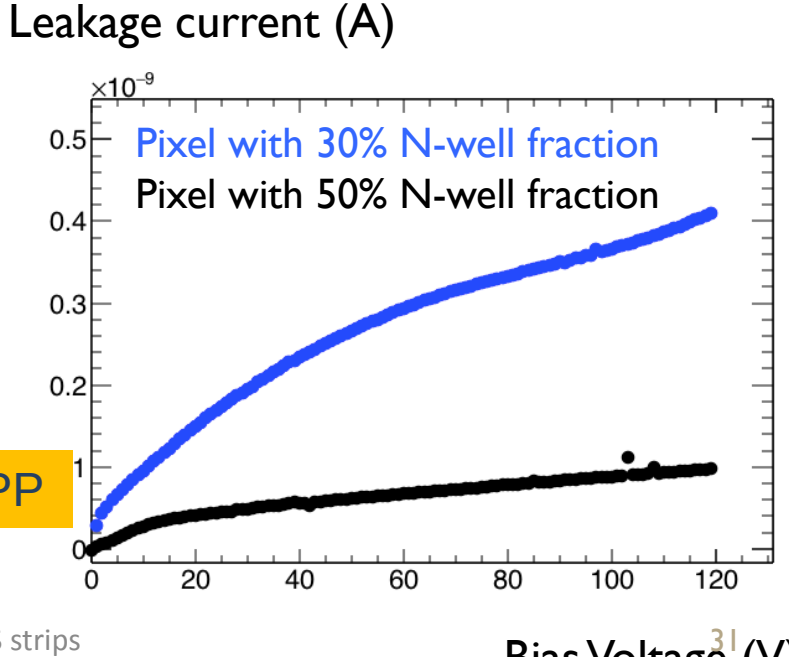
I-V measurement in gamma irradiated CMOS chip

- No break down in pixel array with 50% N-well fraction
- break-down like behavior in part of the pixels with 30% N-well fraction
- Perform two test in one of 30% N-well fraction pixel
  - Break down in the first scan at about 70V.
  - Leakage current increase by order of magnitude
  - The leakage current remain high after the first test.

Pixel size: 45X200μm
with 30% N-well fraction
30 Mrad gamma radiation



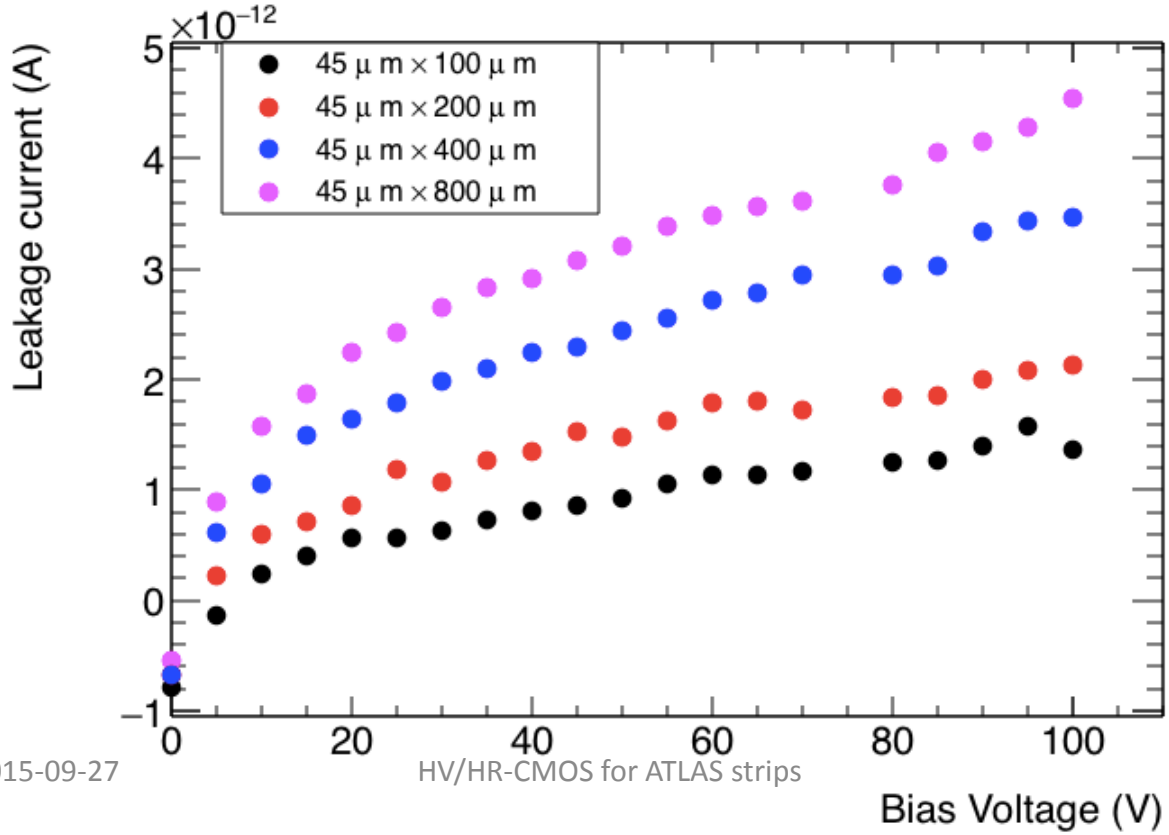
Pixel size: 45X200μm
With 30% N-well fraction
100 Mrad gamma radiation



SCIPP

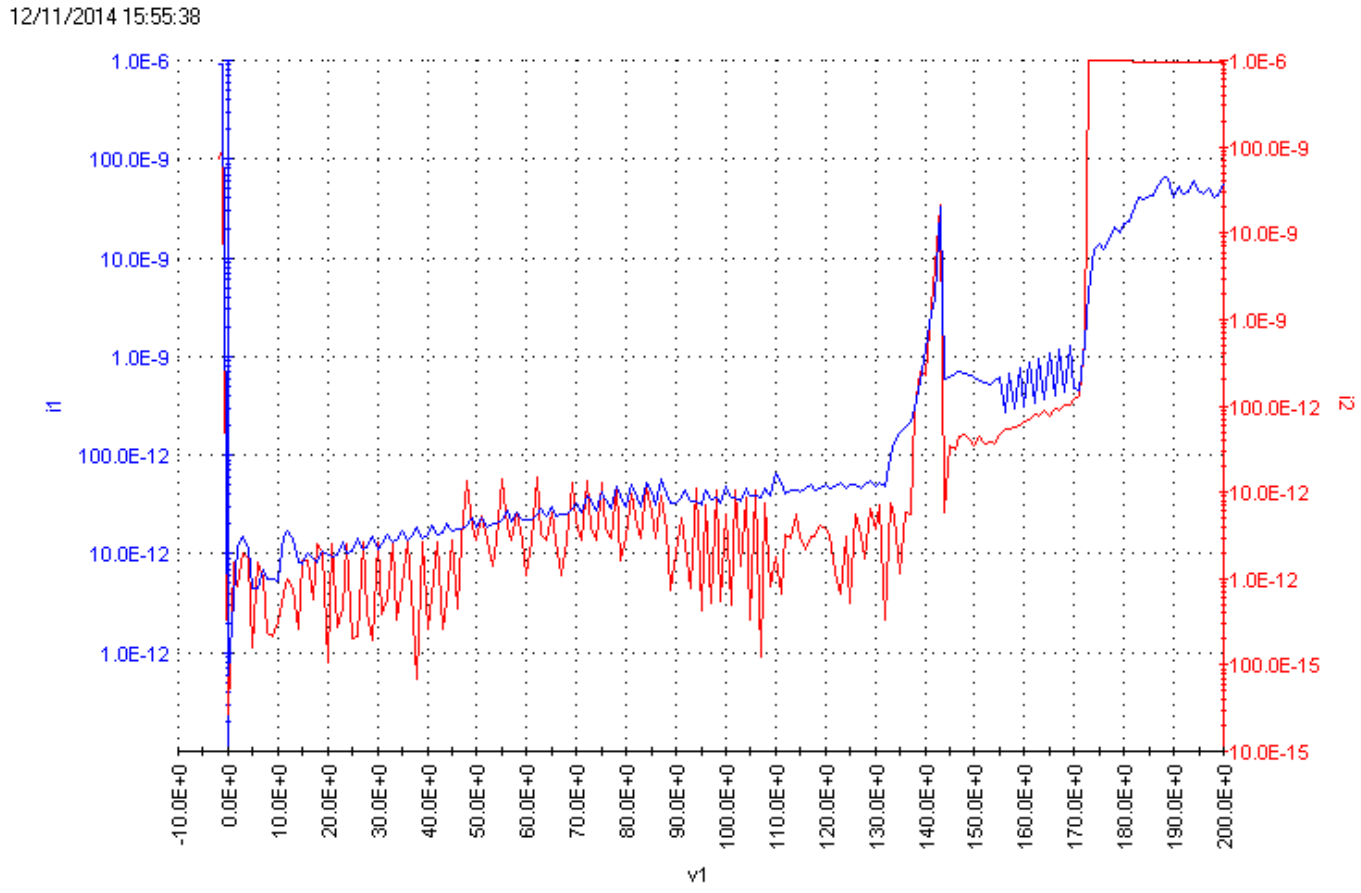
Central pixel IV

- Design of pixel in CHESS1 chip
  - Two design rule in AMS HV-CMOS technology ： 60V and 120V
  - pixel array layout in CHESS1 chip follows the 120V design rule
- I-V measurement result
  - Can Biased up to 120V without breakdown
  - Low leakage current (pA level)
  - Leakage current proportional to pixel size.



SCIPP

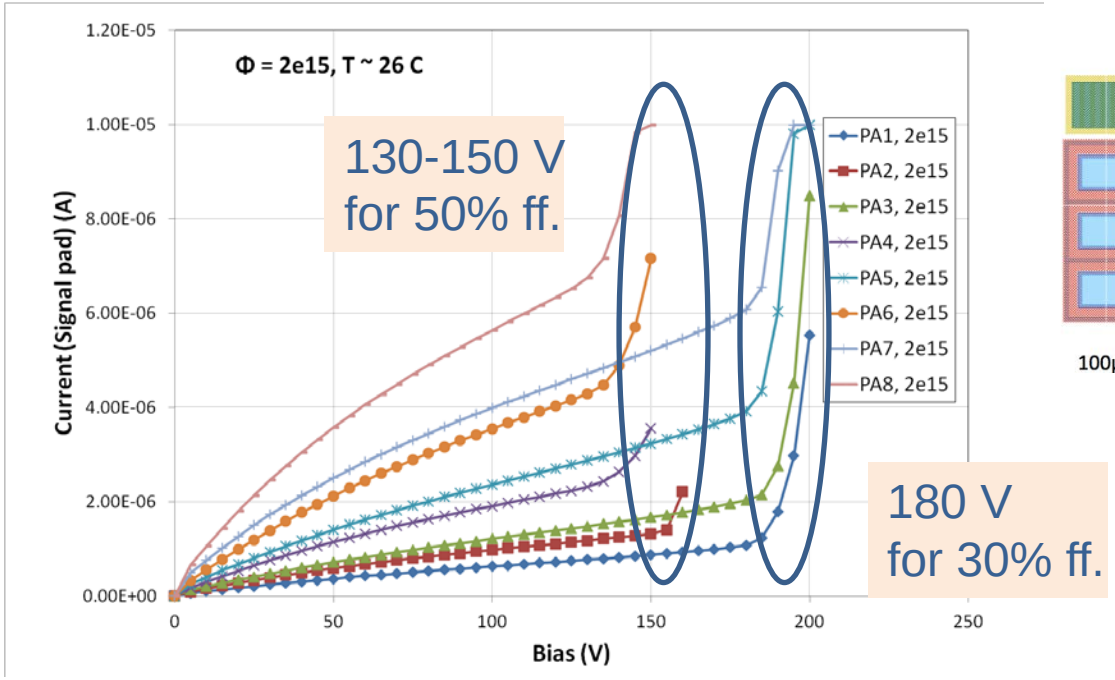
IV curves above 120V

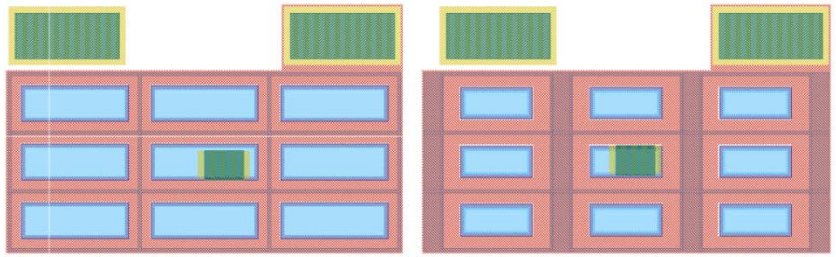


SLAC

Breakdown Voltages with Top Biasing

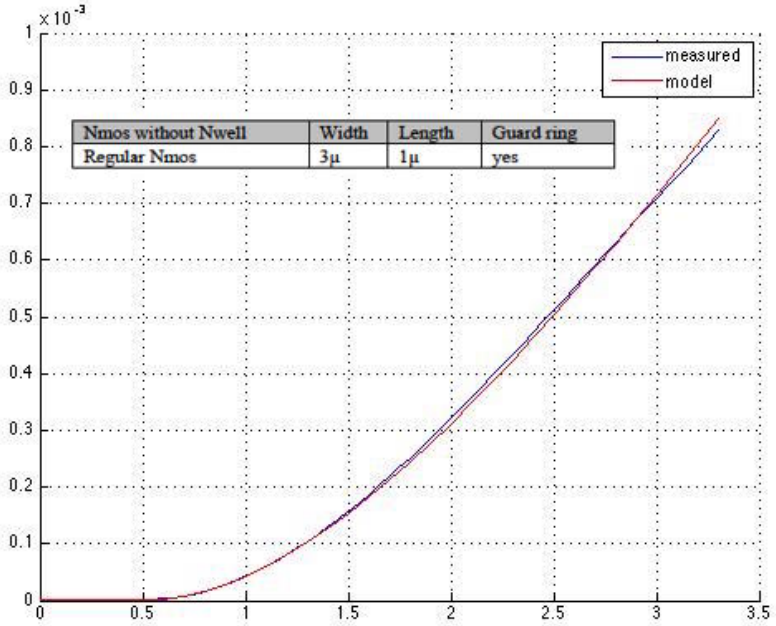
- V(bd): Typically rises with fluence for standard sensors. But seems to be stable with top-side biasing due to voltage drop along finite/small distances between the implants. (Shown for 2e15 neq/cm^2 , but the V(bd) is very similar for 2e15 neq/cm^2)

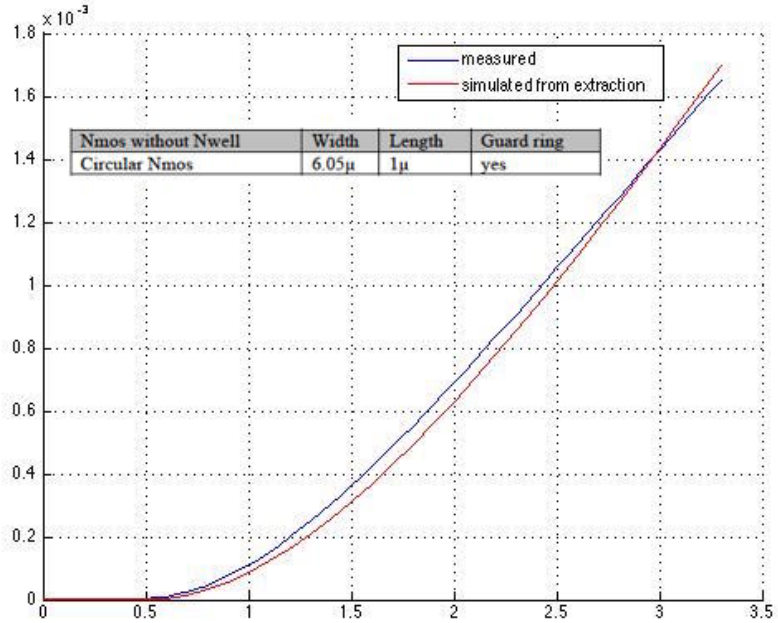


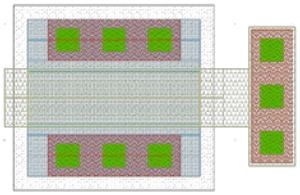


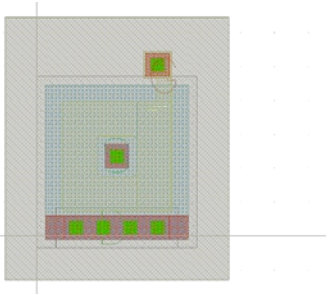
Ljubljana

NMOS CHESS1



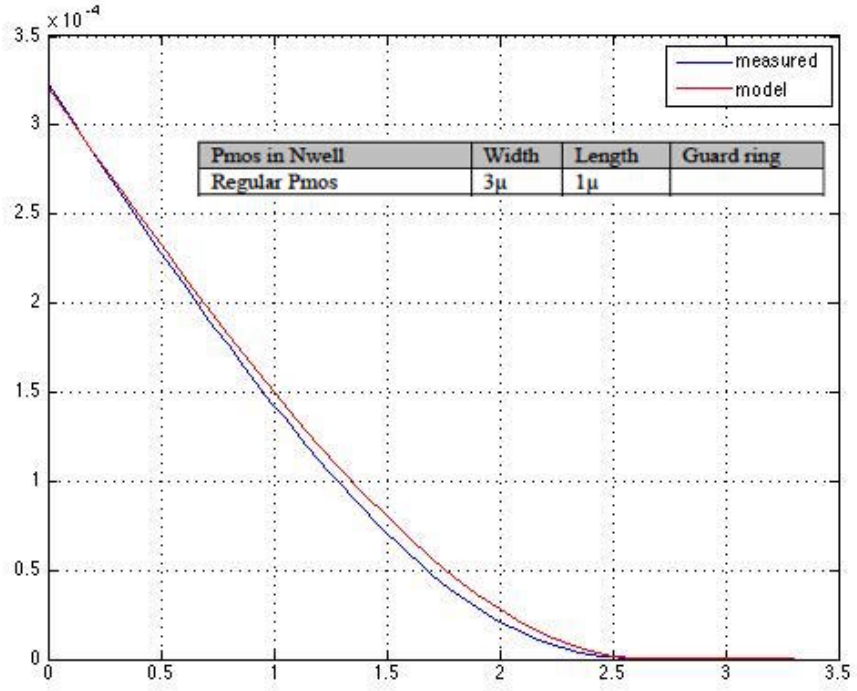






RAL, IHEP, SCIPP

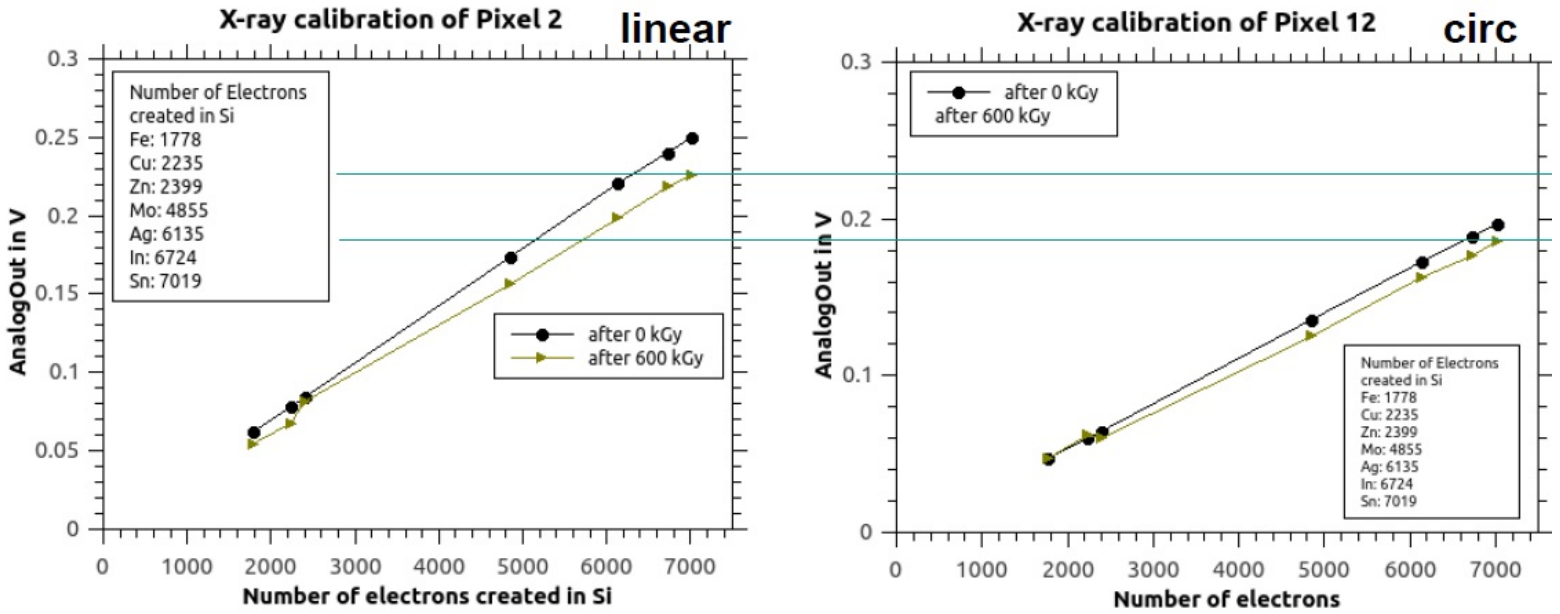
PMOS CHESS1



RAL, IHEP, SCIPP

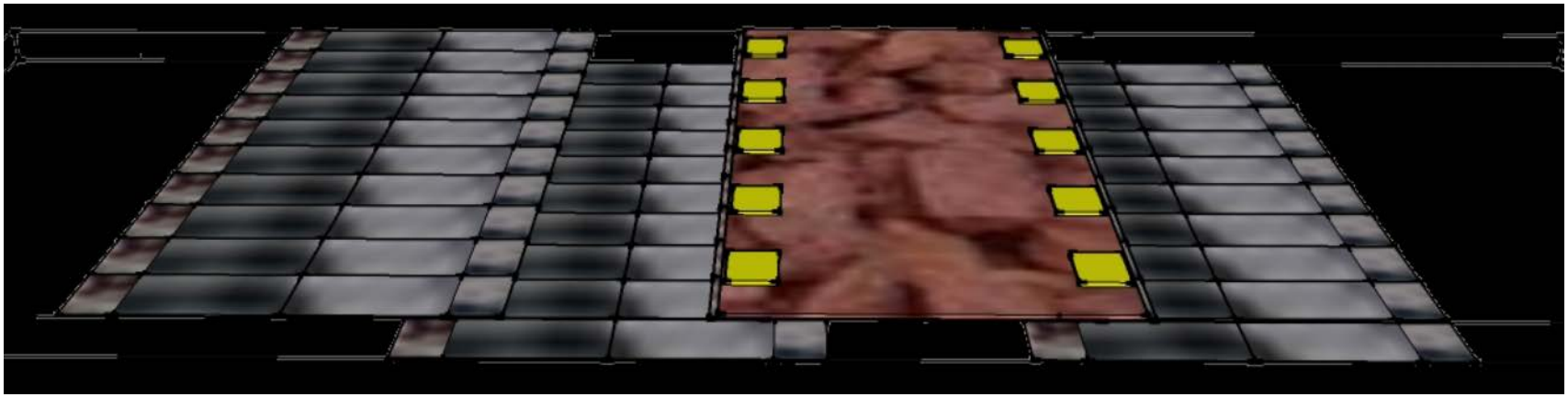
Amplifier Gain

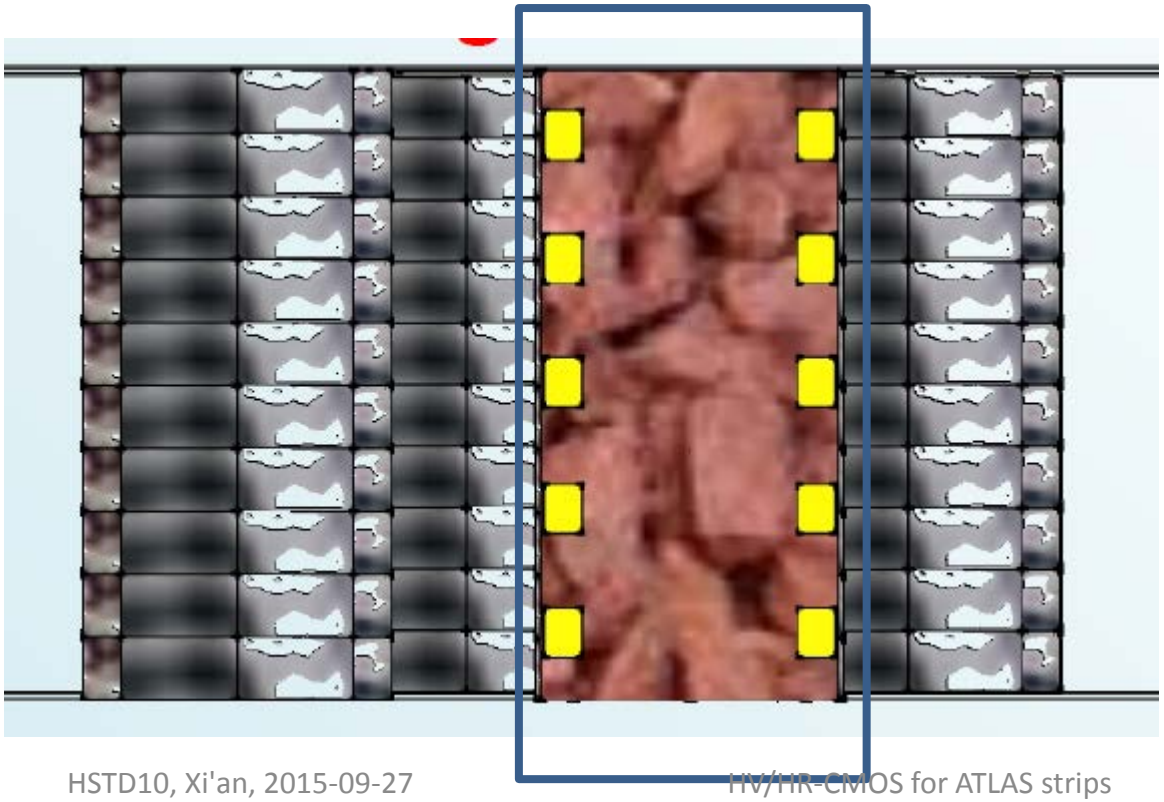
Amplifiers on the HVStripV1 chip have been calibrated with different x-ray sources. They show quite linear behavior. The variation with dose is relatively small.



KIT

Module Concept - Barrel





Barrel module

- Interleaved placement on two sides of the stave
- 10 cm width
- Sensors in ‘rows’ of reticules
- Single hybrid
  - ✓ 10 ABCn’
  - ✓ HCC’
  - ✓ DC/DC convertor
  - ✓ Mechanical support