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Investigation of HV/HR-CMOS technology for the ATLAS Phase-II Strip Tracker Upgrade

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ATLAS has formed strip CMOS project to study the use of CMOS MAPS devices silicon strip sensors for the Phase-II Strip Tracker Upgrade. This choice of sensors promises several advantages over the conventional baseline design, such as better resolution, less material in the tracking volume, and faster construction speed. At the same time, many design features of the sensors are driven by the requirement of minimizing the impact on the rest of the detector. Hence the target devices feature long pixels which are grouped to form a virtual strip with binary-encoded z position. The key performance aspects are radiation hardness compatibility with HL-LHC environment, signal timing resolution compatibility with bunch crossing period of 25 ns, as well as extraction of the full hit position with full-reticle readout architecture.

To date, several test chips have been submitted using two different CMOS technologies. The AMS 350 is a HV-CMOS process, which features the sensor bias of up to 120 V. The TowerJazz 180 nm HR-CMOS process uses a high resistivity epitaxial layer to provide the depletion region on top of substrate. We have evaluated charge collection, output signal timing, gain and noise of these chips. The results strongly support the radiation tolerance of these devices to radiation dose of the HL-LHC in the strip tracker region (60 Mrad and 2x10ˆ15 neq/cmˆ2).

We will also describe our next chip designed as a full-reticle length sensor for prototyping the readout architecture and to investigate large-chip effects, such as common mode noise. The hit encoding engine is capable of reading out up to 8 hits from a pre-defined region. The hits are then transferred off-sensor via high-speed bus to reduce the wirebond count. Placement of the comparators and the bulk wafer resistivity will be varied to find the optimal performance.

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