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Development of n^+-in-p planar pixel sensors for very high radiation environments, designed to retain high efficiency after irradiation

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We have been developing planar-process pixel sensors in p-type 6-in. silicon wafer aiming for applying the pixel sensors for very high radiation environments such as high luminosity upgrade of the large hadron collider (HL-LHC). The planar process has been established well and is a cost-effective solution for the pixel sensors covering large area of a tracking detector. The p-type silicon wafer is kept as p-type after radiation damage. This fact simplifies the lithographic process only required in the side of the pixel structure and keeps the cost to be the minimum.

In our previous prototype pixel sensors, we have identified locations in the pixel structure, especially under the bias rail, where we lose the efficiency for detecting passing charged particles after irradiation. Although the pixel sensor under development is a directly coupled (DC) sensor, we have implemented a biasing structure for quality assurance before bump-bonding readout chips. The new prototype sensors have been designed to mitigate the efficiency loss due to the biasing structure by re-locating the bias rail and the bias resistor, being hidden inside the area of the pixel electrode, together with other variations of the biasing structure.

The new pixel sensors, thinned to 150 μm thick, have been fabricated to mate the ATLAS pixel readout ASIC, FE-I4, bumpbonded, irradiated to a fluence of 3 to 5×10^{15} 1-MeV neutron-equivalent (neq)/cm^2 at CYRIC, and evaluated with the beam of particles at CERN and DESY. The efficiencies of the different pixel structures are compared and new pixel structures are shown to have improved the efficiency greatly. The physics under the bias rail has been understood by using a semiconductor technology simulation program (TCAD).

Primary author:
Y. Unno

Co-Authors:
ATLAS-Japan Silicon Collaboration and Hamamatsu Photonics K.K.

Primary author: UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP))

Presenter: UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP))

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