Belle II Silicon Vertex Detector

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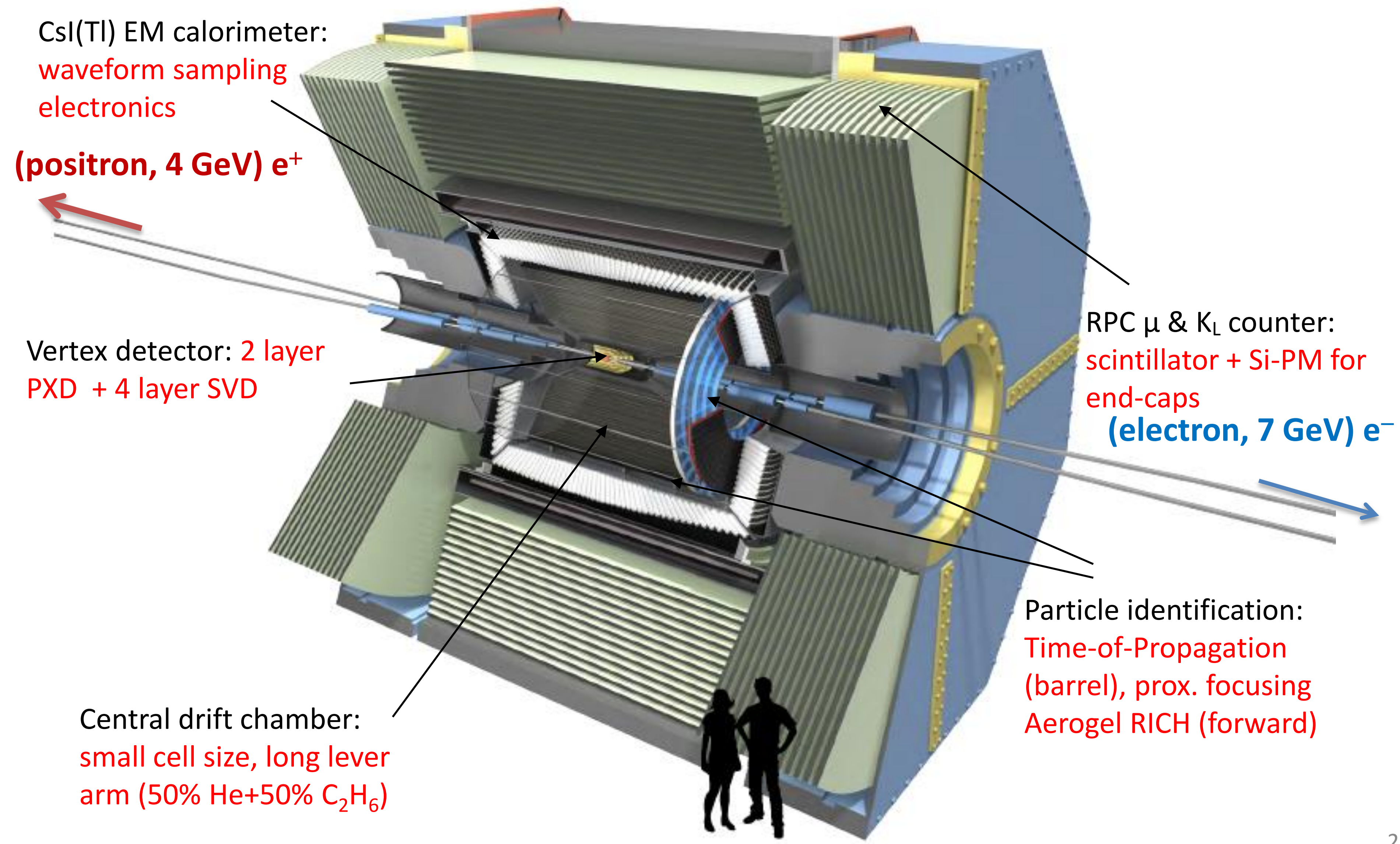
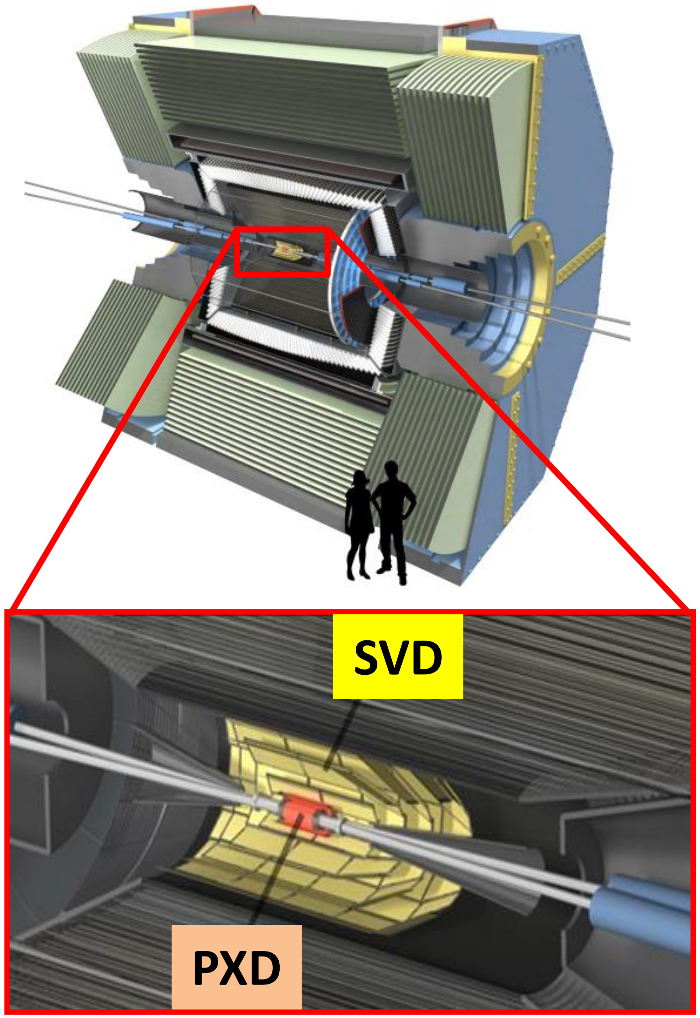
Belle II @ SuperKEKB

- Search for physics beyond the standard model using high-statistics samples of B and D mesons and τ leptons ➡ design luminosity 8×10^{35} cm^{-2}s^{-1}



Belle II Vertex Detector (VXD)



- **Determine the vertex position of the weakly decaying particles**
- **Measure the two-dimensional track position and momentum for charged particles**

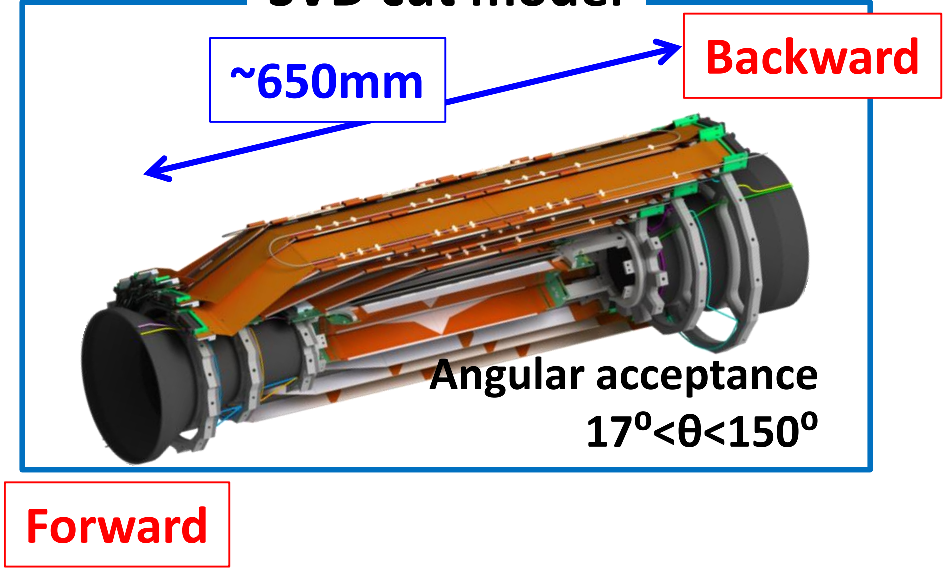
- PiXel Detector (PXD)
  - ➢ See the next talk
- Silicon Vertex Detector (SVD)
  - – Double-sided silicon strip detectors

VXD requirements

- Fast – to operate in high rate environment
- Excellent spatial resolution
- Radiation hard (up to 100 kGray)
- Good tracking capability – to track particles down to 50 MeV in p_T

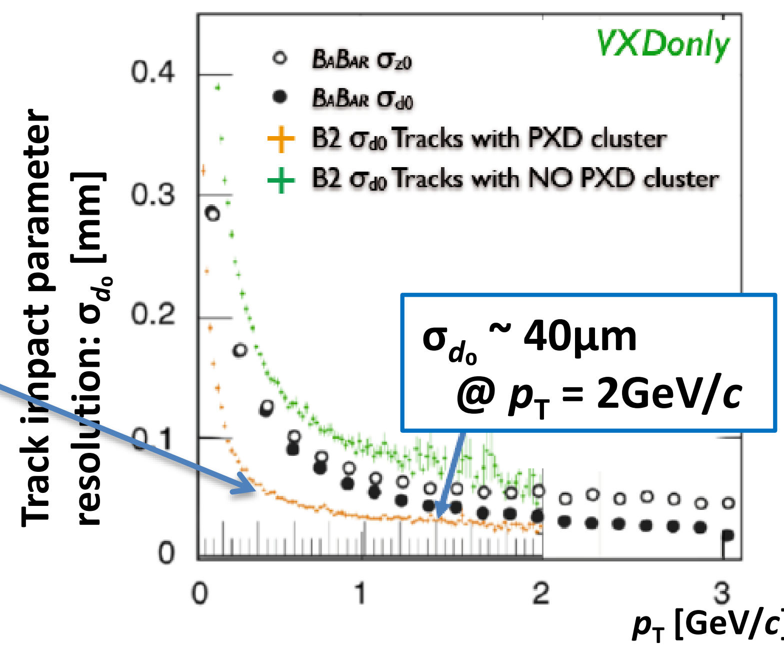
SVD Structure Overview

SVD cut model

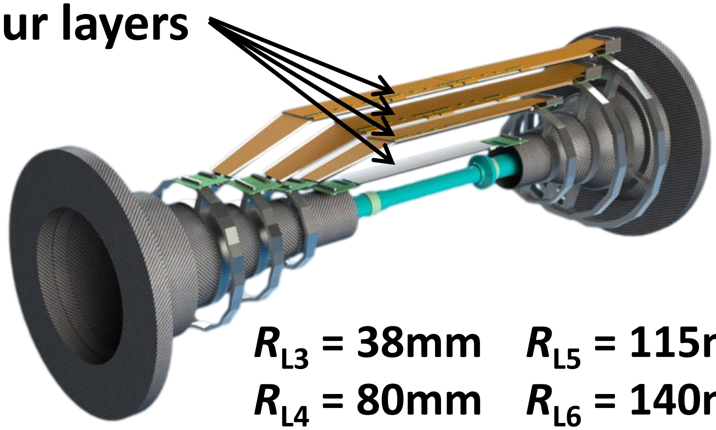


Layer	Institute
3	University of Melbourne
4	TIFR Mumbai
5	HEPHY Vienna
6	IPMU University of Tokyo
FW & BW	INFN Pisa

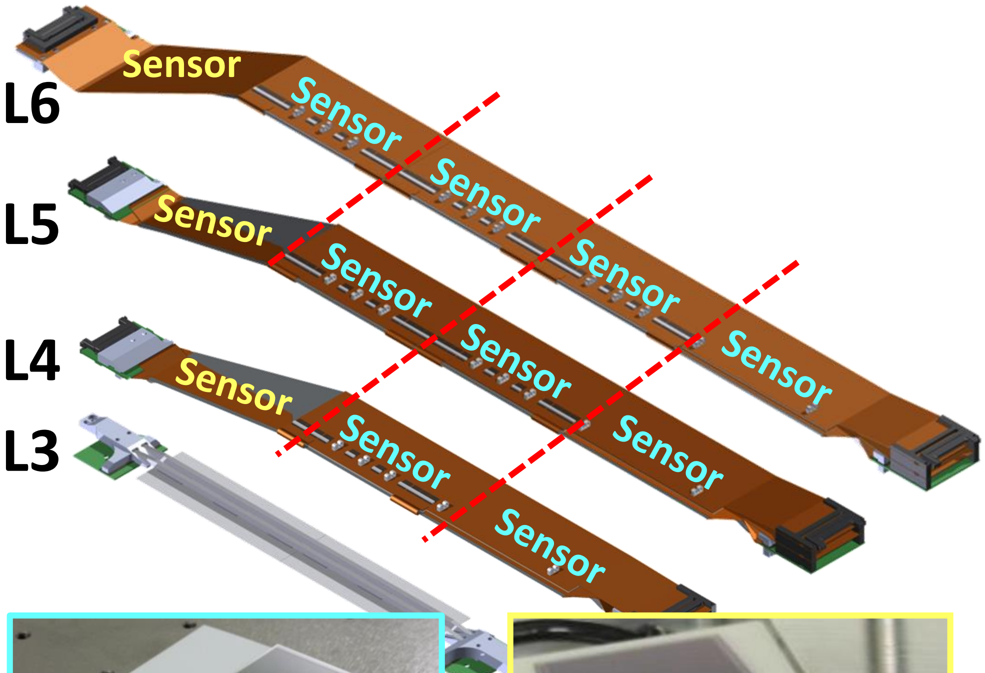
- **4 SVD layers (L3 to L6) composed of ladders arranged in a windmill structure**
- **Improved resolution at IP with respect to Belle I**
- **Very light weight – only 0.58% X_0 per layer**



SVD Ladder Layout



R_{L3} = 38mm R_{L5} = 115mm
R_{L4} = 80mm R_{L6} = 140mm



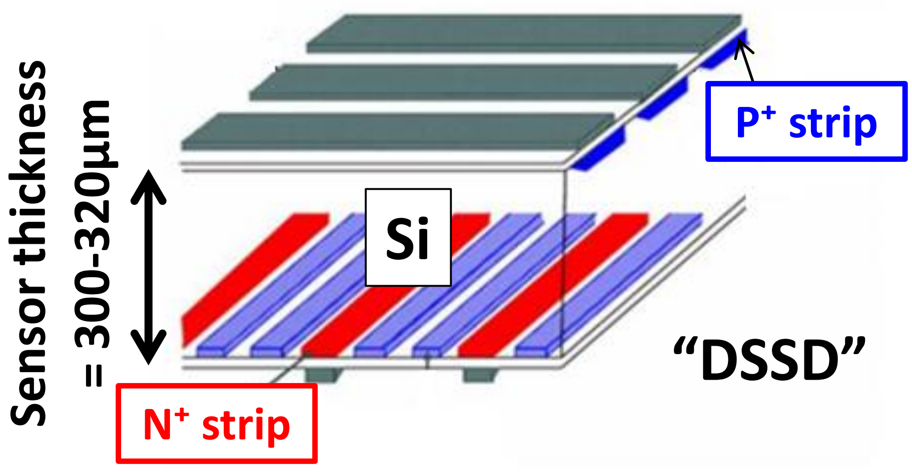
Layer	Ladders	Sensors / Ladder	APVs
6	16	5	800
5	12	4	480
4	10	3	300
3	7	2	168


Rectangular sensor


Trapezoidal sensor

SVD Sensors and Readout ASIC

Double-sided Si strip detector

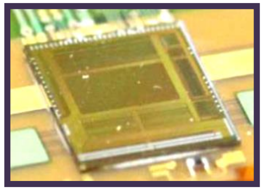


	Rectangular	Trapezoidal
# of *p*-strips	768	768
p-strip pitch	75 µm	50…75 µm
# of *n*-strips	512	512
n-strip pitch	240 µm	240 µm
Active area	57.7x122.9mm²	5890mm²

Readout ASIC (APV25)

- As high hit rate is anticipated at Belle II, the readout chip should have a short signal shaping time for low noise and a good radiation hardness

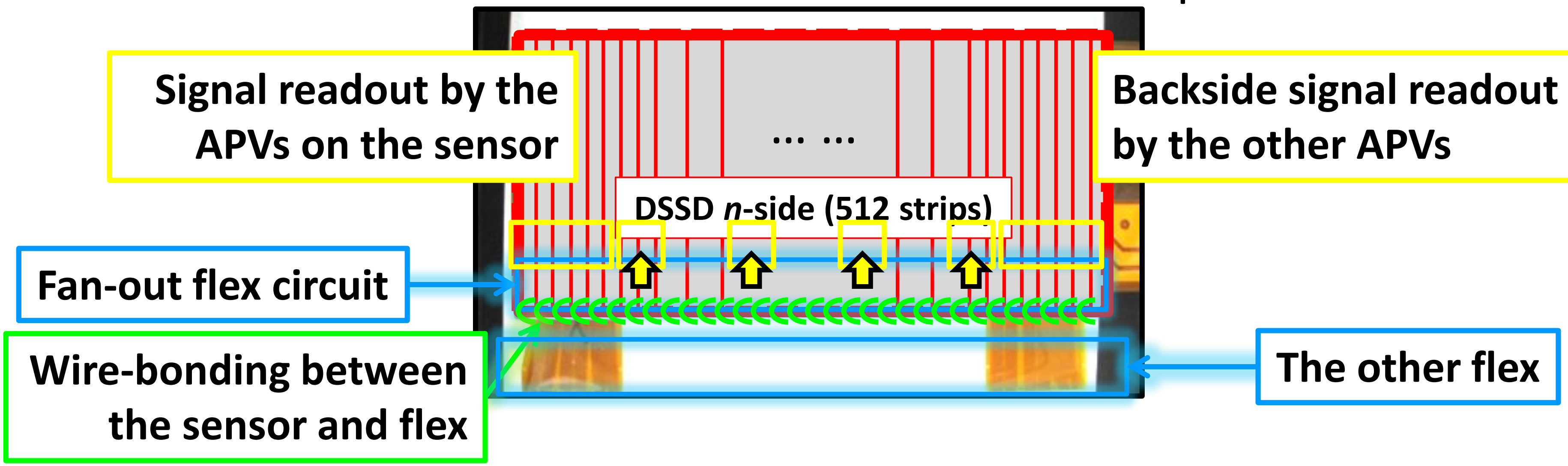
We adopted the APV25



- The APV25 was originally developed for the CMS experiment
  - Shaping time = 50 ns
  - Radiation hardness > 1 MGray
- Other characteristics
  - # of input channels = 128 / chip
  - 192-deep analog pipeline for the dead-time reduction
  - Thinned down to 100 µm for the material budget reduction

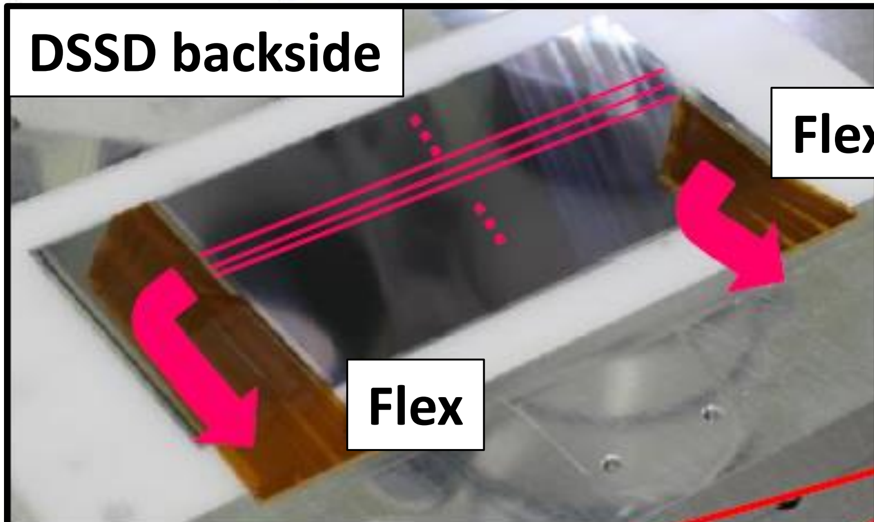
Chip-on-Sensor "Origami" Concept

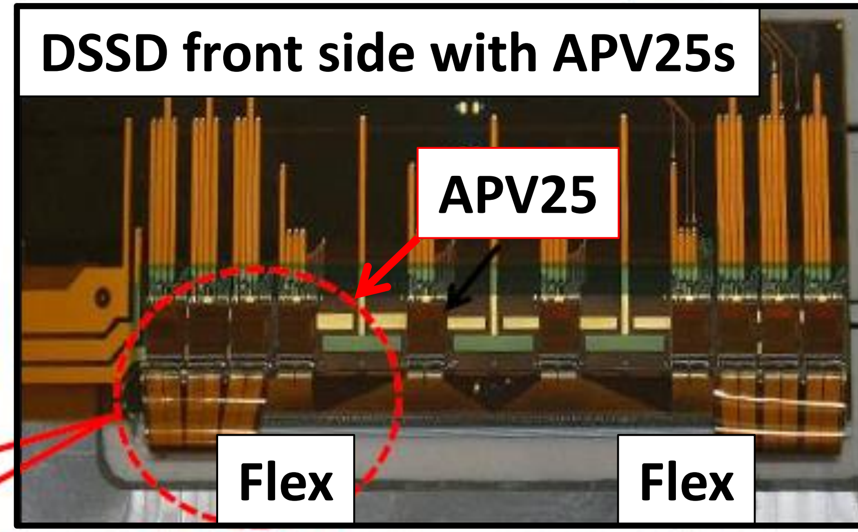
- APV25 on sensor
  - APVs for the inner sensors are placed directly on DSSDs to reduce the analog path length (capacitive noise)
- P-side readout
  - Signals on the sensor backside are brought to the upper side by other flex circuits and readout by APV25 chips mounted on the top

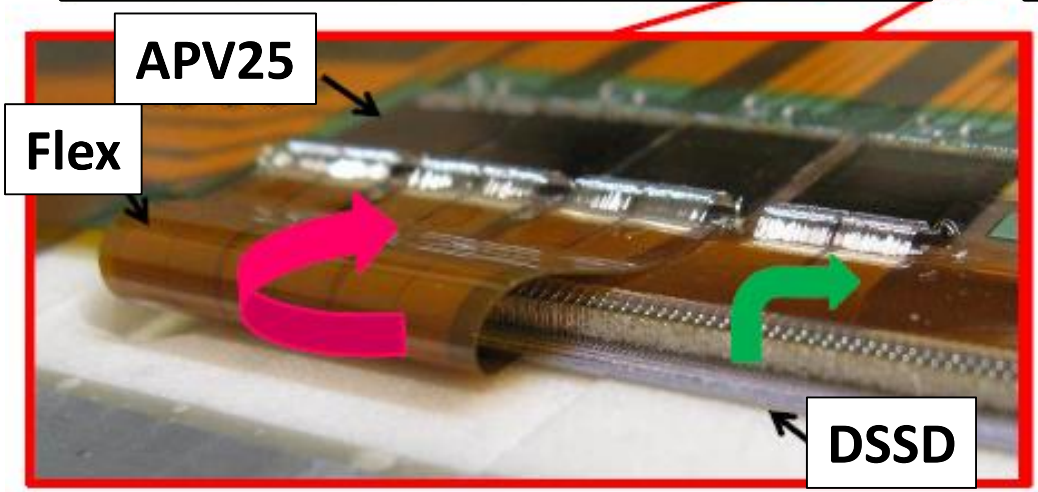


Readout ASICs on the same side & line → easier chilling by a single cooling pipe

A Snapshot of the "Origami" Concept

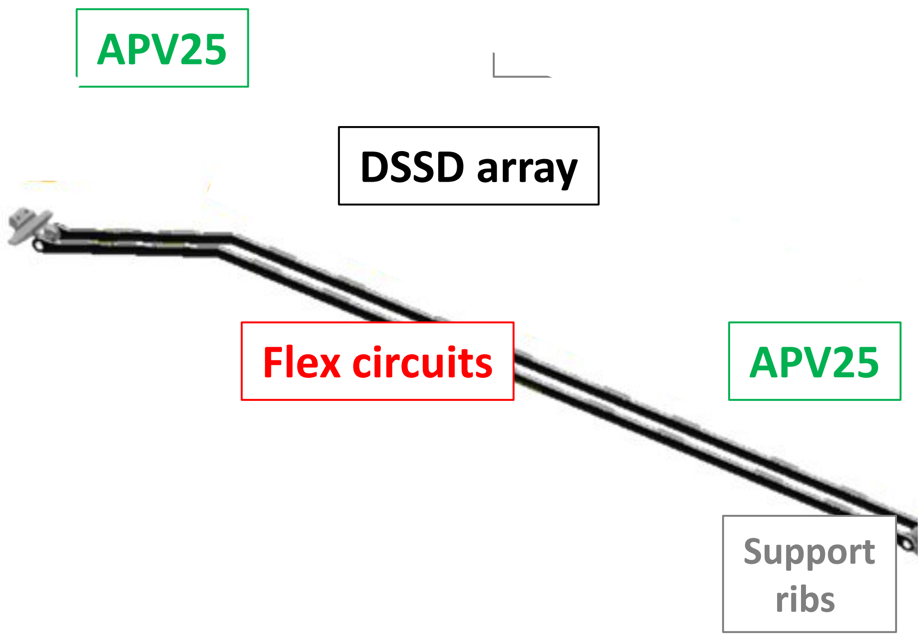






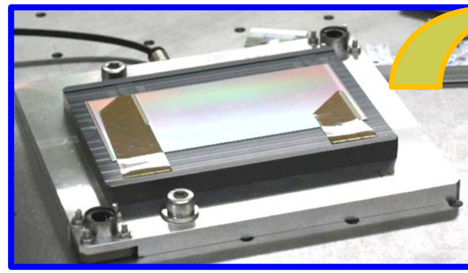
The backside signals are transmitted to the APV25 via *bent* (and glued) flex circuits

SVD Ladder Assembly

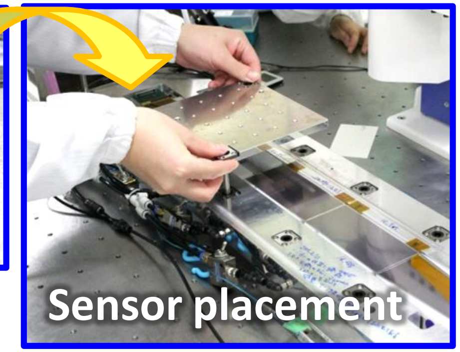


Precision DSSD alignment

DSSDs are handled with precision assembly jigs [*O*(50µm)], on which the sensors are fixed by vacuum chucking

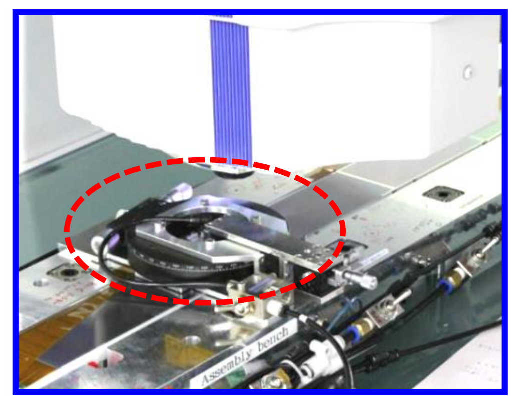


Sensor fixed on a jig



Sensor placement

Sensors are aligned with a precision of 10µm by a position tuning jig with monitoring through a CMM

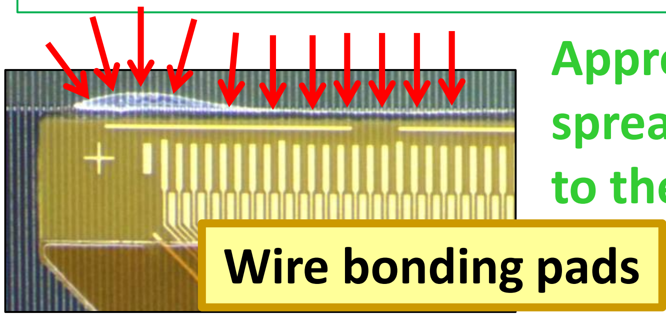


SVD Ladder Assembly

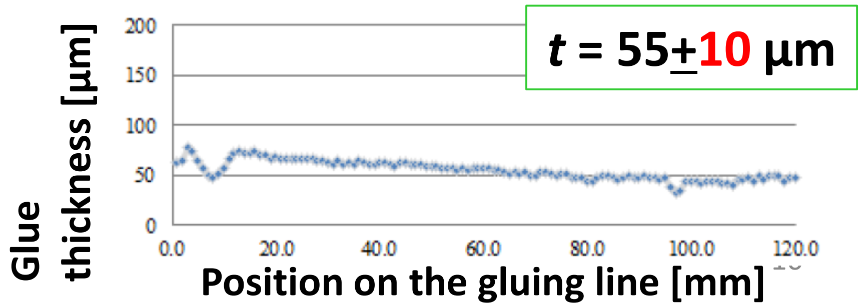
Ladder fabrication: gluing

Ladders are fabricated by gluing the components by Araldite®2011

Glue spread below bonding pads can affect the bonding yield and pull strength → glue amount and glue lining are controlled by a gluing robot



Appropriate spread of glue to the flex edge



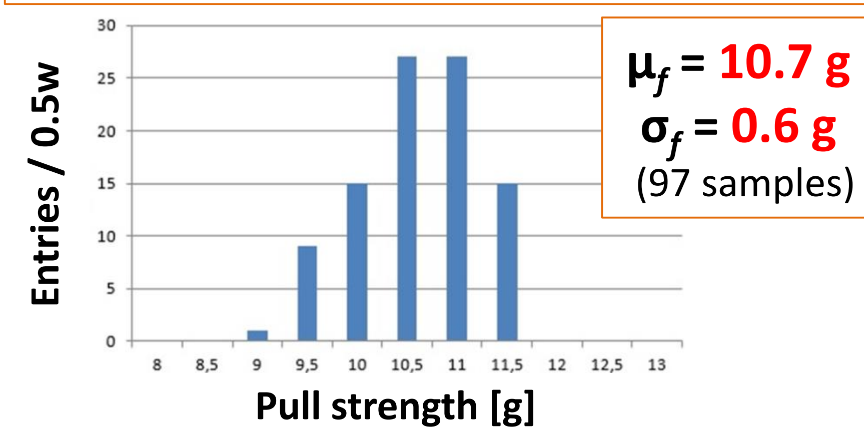
Electrical connection: wire bonding

The flex↔DSSD strips and flex↔APVs are electrically connected by the wire bonding

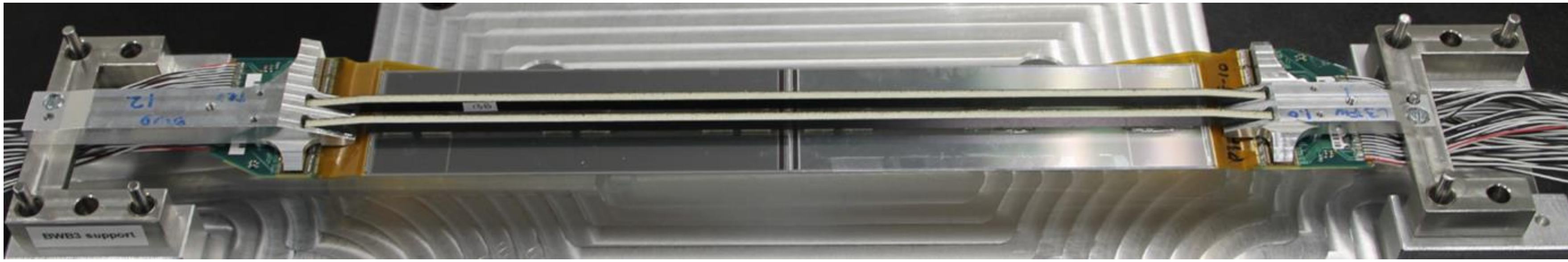
with Aℓ(99%) wire (ϕ = 25µm)

Number of total bonds = 450k

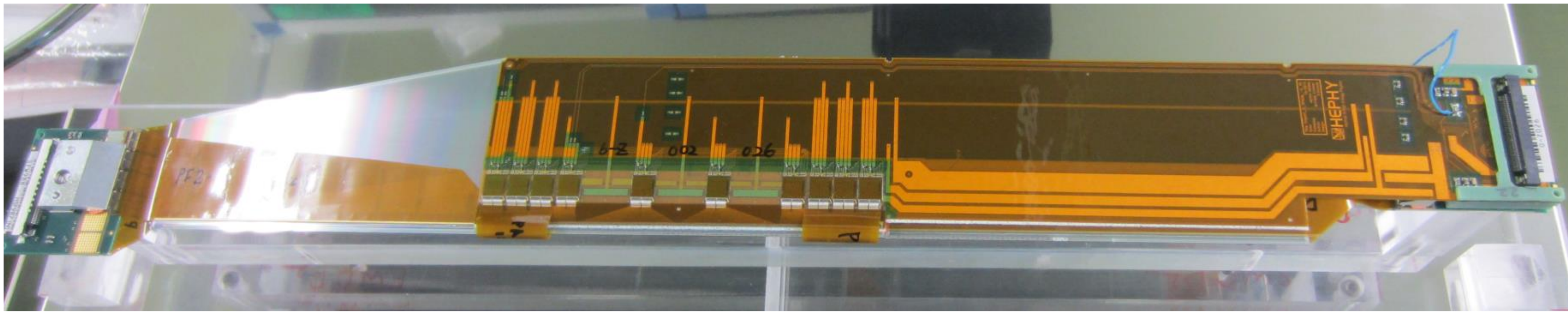
Bonding machine parameters are fine tuned to realize yield > 99% and pull strength f:μ_f > 5g, σ_f/f < 20%



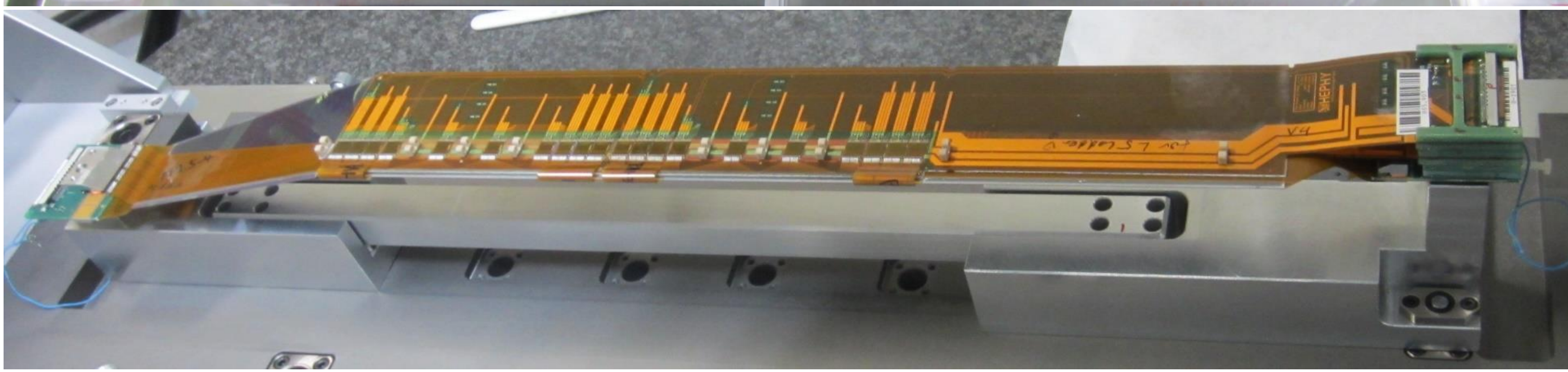
Assembled Ladders



L3



L4

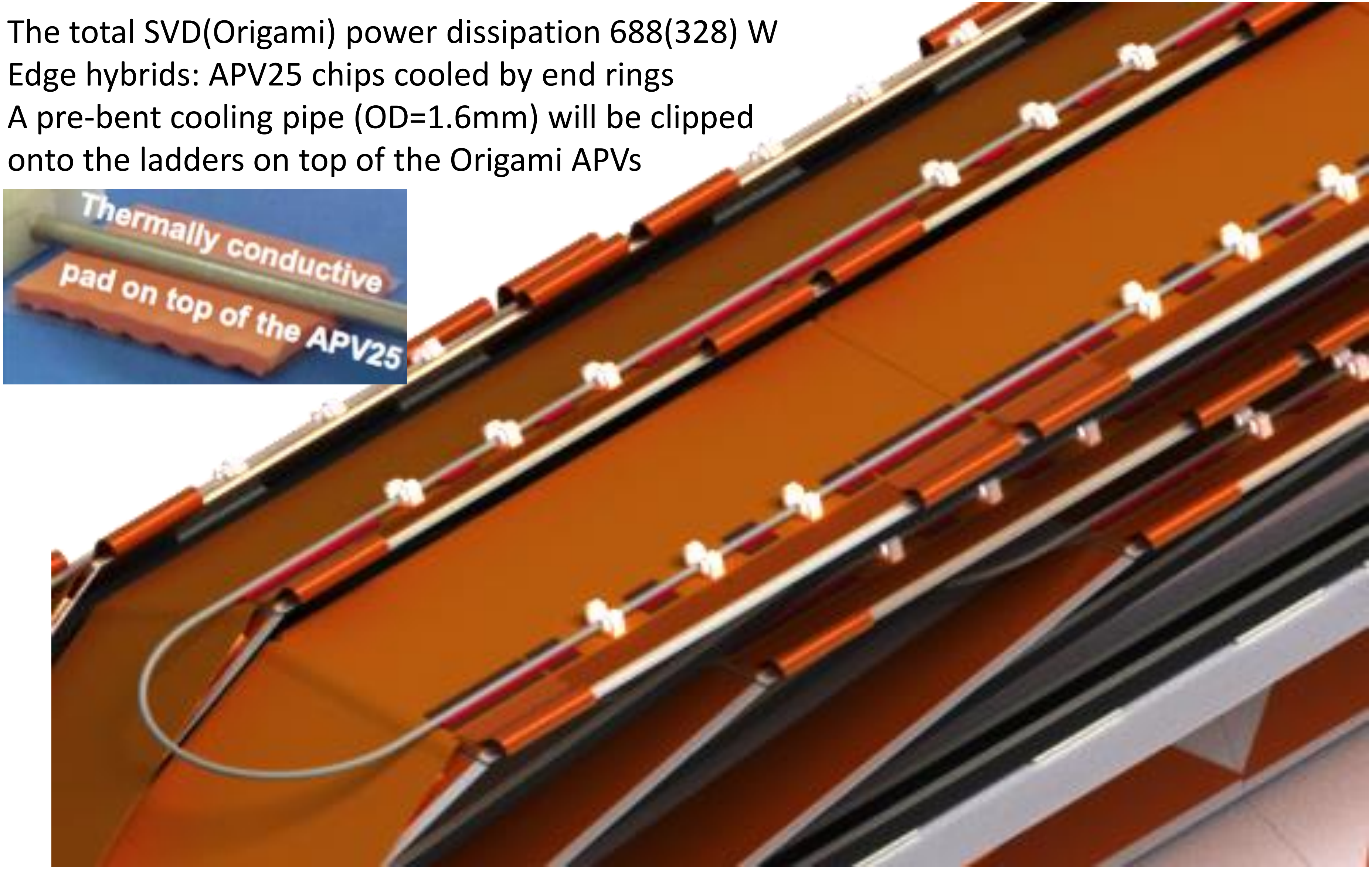


L5

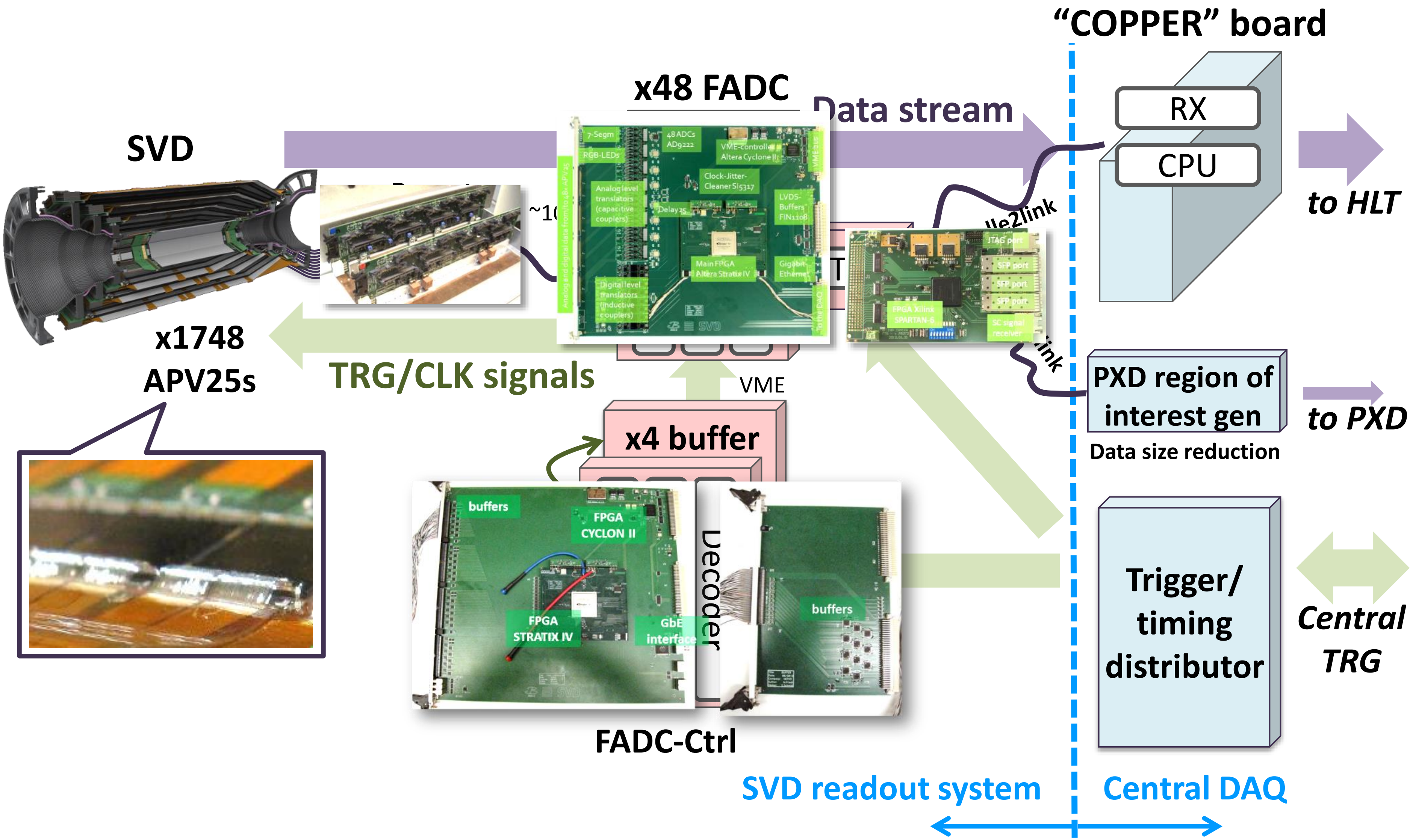
L6

CO_2 Cooling

The total SVD(Origami) power dissipation 688(328) W
Edge hybrids: APV25 chips cooled by end rings
A pre-bent cooling pipe (OD=1.6mm) will be clipped onto the ladders on top of the Origami APVs



FADC Readout System

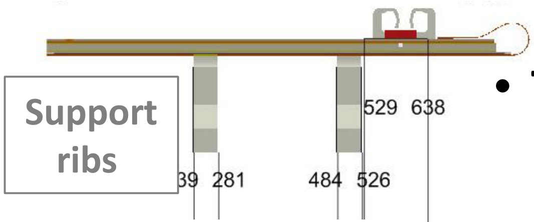


Prototypes of all components have been developed

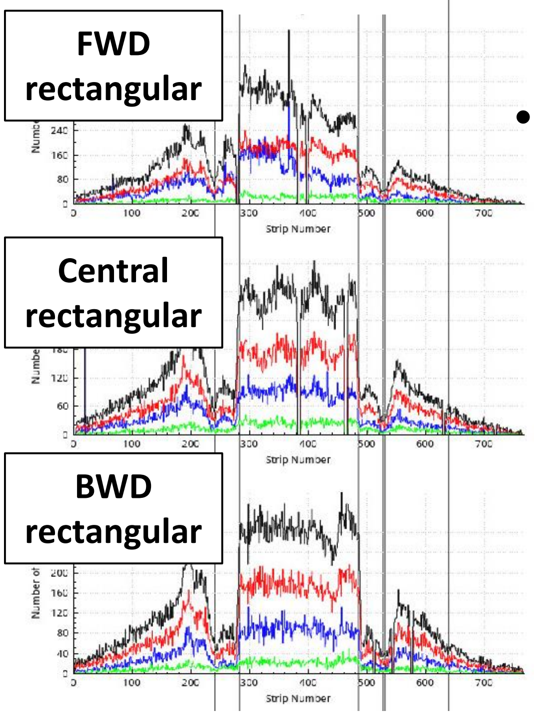
Electrical Performance Studies

Study on the full functioning ladder

Ladder cross-section



Hit maps

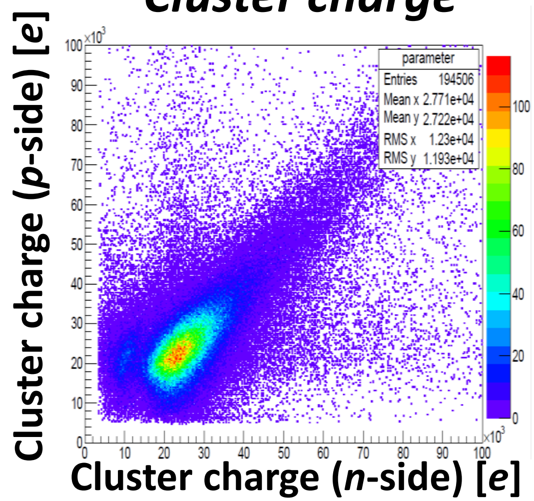


- The ladder is bombarded by β-rays from ^{90}Sr (12.3MBq)
- Shades by the support ribs are clearly observed in the hit maps

Simultaneous operation of origami sensors worked as expected

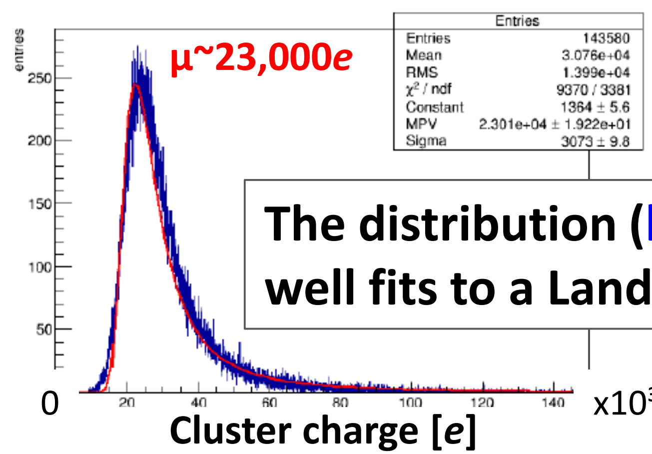
Study on a single sensor

Cluster charge



Correlation between *p*- and *n*-side clusters

P-side cluster charge (#strip≥2)

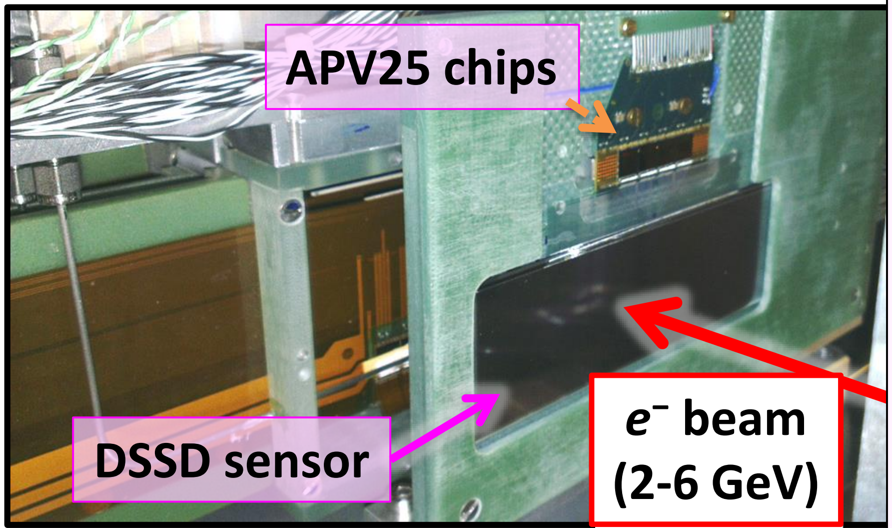


The distribution (blue) well fits to a Landau (red)

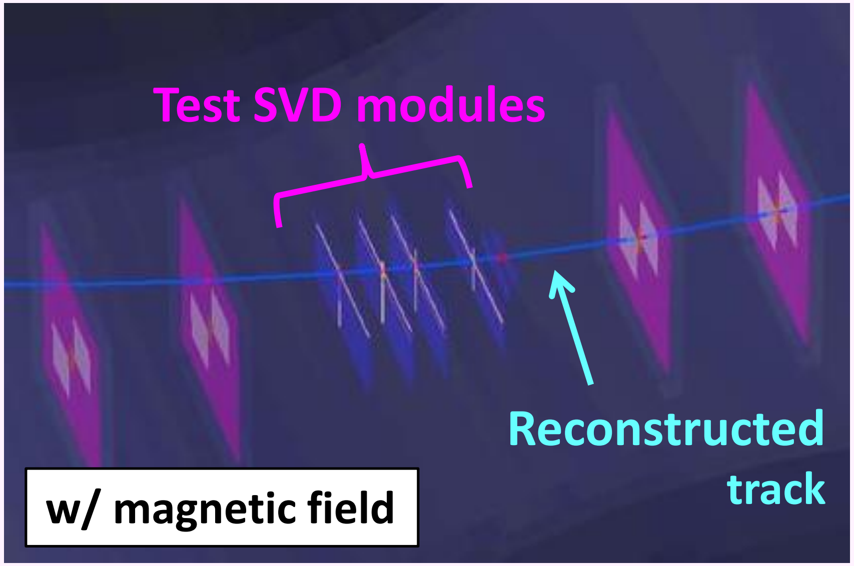
SVD+PXD DAQ Test @ DESY Beam Line

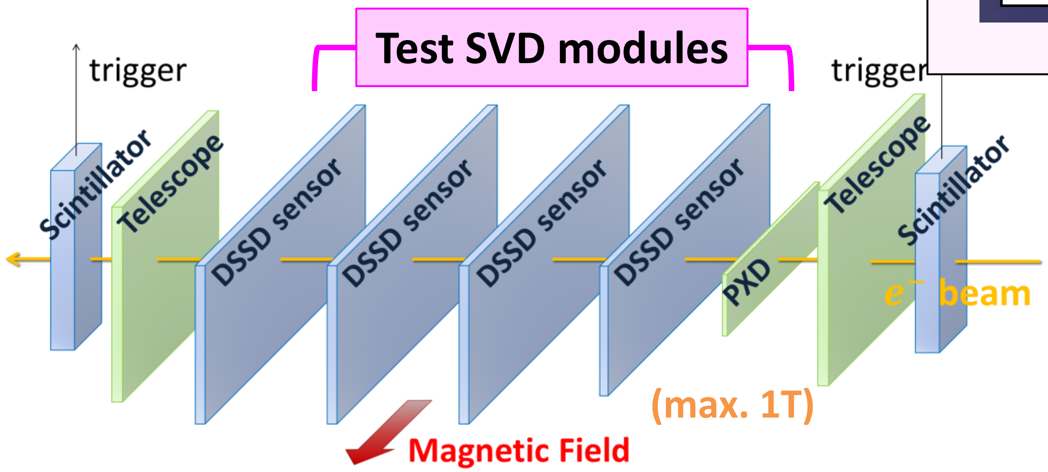
Jan-Feb 2014

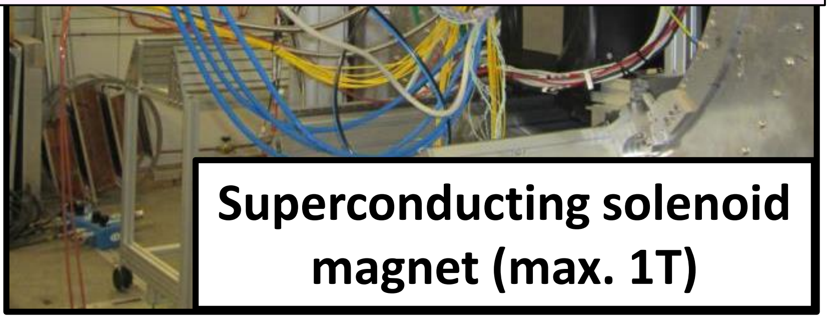
4-layers Test SVD modules



Event display

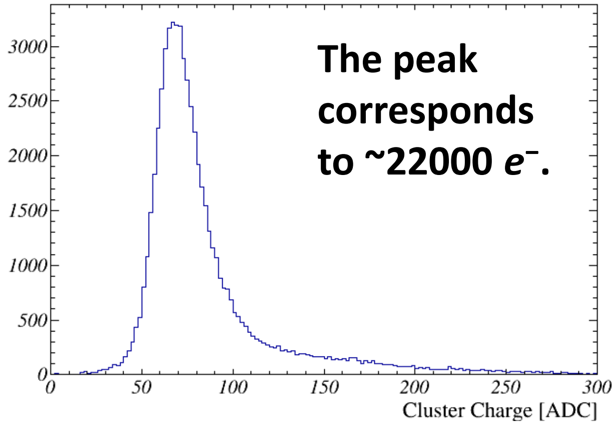




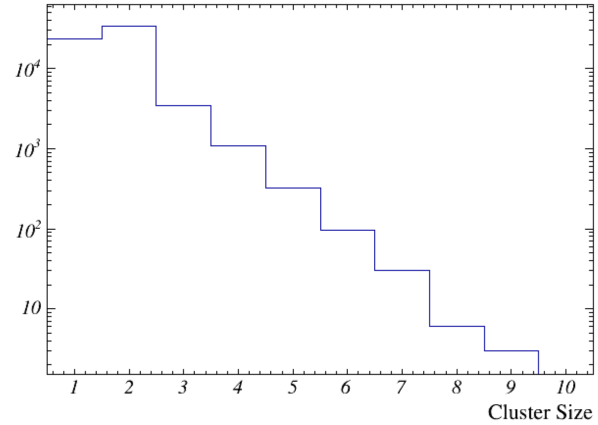


SVD+PXD DAQ Test @ DESY Beam Line

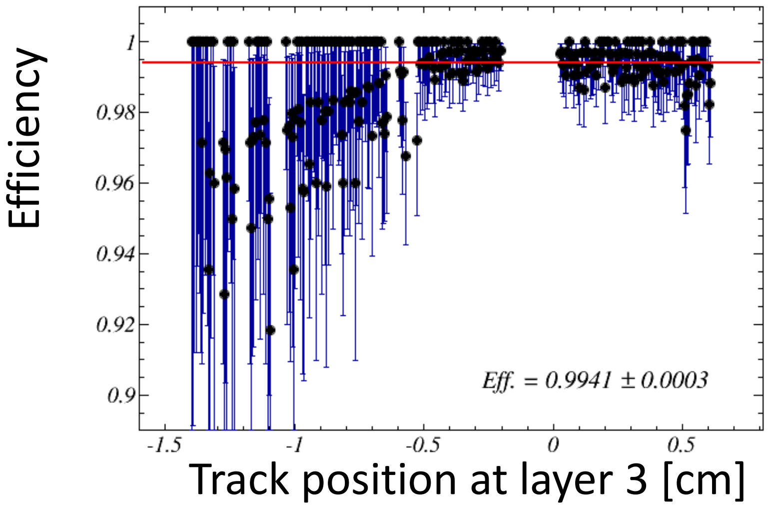
Cluster charge distribution



Cluster size distribution **(P side layer 3 DSSD)**



Cluster hit efficiency for tracks extrapolated from other layers

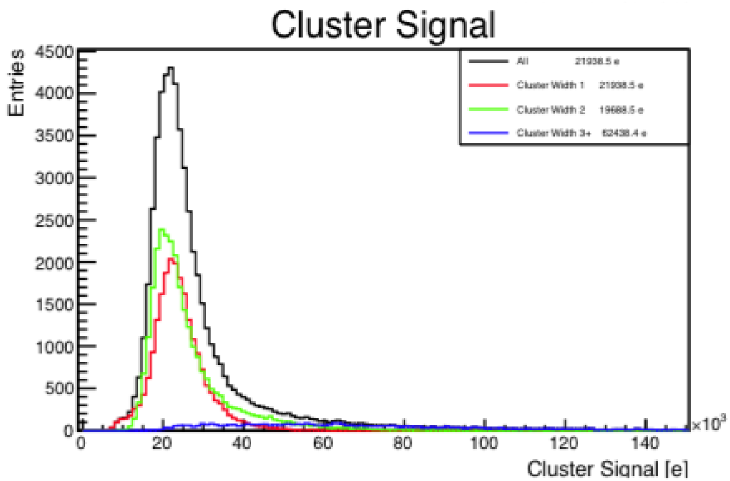


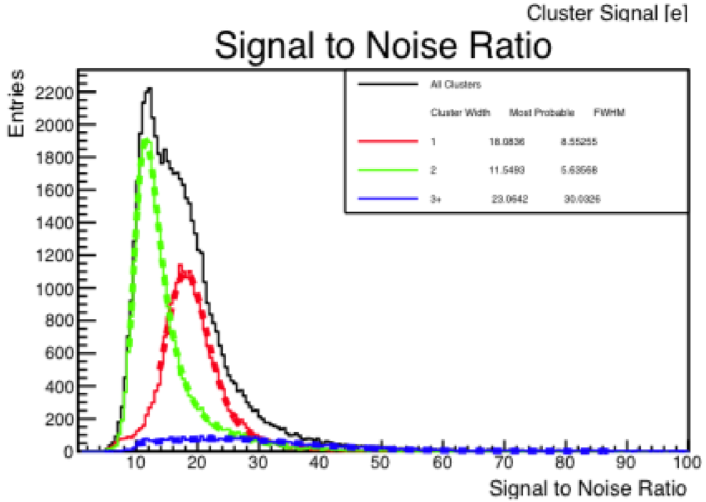
efficiency: 99.4%

SVD TEST @ CERN BEAM

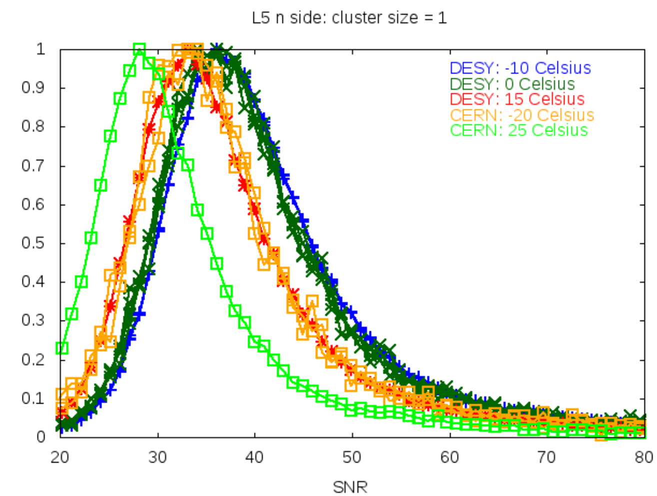
Nov 2014

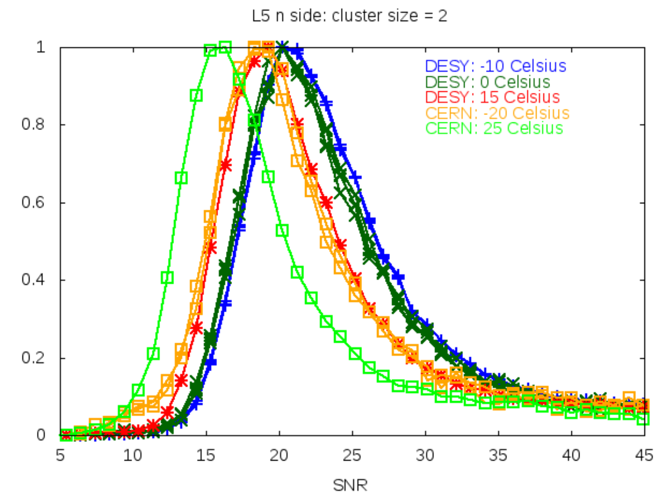
FWD/BWD module, no cooling





L5 module, with/without cooling





VXD (PXD+SVD) Schedule

Milestones	
First mass production ladder (L3-L6)	Nov 2015
2nd beam test	Jan-Feb 2016
Start of ladder mount to support structure	July 2016
SVD readiness in KEK	Feb 2017
PXD readiness in KEK	Apr 2017
PXD+SVD integration	Jun 2017
PXD+SVD combined cosmic ray test	Jun 2017
PXD+SVD installation	Apr 2018
Start of physics run	4Q 2018

Summary

- SVD is a 4 layer silicon strip detector for the Belle II experiment
  - Together with the PXD it will provide inner tracking
  - Improved track resolution at the IP and better low momentum tracking w.r.t. to the Belle I SVD
- SVD ladders
  - Assembly challenging because of the novel ‘origami chip-on-sensor’ concept
  - The prototype phase is now coming to an end, mass production will start in autumn 2015
- FADC readout
  - Prototypes of the system exist and the full readout chain has been confirmed