A Low-latency, Low-overhead Encoder for Data Transmission in the ATLAS Liquid Argon Calorimeter Trigger Upgrade

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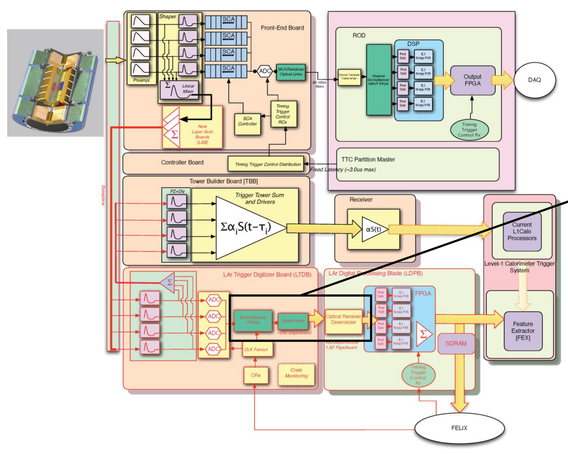
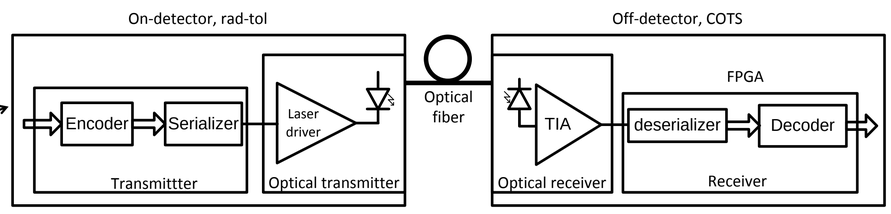
Introduction

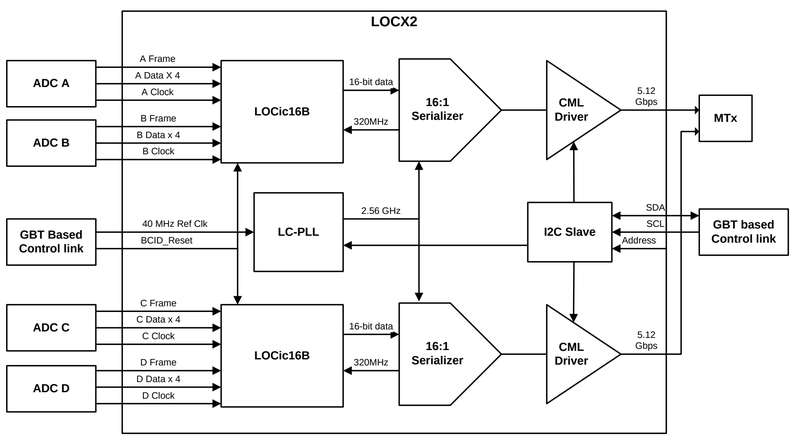




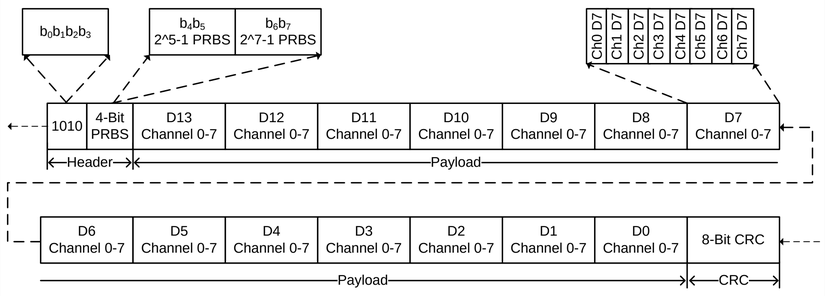
The block diagram of an optical link

- The ATLAS Liquid Argon calorimeter (LAr) Phase-I trigger upgrade calls for a data transmission rate of 204.8 Gbps for each front-end board (LTDB) [1].
- The optical link on the transmitter side consists of a transmitter ASIC LOCx2 and a custom optical transmitter module MTx.
- LOCx2 is a two-channal transmitter ASIC. Each channel receives data from the upstream ADCs [2], encodes the data, and outputs them in serial at a speed of 5.12 Gbps. The transmitter ASIC is fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology for radiation-tolerance.
- The latency budget of the optical link is 150 ns. The encoder and decoder are the major contributors of the latency of the optical links, and should be carefully designed to achieve low latency.

The design of AISC

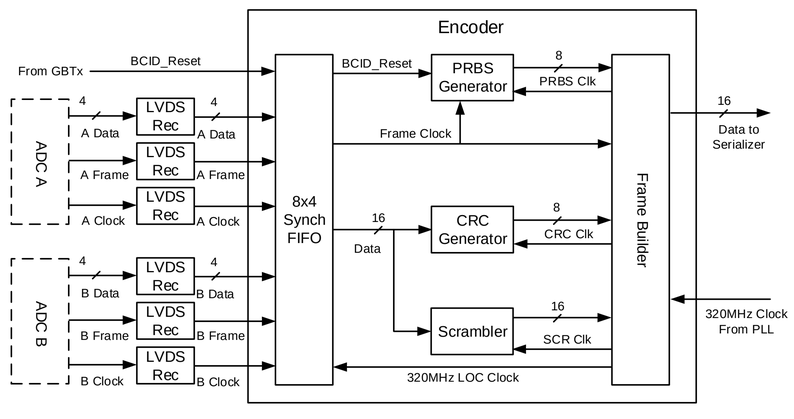


The block diagram of the ASIC LOCx2

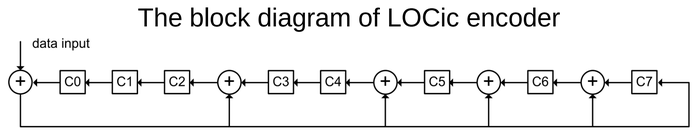


The frame definition of the ASIC LOCx2

- The ASIC uses a custom line code called LOCic [3].
- Each frame consists of 128 bits, including 8-bit frame header, 112-bit payload and 8-bit frame trailer.
- The payload is scrambled before transmitted, whereas the frame header and the frame trailer are not scrambled.
- The overhead is 14.3% (= 16/112).
- 12-bit BCID information is embedded in the frame header

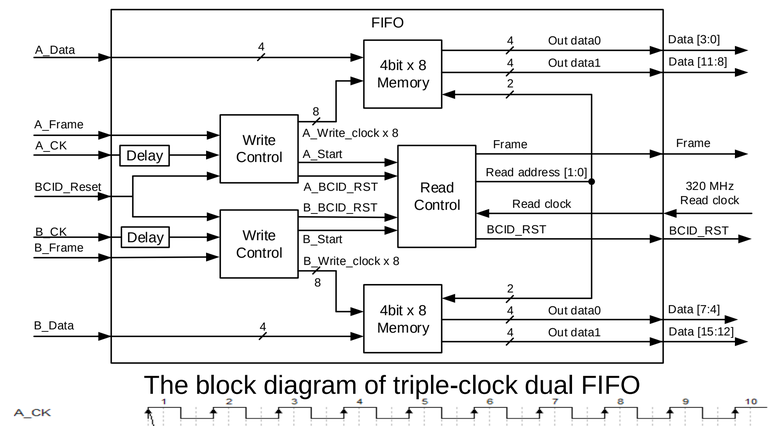


The block diagram of LOCic encoder

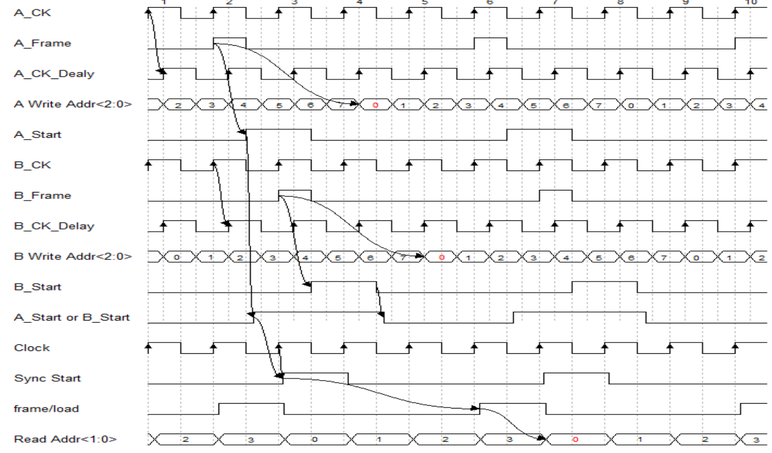


The serial processing diagram of CRC calculation

- We need to calculate 8 CRC bits from 16 input bits and 8 previous result bits.
- The parallel CRC calculation, derived from the serial processing diagram, is too complicated to be shown as a diagram.
- In the parallel CRC calculation, each output bit is the XOR operation of up to 17 input bits or previous result bits. The implementation of such a 17-input XOR gate corresponds to a chain of 5 stages of 2-input XOR gates. The simulation indicates that it is marginal for the CRC calculation to operate at 320 MHz.
- A pipeline technique is used in the design. It takes two clock cycles to calculate the 8-bit CRC results for each 16-bit input data. In each frame period, it takes one more clock cycle to calculate CRC due to the pipeline operation than to scramble. Because the CRC code is attached after the scrambled data, the pipeline technique has no latency penalty.



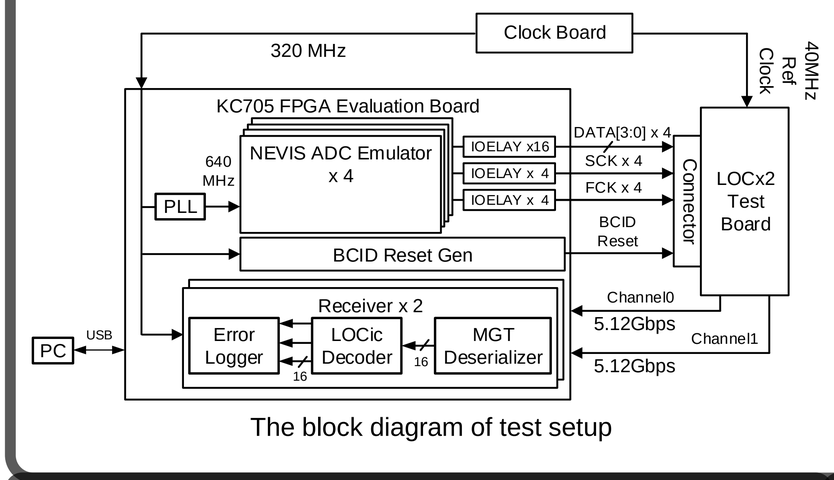
The block diagram of triple-clock dual FIFO



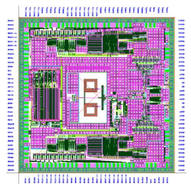
The timing diagram of FIFO Write and Read

- The FIFO is composed of two independent write controllers, one read controller, and two sets of storage cells. Storage cells are composed of static D-flip-flops. Each sets of storage cells is 8-bit deep.
- Write and read controllers are reset after each frame by input Frame signal which clears the potential errors caused by SEE.

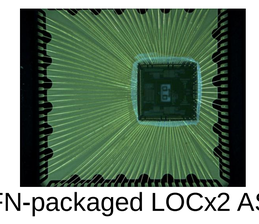
The test system and measurement results



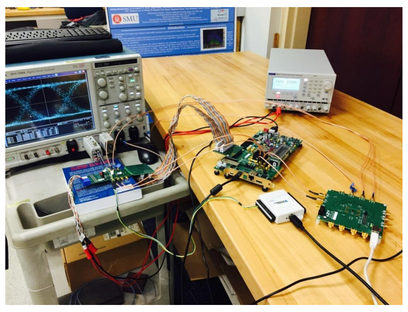
The block diagram of test setup



Layout of LOCx2



QFN-packaged LOCx2 ASIC



A picture of test setup

The power consumption of LOCic encoder is 96.3 mW, totle chips LOCx2 is 842.5 mW.

Function block			Latency (ns)
TX	LOCic Encoder	FIFO	8.4-11.6
		Scrambler & CRC gen	6.25
		Frame Builder	3.125
	Serializer		6.25
	Total LOCx2		24.0-27.2
RX	Deserializer		28.5-31.4
	LOCic Decoder	Data Extractor	9.4
		Descrambler	3.1
		CRC Check	3.1
	Total FPGA		44.1-47.0
Total optical link			68.1-74.2

Simulation

Measurement

Latency of the optical link

Conclusion and outlook

- An custom ADC data encoder ASIC for serial transmission, LOCic, is designed and tested for the ATLAS LAr Calorimeter trigger upgrade.
- The LOCic encoder features an overhead of 14.3% , a latency of less than 21 ns and a power consumption of about 96.3 mW, meeting the design goal.
- The next version will interface with both ASIC and COST ADCs.

Acknowledgments

This work is supported by US-ATLAS R&D program for the upgrade of the LHC, the US Department of Energy Grant DE-FG02-04ER1299. We are grateful to Drs. Hucheng Chen and Hao Xu of Brookhaven National Laboratory, Dr. Nicolas Dumont Dayot of LAPP and Bernard Dinkespiler of CPPM for beneficial discussion.

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[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] J. Kuppambatti, et al, A radiation-hard dual channel 4-bit pipeline for a 12-bit 40 MS/s ADC prototype with extended dynamic range for the ATLAS Liquid Argon Calorimeter readout electronics upgrade at the CERN LHC, 2013 JINST 8 P09008
[3] B. Deng, et al, *A line code with quick-resynchronization capability and low latency for the optical data links of LHC experiments*, 2014 JINST 9 P07020

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