

A low-latency and low overhead encoder ASIC for the serial data transmission in ATLAS LAr calorimeter

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The ATLAS LAr calorimeter readout phase-I trigger upgrade calls for a data rate of 204.8 Gbps for each front-end board (LTDB). These data will be transmitted over optical fibers to the back-end. The optical link transmitter side consists of an encoder, a serializer and a custom optical transmitter. The encoder receives data from the upstream ADCs and encoded the data into frames. The LOCic ASIC has been developed with a 0.25 micron Silicon-on-Sapphire CMOS technology.

The front-end ADCs are 12-bit 40 MSPS ADCs with 640 Mbps serial output. The custom data frame comprises of 112-bit scrambled ADC data, 8-bit CRC (Cyclic Redundancy Check) code and 8-bit frame header. The 8-bit frame header, used to identify the frame boundary, also provides the capability to quickly re-synchronize the frame boundary if the serial data shift a few bits due to radiation.

The LOCic comprises of a synchronous FIFO, a CRC generator, a scrambler, a header generator and a frame builder to composite the data. To reach the clock frequency of 640 MHz we adopted pipeline technique to simplify the circuit logic executed in each clock period, especially in the CRC generator with a limit of 8 XOR logic units in each step.

LOCic has been tested using a Kintex 7 FPGA evaluation board. The FPGA implemented a ADC emulator and a decoder. The decoder identifies the data frame boundary correctly and the recovered ADC data pass the CRC code check. The latency of the encoder is about 7 ns and the over

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