A High Frame Rate Pixel Chip Design for Synchrotron Radiation Applications


State Key Laboratory of Particle Detection and Electronics
Institute of High Energy Physics, Chinese Academy of Sciences

10th Hiroshima Symposium, 2015-09-29
Outline

• Background
• The readout chip design
  – Pixel Cell Unit
  – The overall design
• The measurement results
  – Measurement results for the readout chip
  – Beam test with sensor bump-bonded
• Related topics
  – Preliminary design of the module
• Conclusion
Silicon Pixel Detector R&D for HEPS

• One of the R&Ds in HEPS (High Energy Photon Source, the next generation of photon source in China)
• Focusing on synchrotron radiation applications: SAXS, Macro Molecule...
• The pixel cell works in single photon counting mode, readout by frame refreshing.
• A hybrid pixel system:
  – Si-P in N Sensor + Bump Bonding + ASIC
• Project specification
  – Area: 8cm × 8cm
  – Pixel size: 150μm × 150μm
  – Frame rate: 1kHz
  – Dynamic range: 20bit
  – Energy range: 8~20keV
Silicon Pixel Detector R&D for HEPS

- Localization of design:
  - Sensor: co-design and measurement
  - Self-designed ASIC readout chip
  - Self-designed backend electronics and DAQ system
  - Bump Bonding: co-design and evaluation
  - Self-designed mechanical supporting system

- ASIC design specification

<table>
<thead>
<tr>
<th>Pixel Cell Size</th>
<th>150μm × 150μm</th>
<th>Frame rate</th>
<th>100~1kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel array</td>
<td>72col × 104row</td>
<td>Energy range</td>
<td>8keV~20keV</td>
</tr>
<tr>
<td>Operation mode</td>
<td>Counting</td>
<td>Counting depth</td>
<td>20bit</td>
</tr>
<tr>
<td>ENC</td>
<td>&lt;200e</td>
<td>Thres. Dispersion</td>
<td>&lt;200e</td>
</tr>
<tr>
<td>Estimate power</td>
<td>&lt;50μW/pixel</td>
<td>Total power diss.</td>
<td>400mW</td>
</tr>
</tbody>
</table>
Milestones of the Project

- **2012.5**
  - Single pixel tested
  - Chip test
  - 4×4 pixel array

- **2014.4**
  - 24×20 pixel array
  - Wire-bond with Sensor

- **2014.8**
  - 72×104 full size chip engineering tapeout
  - ATE selection

- **2015.1**
  - Faultless chip

- **2015.3**
  - Single-chip Module
  - Beam test

- **2015.11**
  - Full size Module

- **2012.8**
  - Chip test
  - 72×104 full size evaluation chip engineering tapeout

- **2013.9**
  - Faultless chip
  - ATE Selection
  - Bump-bonding
  - Flip-Chip samples

- **2014.3**
  - Test & Evaluation
  - High yield bump-bonding process
  - Small size sensor sample
  - Wire-bond with ASIC
  - Full size sensor trial-manufacture

- **2014.8**
  - Multi-chip bump-bonding samples

- **2014.12**
  - Mechanics and detector trial-manufacture

- **Now**
Pixel ASIC Design—— Pixel Cell

- Based on CSA and discrimination, a “zero-noise” detection can be achieved.
- Much higher S/N ratio can be got compared with conventional “3T” charge integration readout, e.g. MAPS, CCD
- Frame rate greatly increased from ~Hz to ~kHz thanks to pixel level discrimination and digitization
- Hybrid detector: Sensor and ASIC can be separately upgraded, more complicated functions can be integrated in ASIC

- Process: SMIC 0.13μm, 1P8M, Mixed Signal
Overview of the ASIC and Prototype System

- **Pixel Readout Chip:**
  - Pixel Array: $104 \times 72$ cells
  - Single Chip area: $1.7 \text{cm} \times 1.1 \text{cm}$
  - Periphery: Bias generation, monitoring, readout driver, and IO logic

- **Single Module:**
  - $4 \times 2$ Pixel-Readout-Chips bump bond with a large Si-P in N sensor
  - Single module area: $4.5 \text{cm} \times 3.6 \text{cm}$

- **Prototype system:**
  - $2 \times 3$ module
  - Total area: $9 \text{cm} \times 10.8 \text{cm}$
Readout Chip Design – Simulation

- **Simulation input:** 0~6ke⁻
  - Input energy: 0~20keV
- **Peak linearity:**
  - @CSA output: 1%
  - @Shaper output: 2%
- **Dynamic range:** up to 100keV
- **ToT characteristics at discriminator output**
  - For future applications
- **ENC (@Cd=200fF)**
  - @CSA: 119.5e⁻
  - @Shaper: 117.9e⁻
- **S/N ratio @8keV **≈ 16.9
- **Noise slope:** 93e⁻ + 225.8e⁻/pF

**Process:** SMIC 0.13μm 1P8M, VDD=1.2V

**Power dissipation:** 18.9μW/Pixel for analog, 20μW/Pixel for digital
  - Full chip will be less than 400mW
Outline

• Background

• The readout chip design
  – Pixel Cell Unit
  – The overall design

• The measurement results
  – Measurement results for the readout chip
  – Beam test with sensor bump-bonded

• Related topics
  – The status of the bump-bonding
  – Preliminary design of the module

• Conclusion
Bare die test for engineering tapeout

Due to the wafer level process of bump bonding, chip can only be tested before the process.

For high yield, all chips on all wafers were tested by ATE. Defectless chips were selected and mapped.

ATE test procedure was formulated, and wafers were tested by a company.
Measurement of the chip – noise and uniformity

- All measurements were done at 20MHz clock
  - Frame rate can be guaranteed to be 1.2kHz
- Noise and threshold of all pixels were measured by S-curves method, and the thresholds distribution were flattened by calibration
- Equivalent input noise is $93.9\mu V \pm 11.6\mu V$
  - For all wafers: ENC<$120\mu V$
- Threshold non-uniformity:
  - Before Calibration: $252.5\mu V$; after: $21.5\mu V$
  - For all wafers <$60\mu V$
- No crosstalk between analog-digital and pixel-pixel were found
Measurement of the chip – yield

- Each 8-inch wafer produces 134 chips, 1~9 classes were assigned according to the bare die test:
  - Bin 1: chips with no defects
  - Bin 6: dead/noisy pixels < 0.1% (8 Pixels)

- Only Bin 1 chips were selected for bump bonding currently, Bin 6 is also in acceptable level.

- Yield of all wafers ranges in 47%~68%
  - The larger chips and more complicated functionality, the more defects and lower yield

- Wafer 2 (worst)
  BIN=1&6: 47%
  BIN=1: 45.5%

- Wafer 3
  BIN=1&6: 56.7%
  BIN=1: 55.97%

- Wafer 5
  BIN=1&6: 67.9%
  BIN=1: 67.9%
Outline

• Background
• The readout chip design
  – Pixel Cell Unit
  – The overall design
• The measurement results
  – Measurement results for the readout chip
  – Beam test with sensor bump-bonded
• Related topics
  – Preliminary design of the module
• Conclusion
Chip Measurement and Readout System

• Test System I: for MPW Chip
  – CPLD on motherboard + MPW chip on daughterboard
  – Altera DE2 development board + USB → PC

• Test System II: full size single chip
  – NI Single board-RIO 9626 + chip on daughterboard
  – Online control and calibration by LabVIEW

Test System I - CUT and Motherboard

Test System II
Noise and uniformity with sensor bonded

- Calibration was extracted from S-curves in the similar scheme
- Energy scale to calibration input amplitude was measured by well-defined energy, e.g., beam energy
- It is measured $100\text{mV} \leftrightarrow 353.1e^-$ (before bonding: $100\text{mV} \leftrightarrow 1\text{ke}^-$)
  - ENC after bonding: $115.8e^-$
  - Threshold uniformity after calibration: $55.1e^-$
Sensor and ASIC Co-test Scheme

MPW chip wire-bonded with sensor for co-test

Sensor+Bump Bonding + full size ASIC

Tested with $^{55}$Fe source

Test and setup at X-ray tube
Counting accuracy, vs HV

- Counts per frame VS current of the X-ray tube was measured
  - All pixels show good linearity vs current, but some multi-hits might affect the linearity at high current

- Frame period (8.32ms~2.13s) was extended by 2-div of the clock
  - cnts-per-frame found to be linear in semilog plot
  - Up to 17bits of the counter was working normally

- Full-depleted voltage were measured by the curve of counts vs HV, showing the full-depleted point is around 55V
X-ray imaging @ X-ray tube

- A laser carved workpiece,
  - line width: 250/300/350μm
- Standard SOP8 package
  - Different materials can be seen at different energy: 8kV for plastic and 15kV for bond frame
- The imaging of the resolution test card shows the spatial resolution
  - 3.55/4.0 line pair (145/125μm pitch slims)
Beam test environment @BSRF 1W2B beamline

- Sensor and ASIC were co-tested by wire-bonding (for MPW chip) and bump-bonding (for full size chip) respectively.
- Laser pen, $^{55}$Fe source, X-ray tube, beam light are used as radiation source successively.
S-curve VS energy at beamline

- S-curves were first measured and then normalized, systematic noise and energy threshold were then extracted.
- Energy range: 6keV~19.5keV
  - The full range of BSRF 1W2B
- The fitted curve of global threshold vs energy shows $\pm 2\%$ of the energy linearity
  - Closely meets the simulation, peak amplitude results
  - The energy scale corresponding to the calibration input amplitude is also defined by the fitted curve.

Counts normalized S-curve vs energy

Fitted global DAC Code vs energy

Residual of global DAC vs energy
Measurement of the chip – waveform, linearity and power

Shaper and discriminator single photon output @8keV BSRF

Peak amplitude @shaper output vs calibration input and linearity

- Sensor+ASIC system observed single photon response at both $^{55}$Fe source and synchrotron beam light
- Measured linearity at preamp and shaper are 1% and 2%, respectively
- Tested power dissipation of all chip by ATE is $274.8\text{mW} \pm 17.8\text{mW}$ ($36.6\mu\text{W/Px}$):
  - Analog Power: $158.5\text{mW} \pm 13.0\text{mW}$, as $21\mu\text{W/Px}$
  - Digital Power: $116.3\text{mW} \pm 13.8\text{mW}@20\text{MHz Clk}$, as $15.5\mu\text{W/Px}@1.2\text{kHz Frame Rate}$
- All measured waveform and performance are closely matched with simulation
Light spot of the beam – counting rate

- Light spot of the beam light was observed
- For a nearly go-through beam light, saturation was found in center, the max counting rate (seen as a red ring) is 3.53MHz/Px – can be thought as the saturation rate
- After attenuator, no obvious saturation, max rate 3.48MHz
- The counting rate at outskirts is 1MHz, obviously not saturated, is the normal counting rate
  - 1MHz/Px = $2^{20}$ cnts/s, for the counting dynamic range
  - For area, the counting rate is 4GHz/cm²
- More strict measurement was done for saturation rate, by linearly increased the layer of Al foil attenuator
High frame rate imaging @ beamline

- A frame rate of 1.2kHz is guaranteed by the system clock of 20MHz
  - As clk freq. can be higher, the frame rate can increase
- The fast frame imaging is shown by a rolling fan with 4 leaves, stopping the beam before the module
  - Its rolling freq is 50Hz from the manual, a 6-phase period was measured in the movie (for each leaf), thus 1.2kHz frame rate is proved
- A slow period (~2s) pendulum stopper was also imaged to show the fast frame imaging
- More strict test was done by injecting an AM-modulated triangle waveform for calibration
A diffraction ring of a standard sample was got at the BSRF 1W2A beamline.

By scanning along the diffraction ring, a panoramic view was extracted from the series images:

- Frame rate when scanning is 120Hz
- 10 sequent images were selected for full view, all are raw data (no multi-image integration)
- The size of the panoramic view is 360*104 pixels, 5.4cm*1.56cm
## Performance conclusion

<table>
<thead>
<tr>
<th>Specs</th>
<th>This work</th>
<th>Specs</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>150μm × 150μm</td>
<td>Energy range</td>
<td>5.9~19.5keV (test limit by beam line)</td>
</tr>
<tr>
<td>Pixel array</td>
<td>72 × 104</td>
<td>Noise</td>
<td>93.9e⁻ ± 11.6e⁻ unbond 115.8e⁻ bump bonded</td>
</tr>
<tr>
<td>Frame rate</td>
<td>&gt; 1.2kHz</td>
<td>Uniformity</td>
<td>&lt; 60e⁻ after calibration</td>
</tr>
<tr>
<td>System clk</td>
<td>20MHz</td>
<td>Power dissipation</td>
<td>274.8mW ± 17.8mW (36.6μW/Px)</td>
</tr>
<tr>
<td>Deadtime</td>
<td>175ns/fr@20MHz</td>
<td>Counting depth</td>
<td>20bit</td>
</tr>
<tr>
<td>Counting rate</td>
<td>&gt; 1MHz/Pixel</td>
<td>Saturation rate</td>
<td>~3.5MHz/Pixel</td>
</tr>
</tbody>
</table>
Outline

• Background
• The readout chip design
  – Pixel Cell Unit
  – The overall design
• The measurement results
  – Measurement results for the readout chip
  – Beam test with sensor bump-bonded
• Related topics
  – Preliminary design of the module
• Conclusion
Readout PCB and module conceptual design

- The multiple chip bump bonding process is nearly settled down
- Readout PCB is under design now
  - FE-supporting board
  - Data readout board
- Prototype system: $2 \times 3$ module
  - FE: water cooling + Al supporting
  - Backend: N$_2$ cooling
  - Estimate Power: 20W

A full size (4.5cm*3.6cm, 1Sensor+8ASIC) tech-research module is under wire bonding
Conclusion

• The module with a single ASIC bump bonded with a single size sensor was fully tested
  – All functionality is normal, all measured performance meets the specification of the project
  – The ASIC design is taped out by engineering run, test results prove that it can be the final version

• All techniques are localized in China

• The pixel detector R&D of HEPS is approaching the final step
  – The trial-manufacture for the multiple-chip module is done
  – Readout electronic system is under design
  – The first prototype of the mechanic skeleton is received
Thank you!