

A High Frame Rate Pixel Chip Design for Synchrotron Radiation Applications

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A hybrid pixel detector working in the single photon counting mode was designed for the High Energy Photon Source (HEPS) in China. Aiming for diffraction and protein crystallography applications, the pixel readout chip works in single photon counting mode in each pixel. It contains an array of 104×72 pixels with a pixel size of $150\mu\text{m} \times 150\mu\text{m}$, each owning a counting depth of 20bit. Different from the conventional readout structure based on linear feedback shift register chain, an independent shift register chain was inserted, separated with the counter. Then a 20MHz readout clock can simply increased the frame rate up to 1kHz. By reusing this chain to refresh the configuration data at the same time while data is being readout, the conventional triple-redundancy latches can also be eliminated concerning the SEU events. The measurement showed 118e-equivalent noise after bump bonding and non-uniformity less than 55e- after threshold equalization. All functionalities were proved to be normal at a frame rate of 1.2kHz with a dead-time less than 175ns/frame, which are greatly improved compared with the existing pixel system.

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