Performance of Edgeless Silicon Pixel Sensors on p-type substrate for the ATLAS High-Luminosity Upgrade

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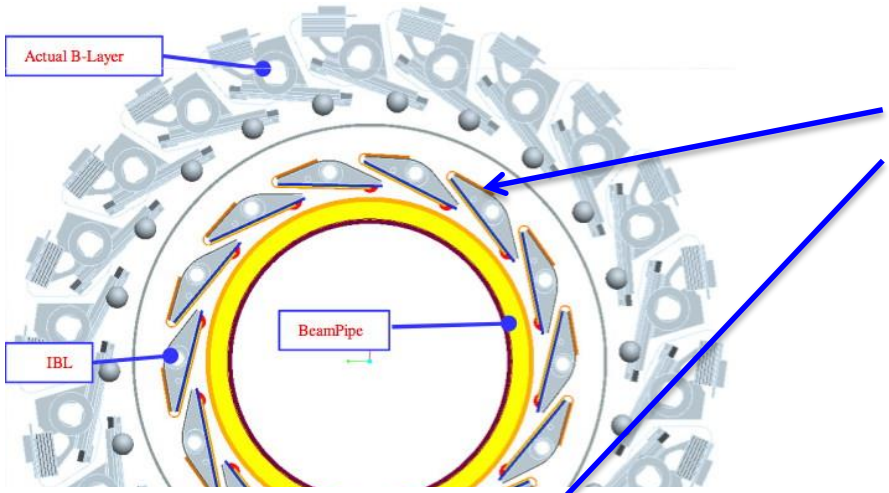
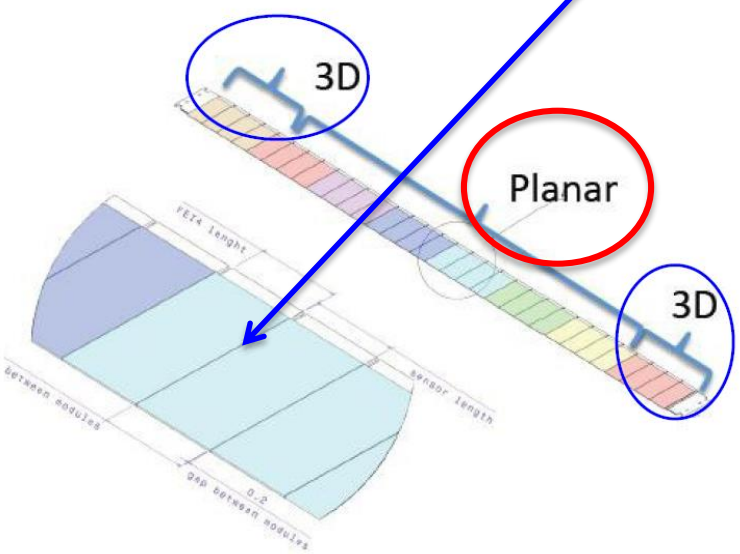
Edgeless or active edge pixel sensors are critical in configurations such as innermost layers or tiled modules, where not enough space (or too much complicated) to design an overlap

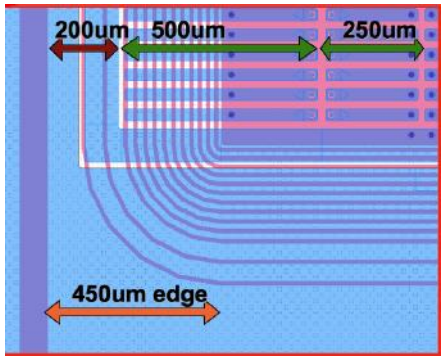


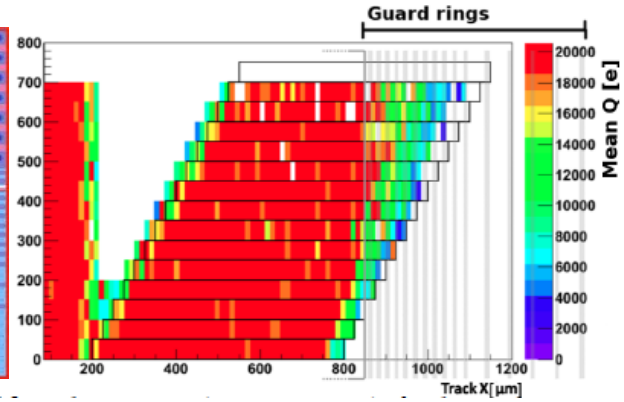


Example: ATLAS IBL overlap in phi but not along z

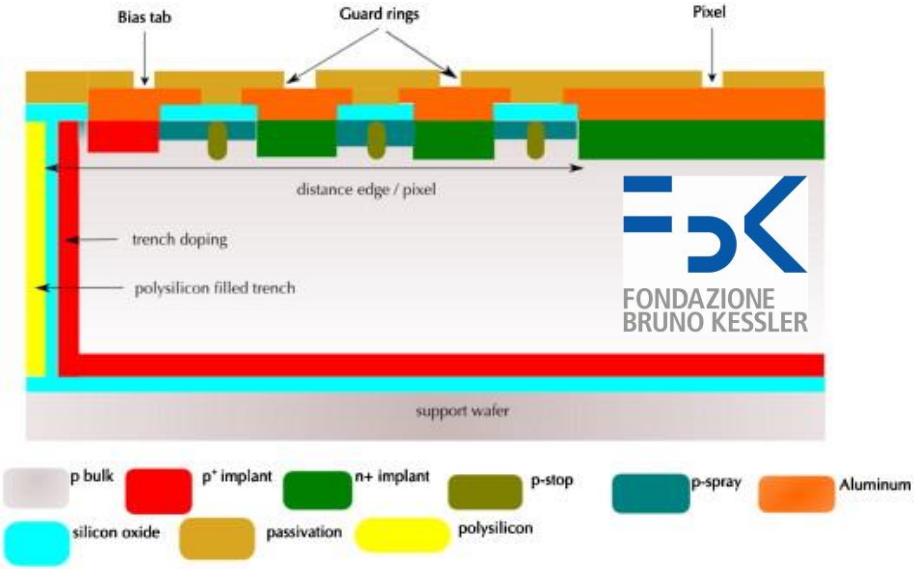
Just as a factoid:
in original ATLAS pixels, guard ring region is 1.1 mm wide!

In the ATLAS IBL (n-in-n) the guard-ring region reduced to 450um and pixels pushed below GRs to recover efficiency

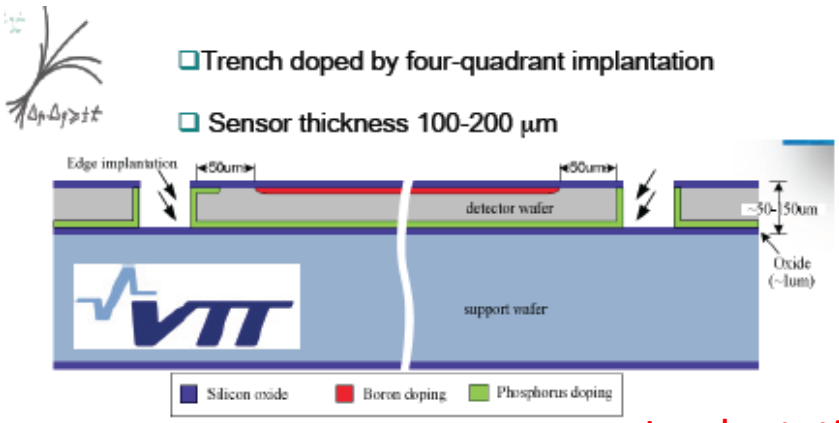




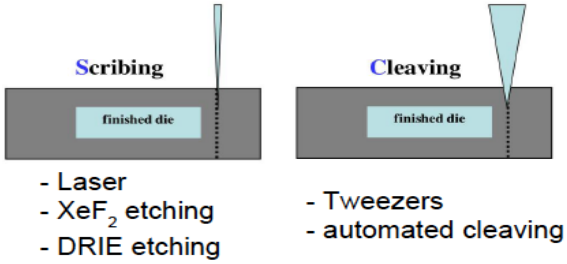
Many techniques developed in the years to extend the efficient region to the sensor edge

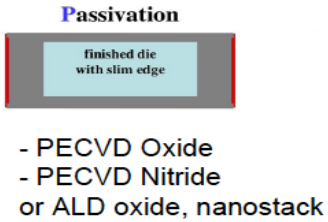


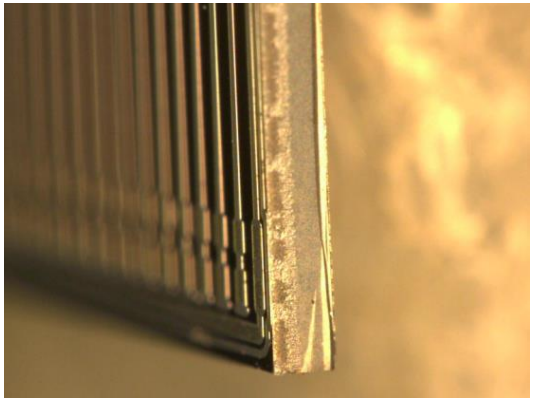
Diffusion
FBK



Implantation
VTT

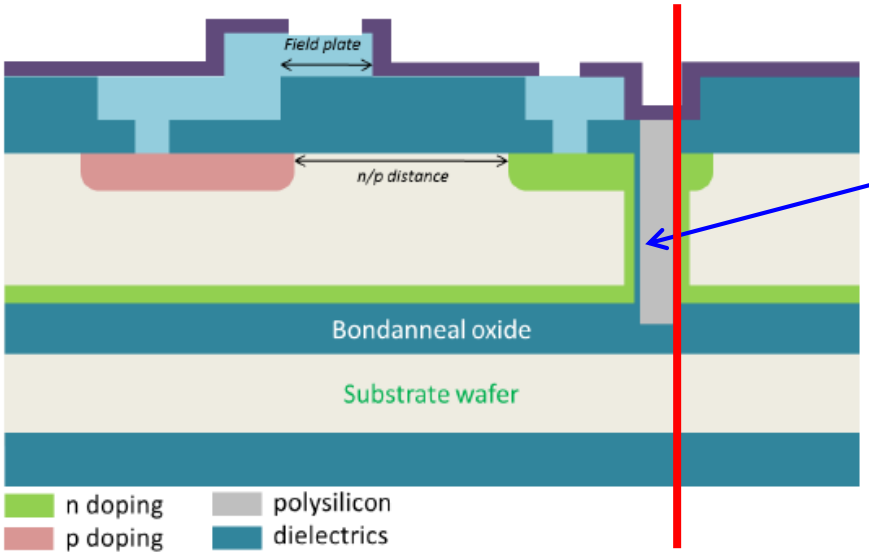






Scribe-Cleave-Passivate
NRL + SCIPP (UCSC)

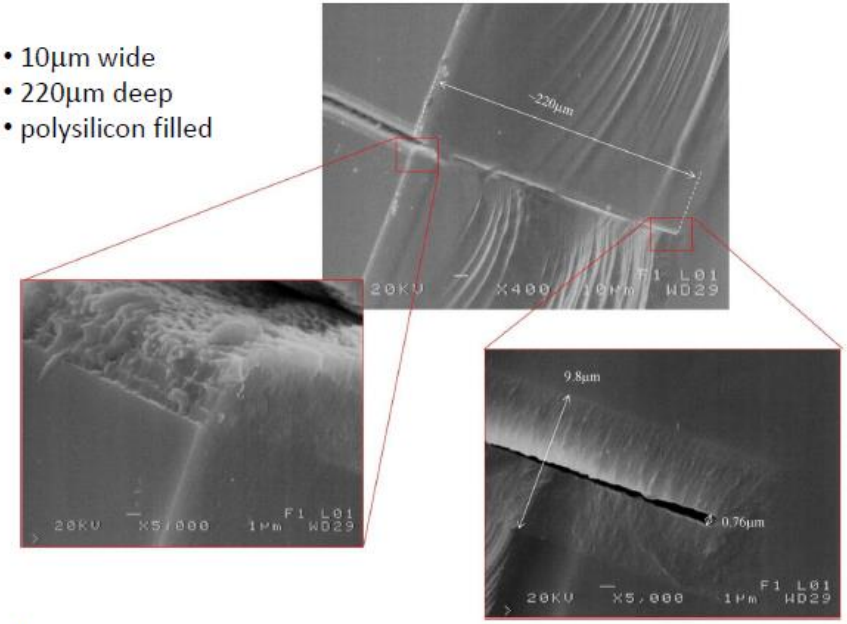
FBK/LPNHE productions: n-in-p active edge pixel sensors

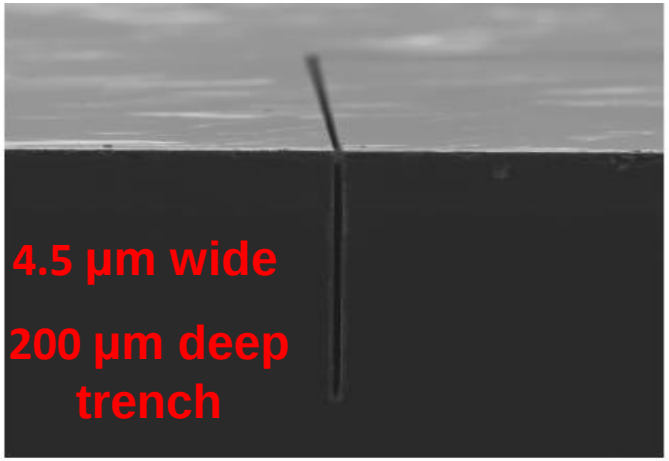


Deep trench diffusion (to prevent electrical field on the damaged cut)

Cut line

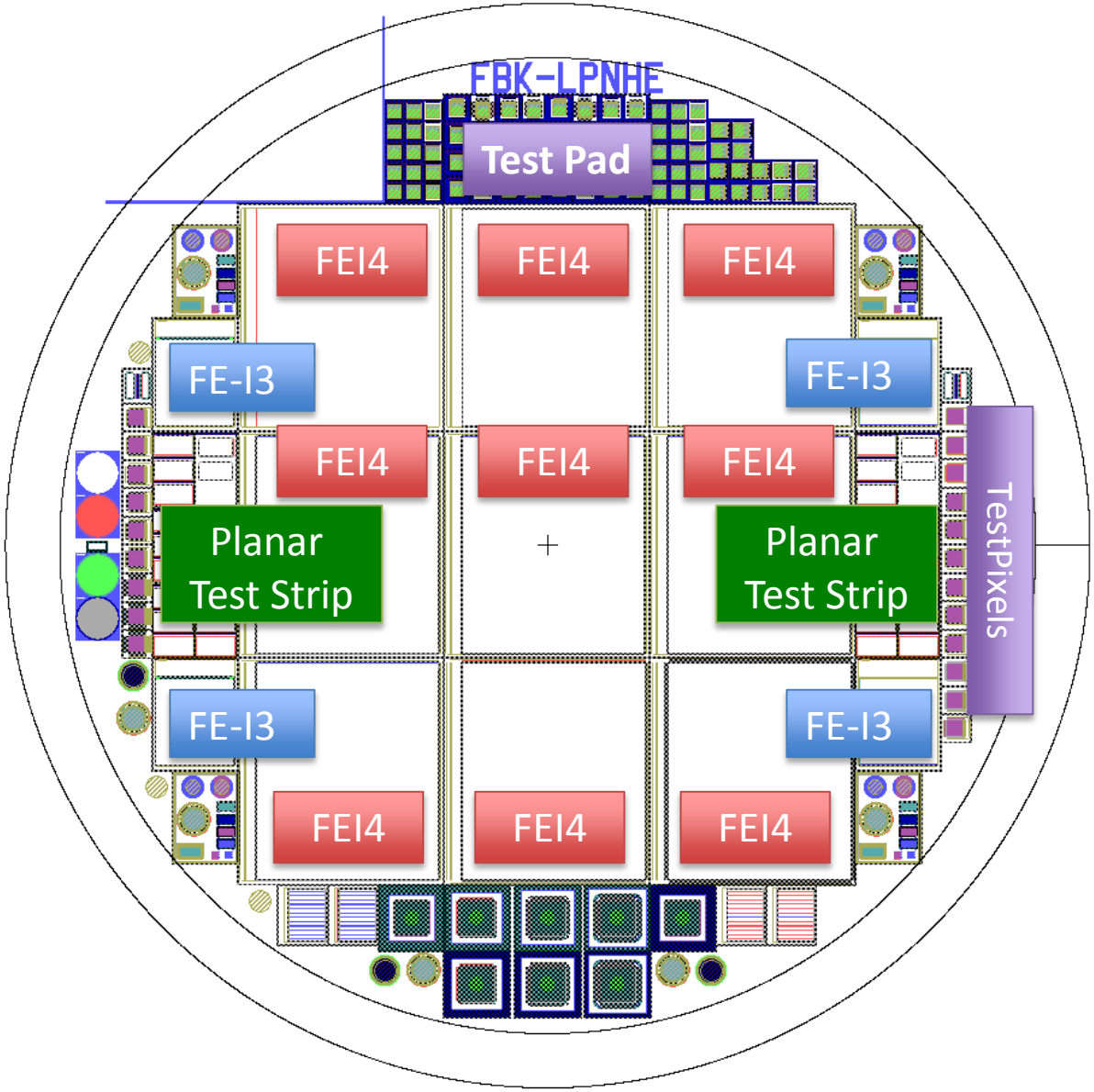
- 10µm wide
- 220µm deep
- polysilicon filled





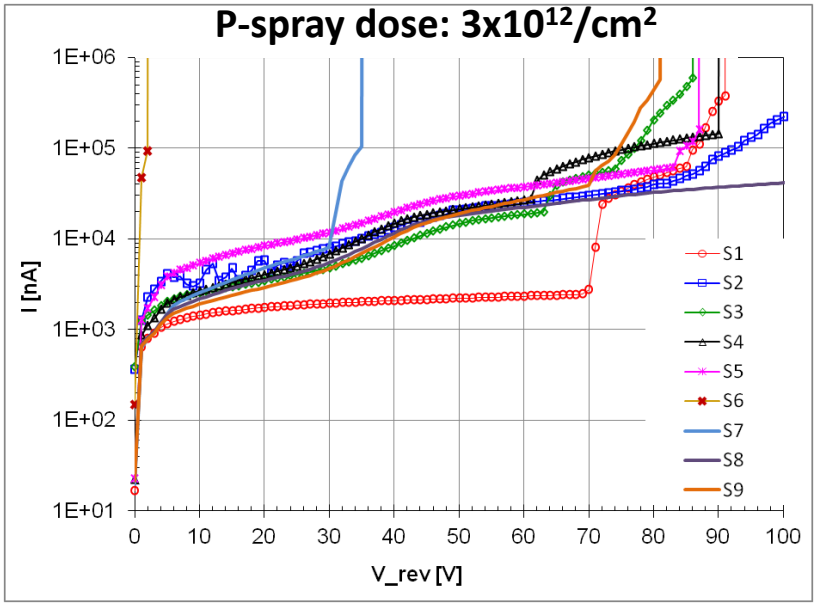
Uniformity of trench filling is critical.

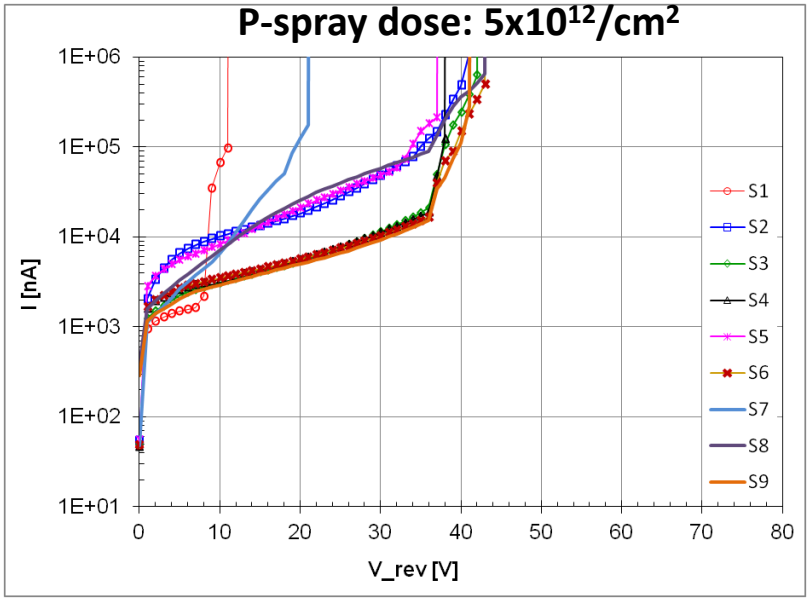
First active edge production we did with FBK dates back to 2013

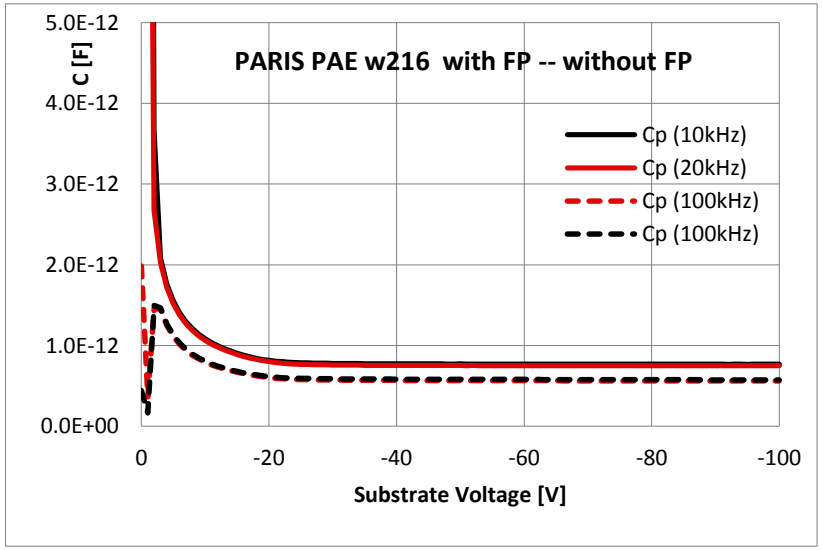


- 9 FE-I4 type Sensors (50µmx250µm Pixels)
  - 0, 1, 2, 3, 5, 10 GRs
  - Different n^+→trench distances
- 4 FE-I3 Sensors(50µmx400µm Pixels)
  - 1 or 2 GRs
- TestPixels/Pad
  - 0, 1, 2, 3, 5, 10 GRs
  - Different n^+→trench distances
- DC Strip Sensors

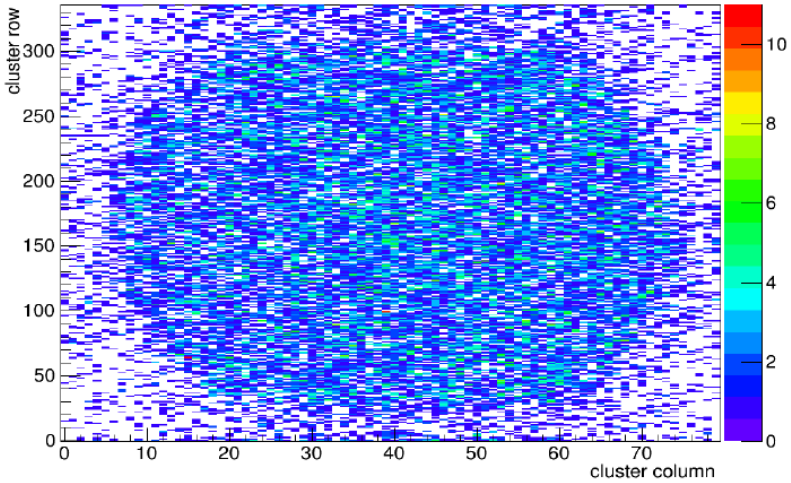
Electrical characterization







Bump-bonded to FE-I4 at IZM (Sr90)

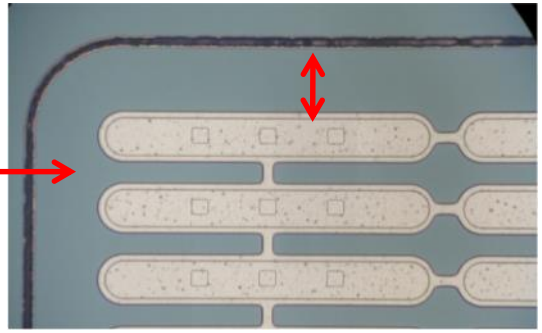


Tested on beam (I): DESY

(4 GeV electrons)

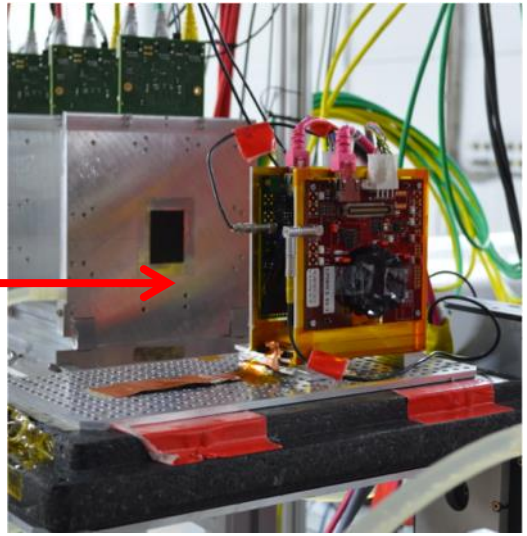
Example: LPNHE5, featuring 100 µm pixel-to-trench distance and no GRs

2 more modules available; not enough beam-time to measure them



Configurations tested

# Events	V_{bias}	Seuil	angle
2M	-30 V	2000 e	0
2M	-40 V	2000 e	0
2M	-40 V	1600 e	0
4M	-40 V	1600 e	15



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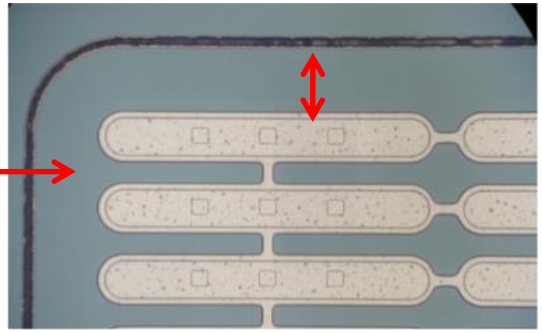

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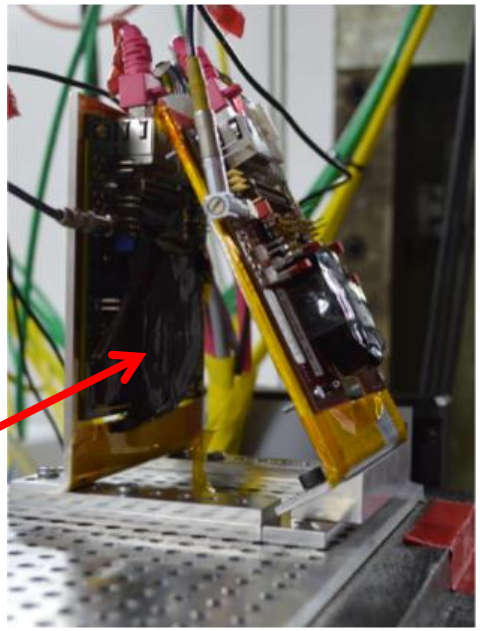
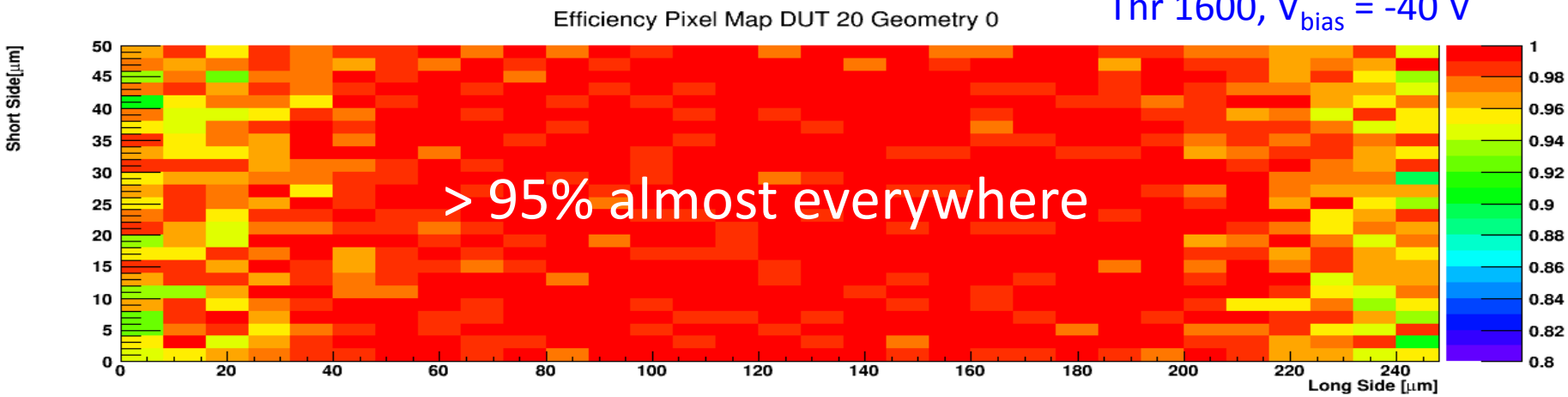
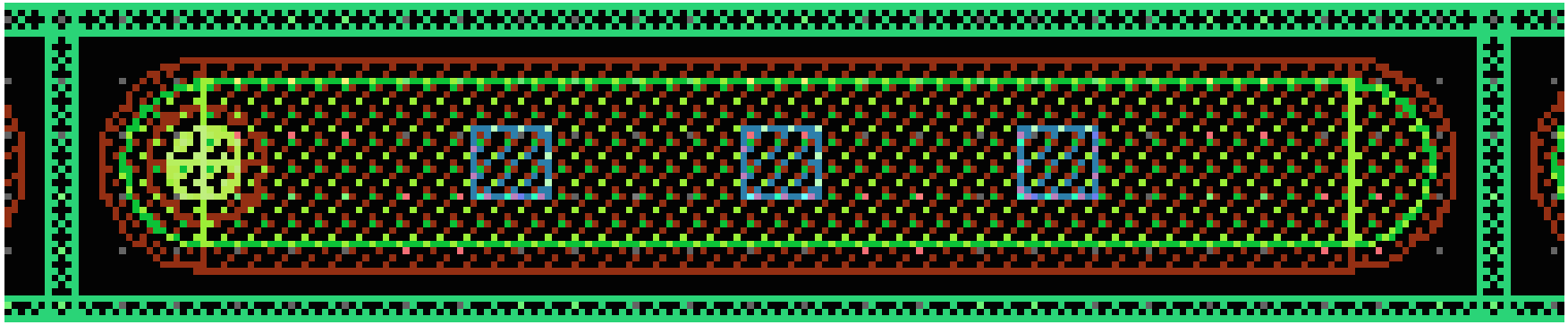


In-pixel efficiency

- Analysis limited by multiple scattering

Thr 1600, V_{bias} = -40 V

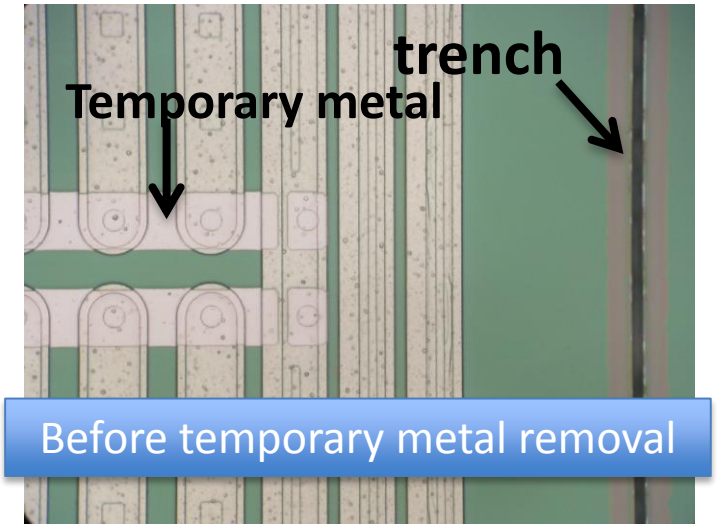




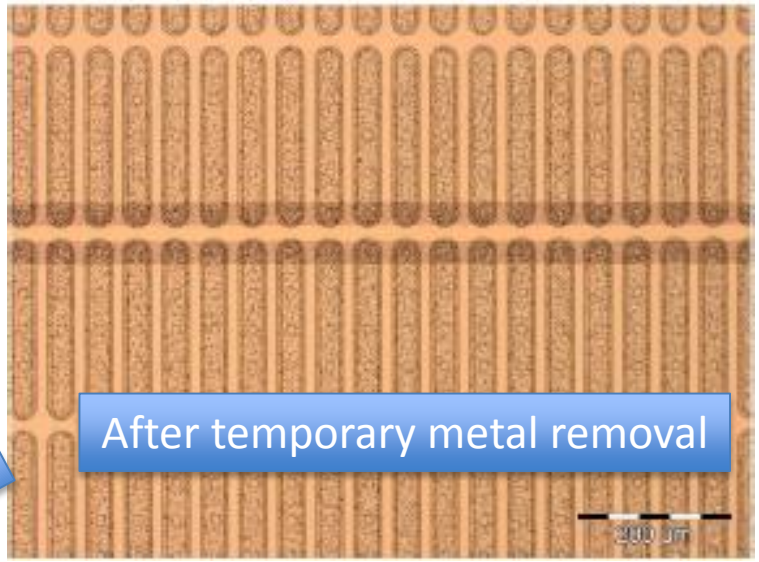
No inefficiency due to bias rail (temporary metal, see next slide)

Some inefficiency due to charge sharing

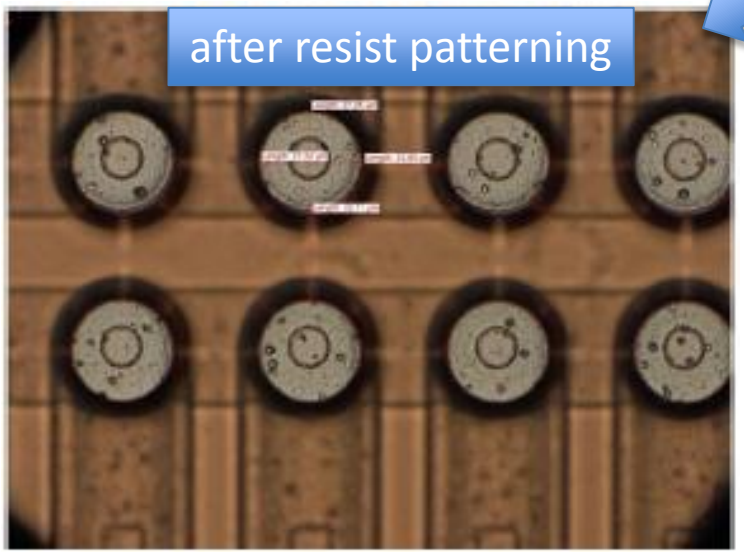
Temporary metal at FBK



Before temporary metal removal



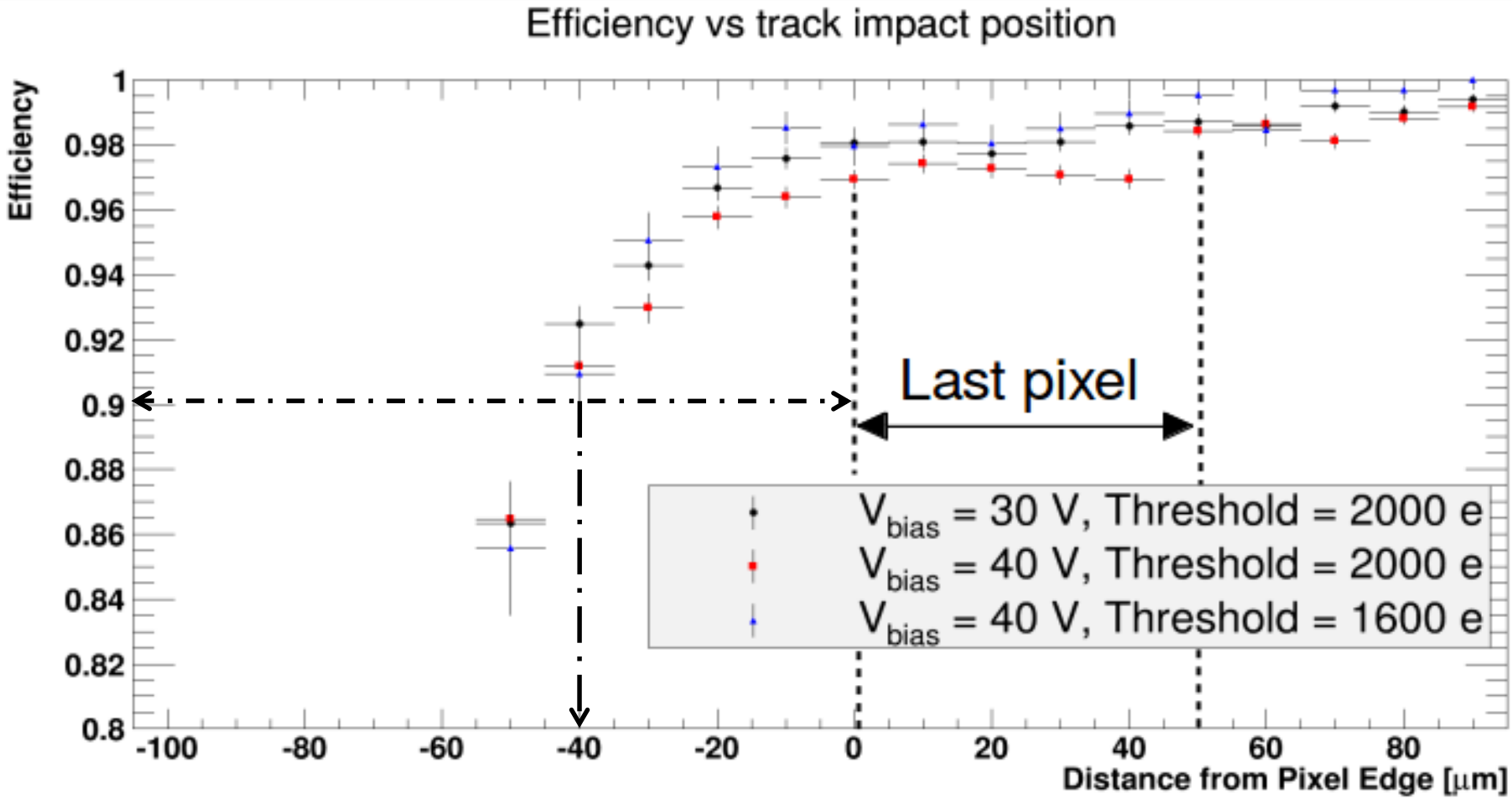
After temporary metal removal



after resist patterning

Technical solution allowing to remove the metal grid used to bias pixels during tests. After the metal removal, no inefficiency left due to bias network

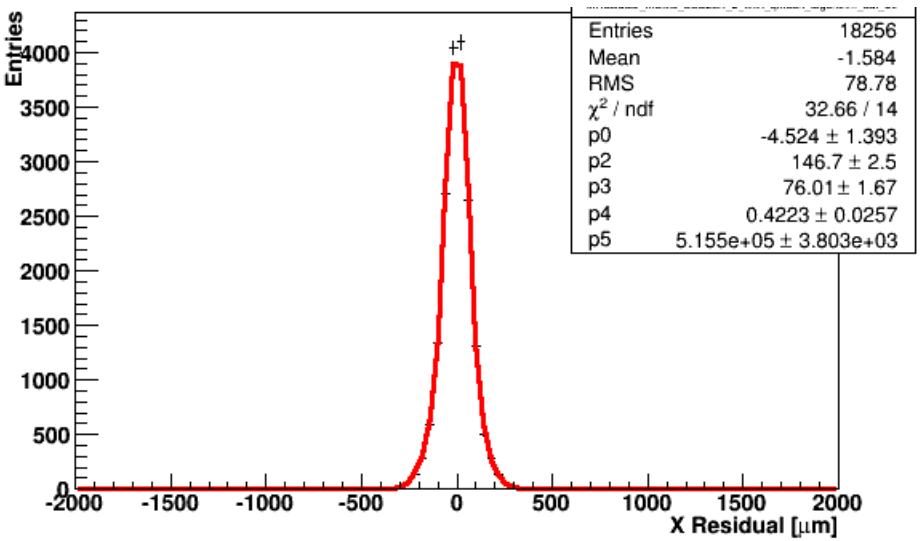
Hit-efficiency at the edge

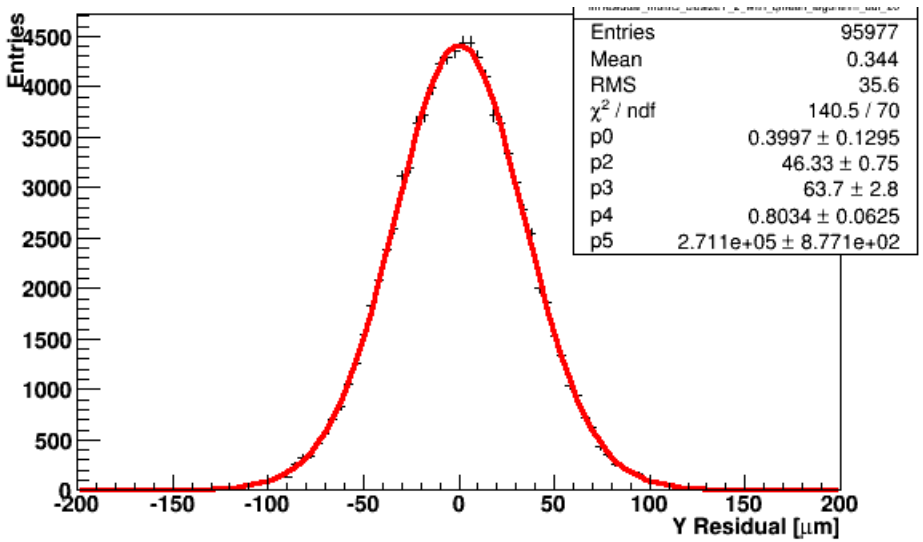


- Hit-efficiency above 90% up to 40 µm outside the last pixel
- No good tracks beyond -50 µm ➔ this is also due to track quality cuts in testbeam reconstruction

Space resolution

- Analysis limited by the multiple scattering: ϑ_{MS} ~ 30 μm



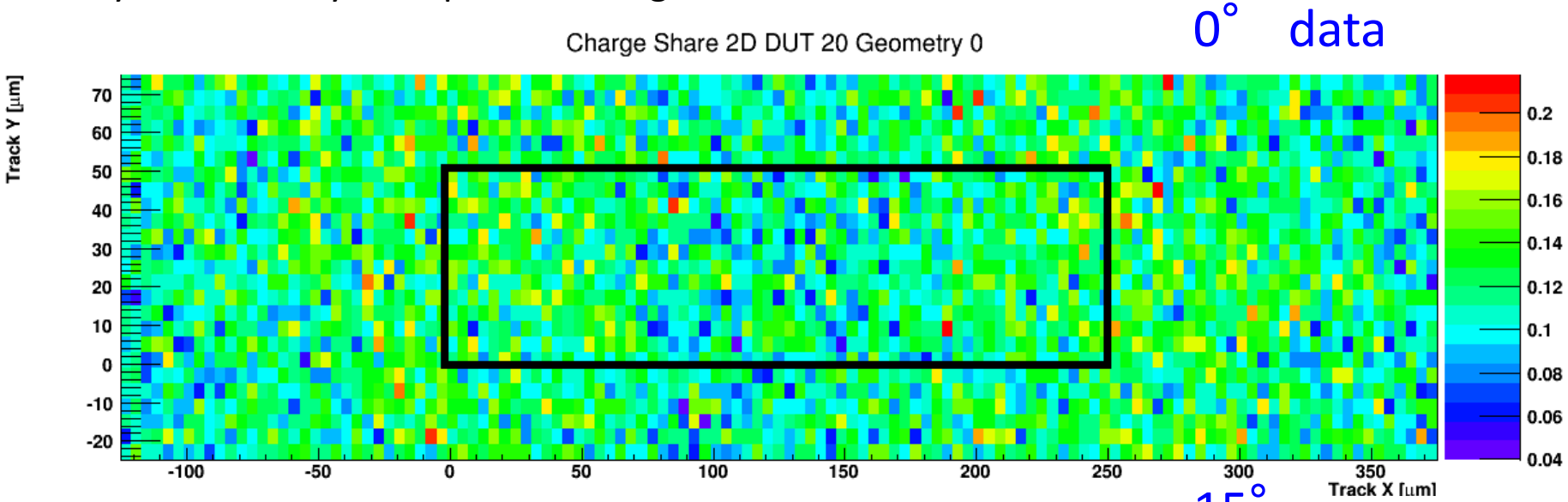


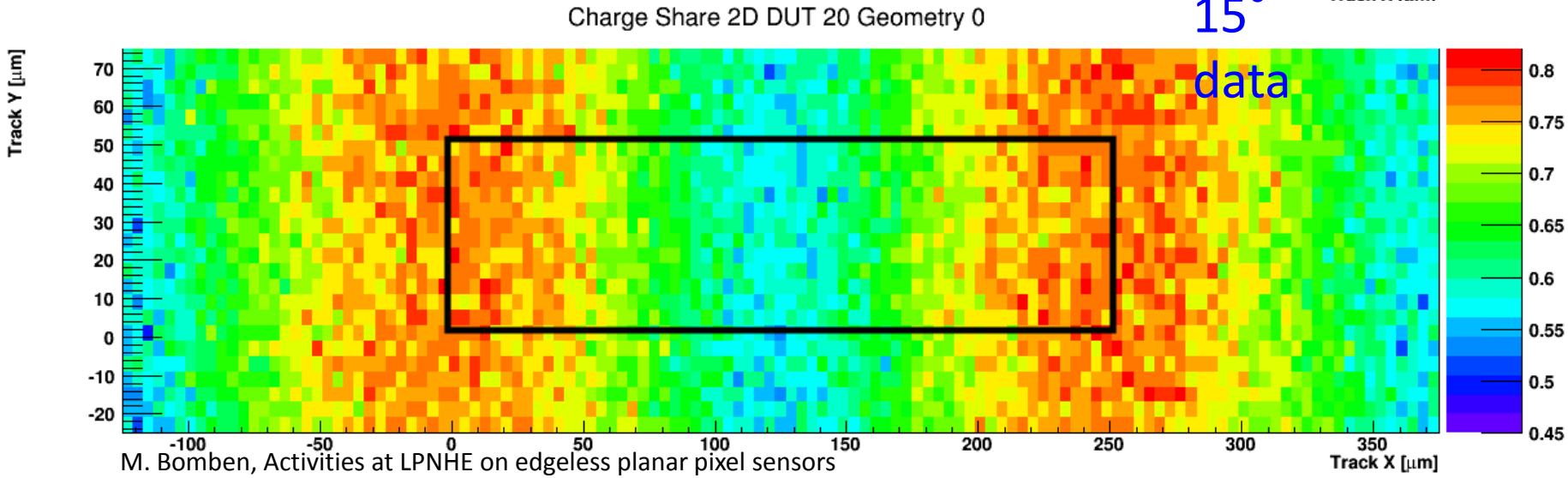
- X: RMS ~ 80 μm; pitch/√12 ~ 72 μm
- Y: RMS ~ 34 μm; pitch/√12 ~ 14 μm

➢ Results consistent with expectations

Charge sharing

- Analysis limited by multiple scattering

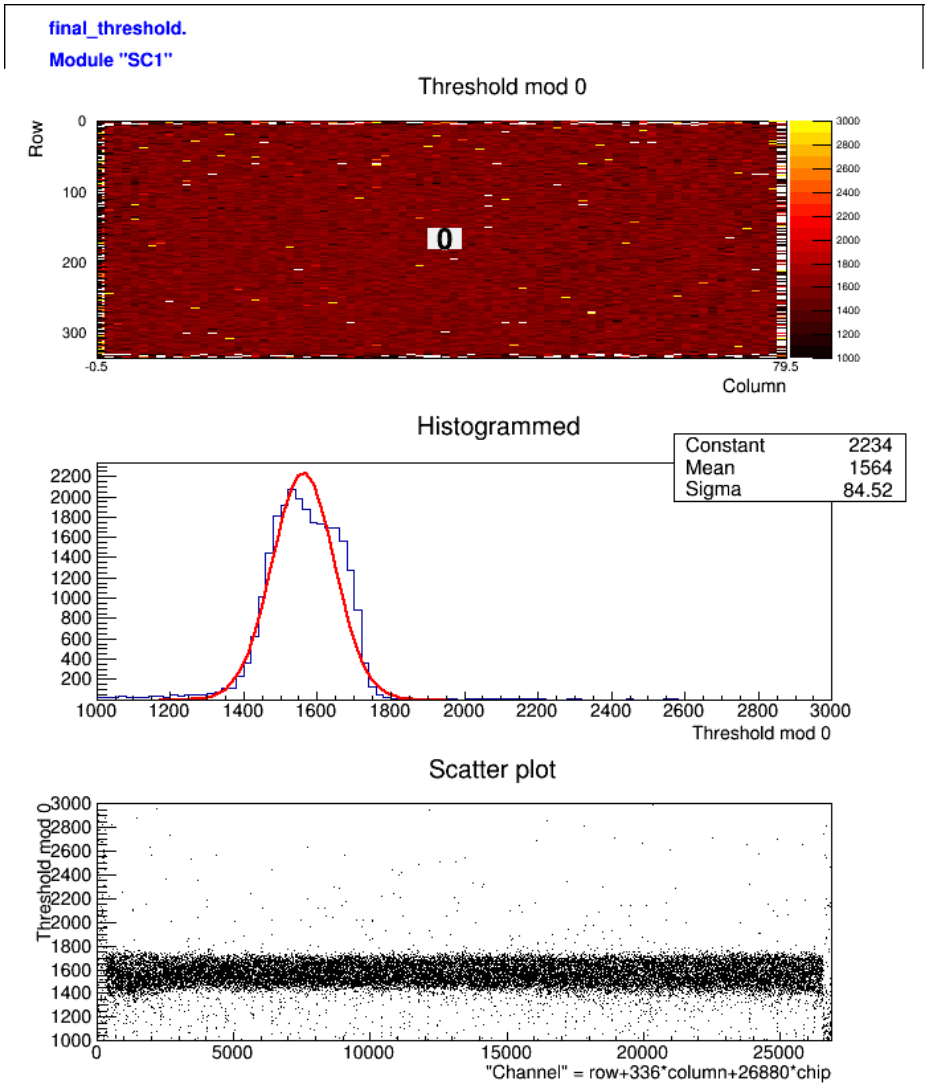


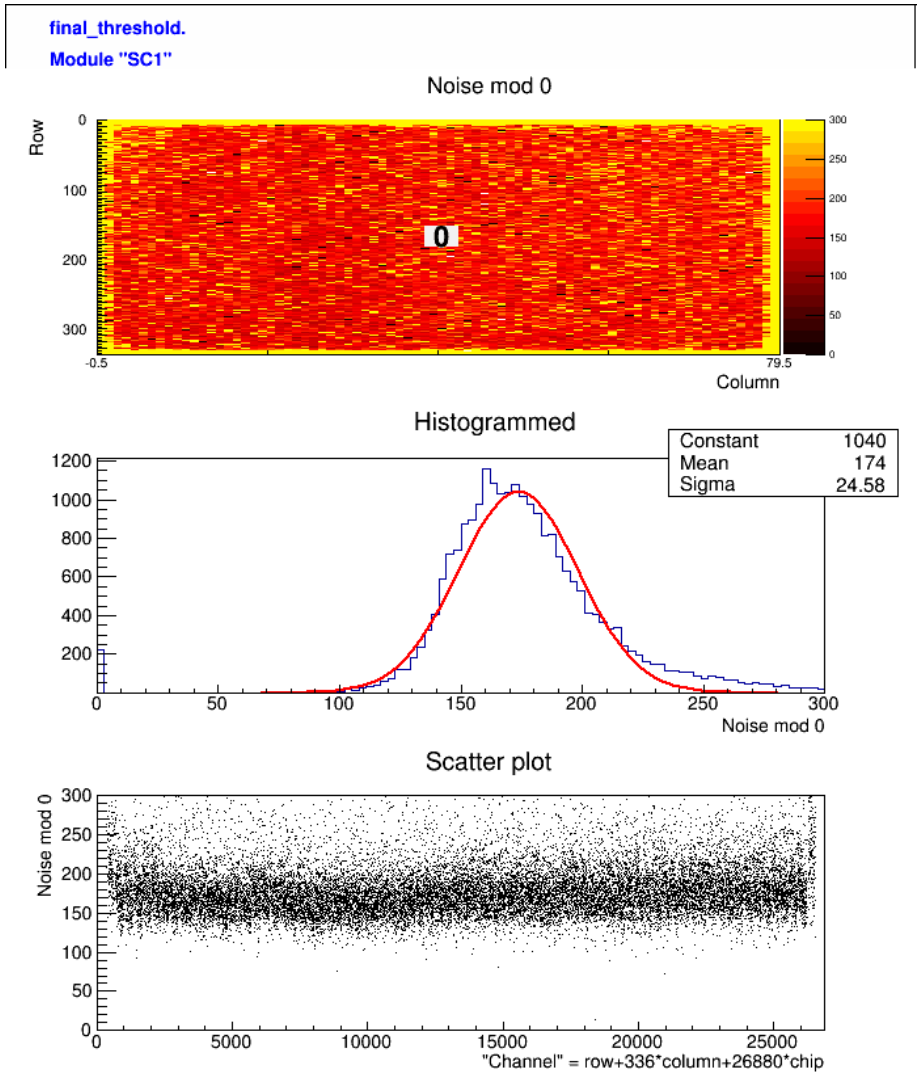


M. Bomben, Activities at LPNHE on edgeless planar pixel sensors

Irradiation at KIT

One sample irradiated to a dose = 1x10^15 neq /cm^2 (26 MeV protons)

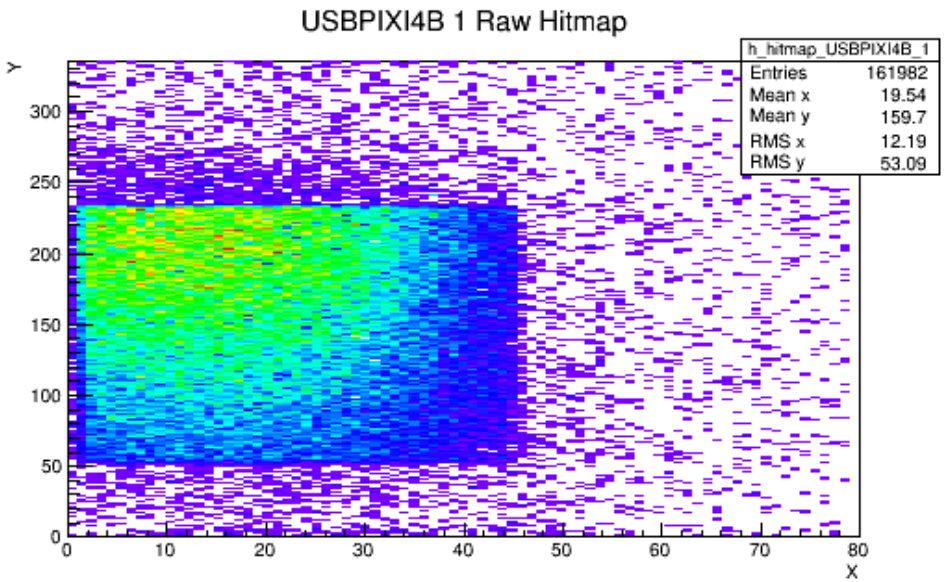




Tested on beam (II): CERN

Measured at SPS (120 MeV protons)

We were hoping to show the plot of hit-efficiency at the edge or the x and y resolution with high energy protons but …



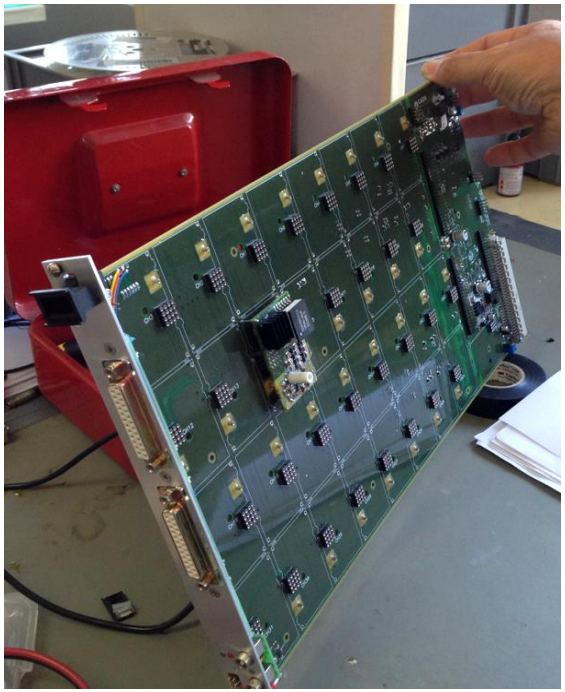
… the testbeam was only two weeks ago and the data is still being analyzed

Qualitative elements (integrated maps, correlations telescope-DUT etc. look ok)

Among other things, production used as test-bench to develop Power Board architectures

These sensors are used in the framework of a EU program of collaboration between University and Industry (IAPP). We have setup a common test-bench in C.A.E.N. at Viareggio (Italy) for the development of new HV power supply boards, in particular we optimized the architecture/specs of the new A1541/1542 cards.

It was a prototype last year



A1542 board

Now it is in production

New productions: FBK-AE-2 (collaboration INFN-FBK-LPNHE)

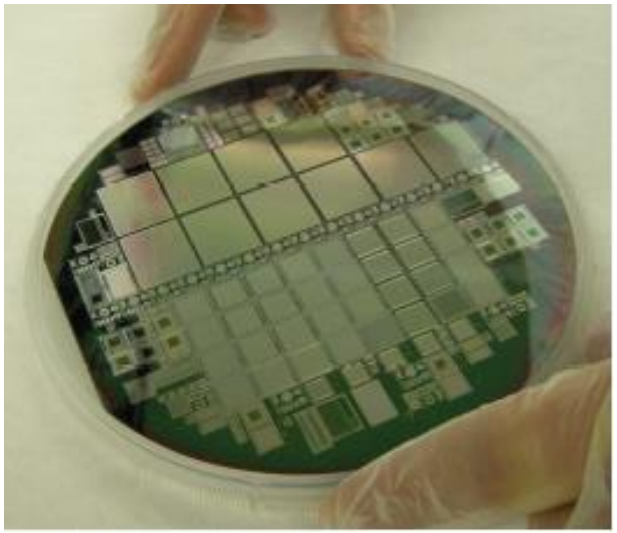
2014-15: FBK moved to 6”: first test production Silicon on Silicon (SiSi) wafers.

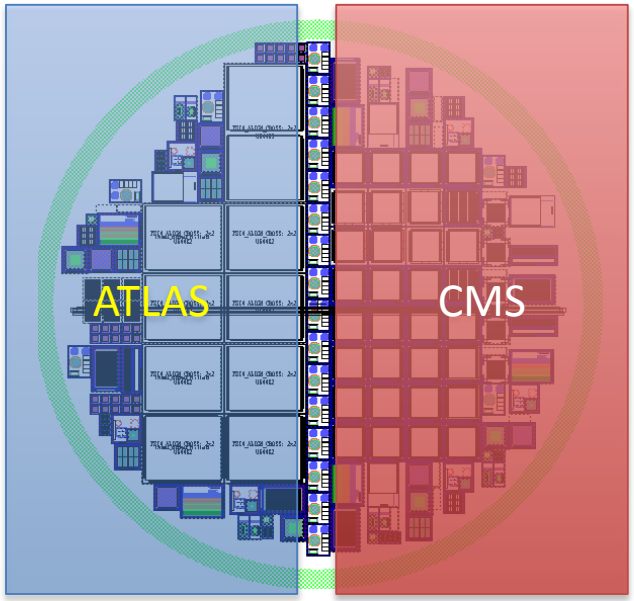
- No active edge, just preparation

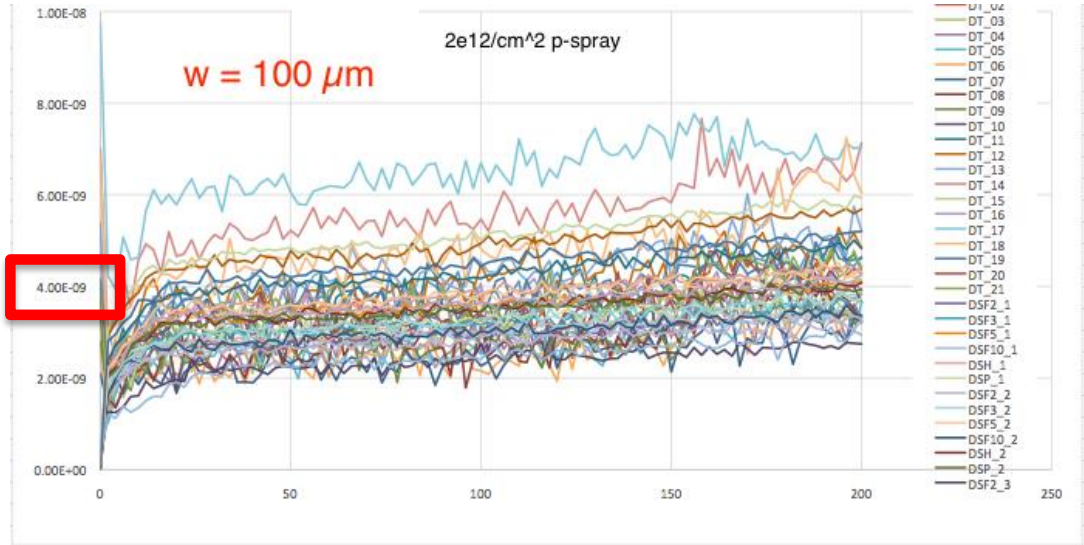
- Sensor wafer thicknesses: 100 µm and 130 µm
- Shared ATLAS and CMS production

  10 FEI4 (ATLAS) + 30 PSI46 (CMS)

  + test structures
- Production finished, electrical tests ok
- Flip-chip almost completed



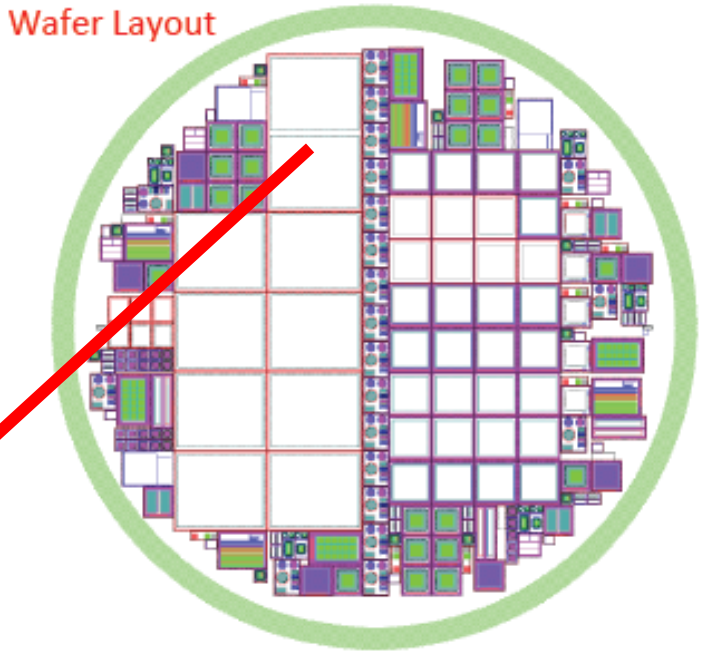


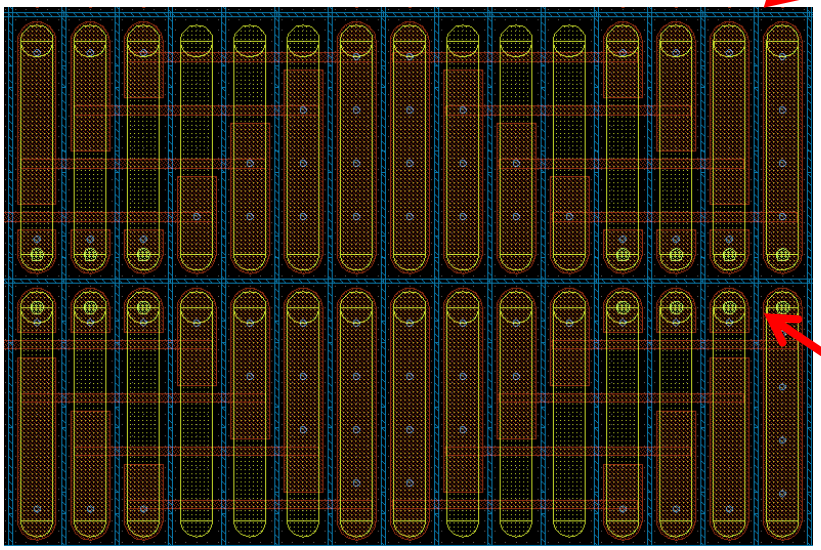


New productions: FBK-AE-3 (collaboration INFN-FBK-LPNHE)

- Late 2015, early 2016: new planar active production
- Based on DWB wafers of the same kind as mentioned in the previous slide

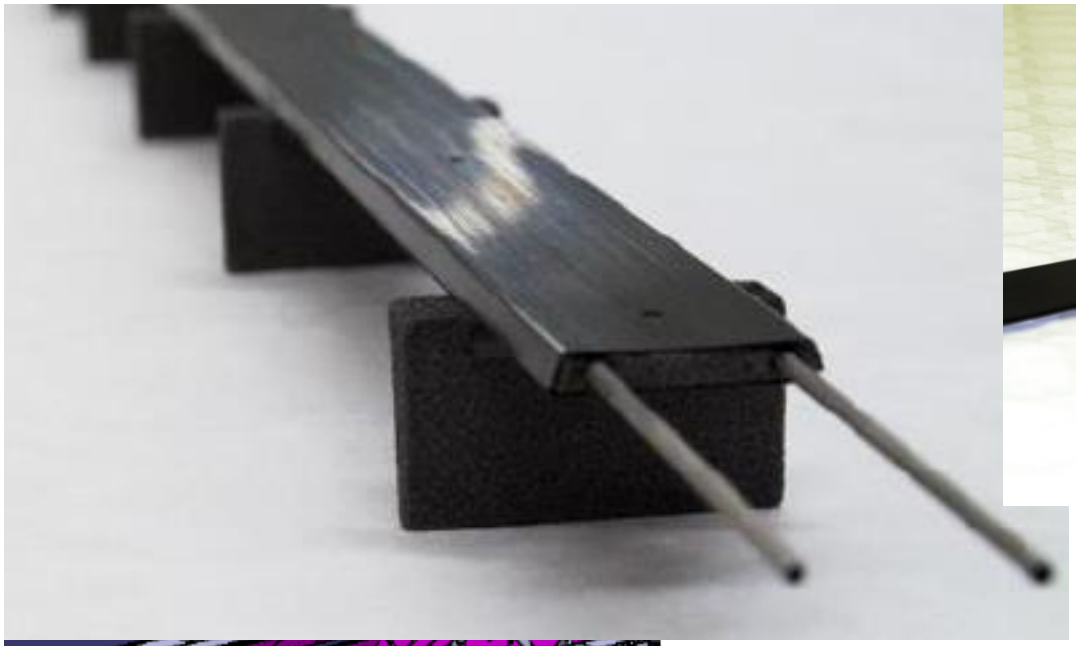
- Layout similar to previous production
- More aggressive designs for single FEI4 chip sensors
- Some RD53 chip-compatible sensors
- ATLAS: 1 double FEI4 chip sensor per wafer for the ALPINE layout

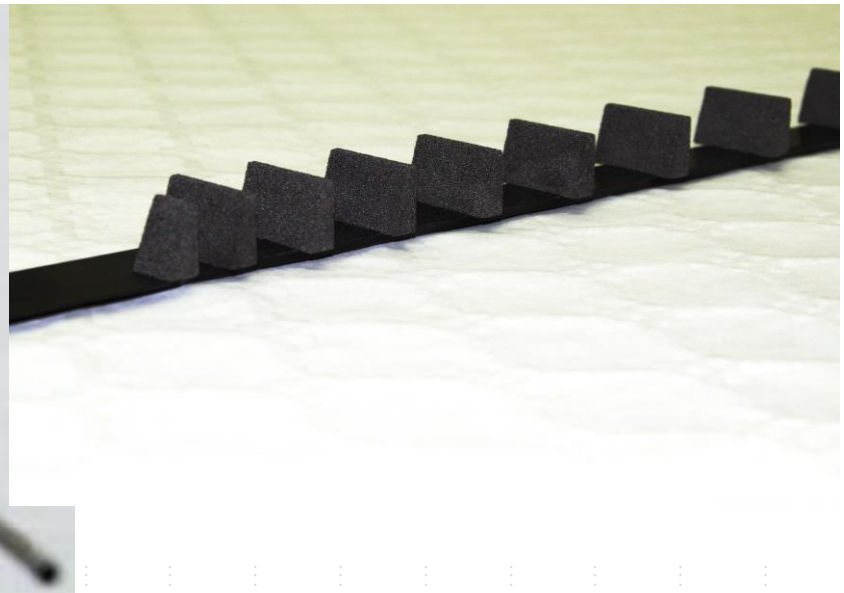


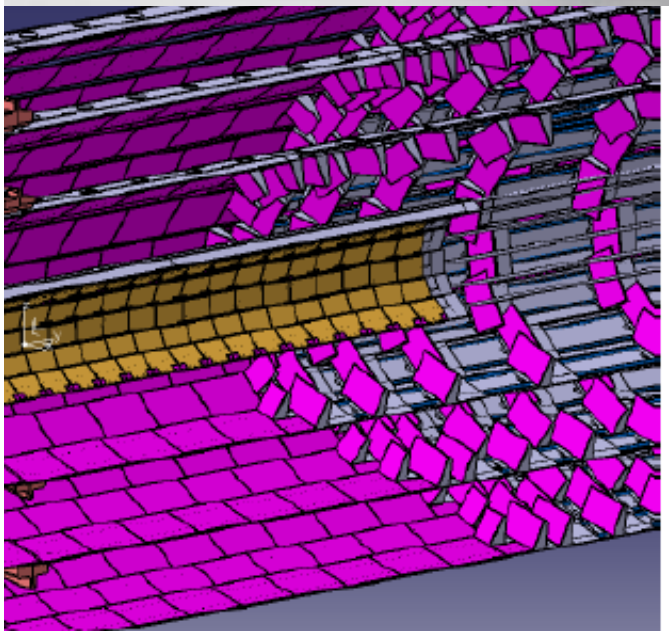


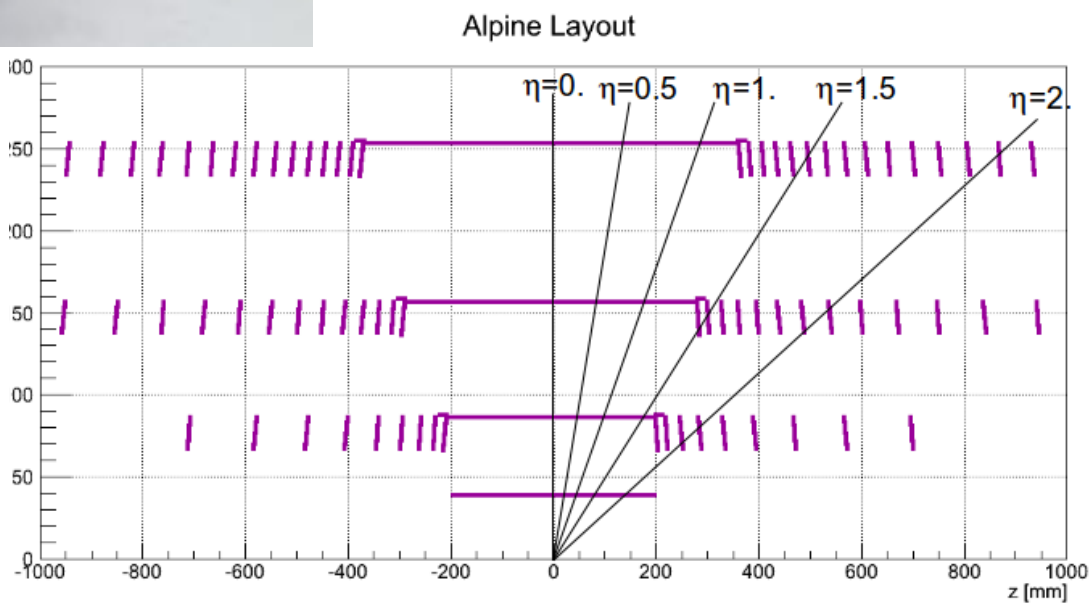
Detail of a "Mountain" sensor, specific for the Alpine layout

Alpine stave









Conclusions and future developments

- Active-edge sensors production in 4'' at FBK finished and tested
  Un-irradiated and irradiated modules on testbeams (DESY/CERN)
  Data rather consolidated, positive results
  CERN high energy proton data still missing
- FBK 6'' first production (no active-edge) delivered and tested. Flip-chip underway
- FBK 6'' first production (active-edge) ready to go as soon as we'll have feedback from the other one

Additional material

FBK/LPNHE active edge

Doped region	impurity	function	peak value (cm^{-3})	reference value (cm^{-3})	rolloff (μm)
Pixel and GR	D	gaussian	2×10^{19}	10^{16}	1.0
Back	A	gaussian	2×10^{19}	10^{16}	1.0
Trench	A	erf	2×10^{19}	10^{12}	2.0
Bias tab	A	gaussian	2×10^{19}	2×10^{16}	0.5
P-spray	A	gaussian	5×10^{16}	7×10^{15}	0.5
P-stop	A	gaussian	5×10^{17}	7×10^{16}	0.5

Table 3: Implant parameters for simulated detectors; A (D) is for acceptor (donor) impurities.

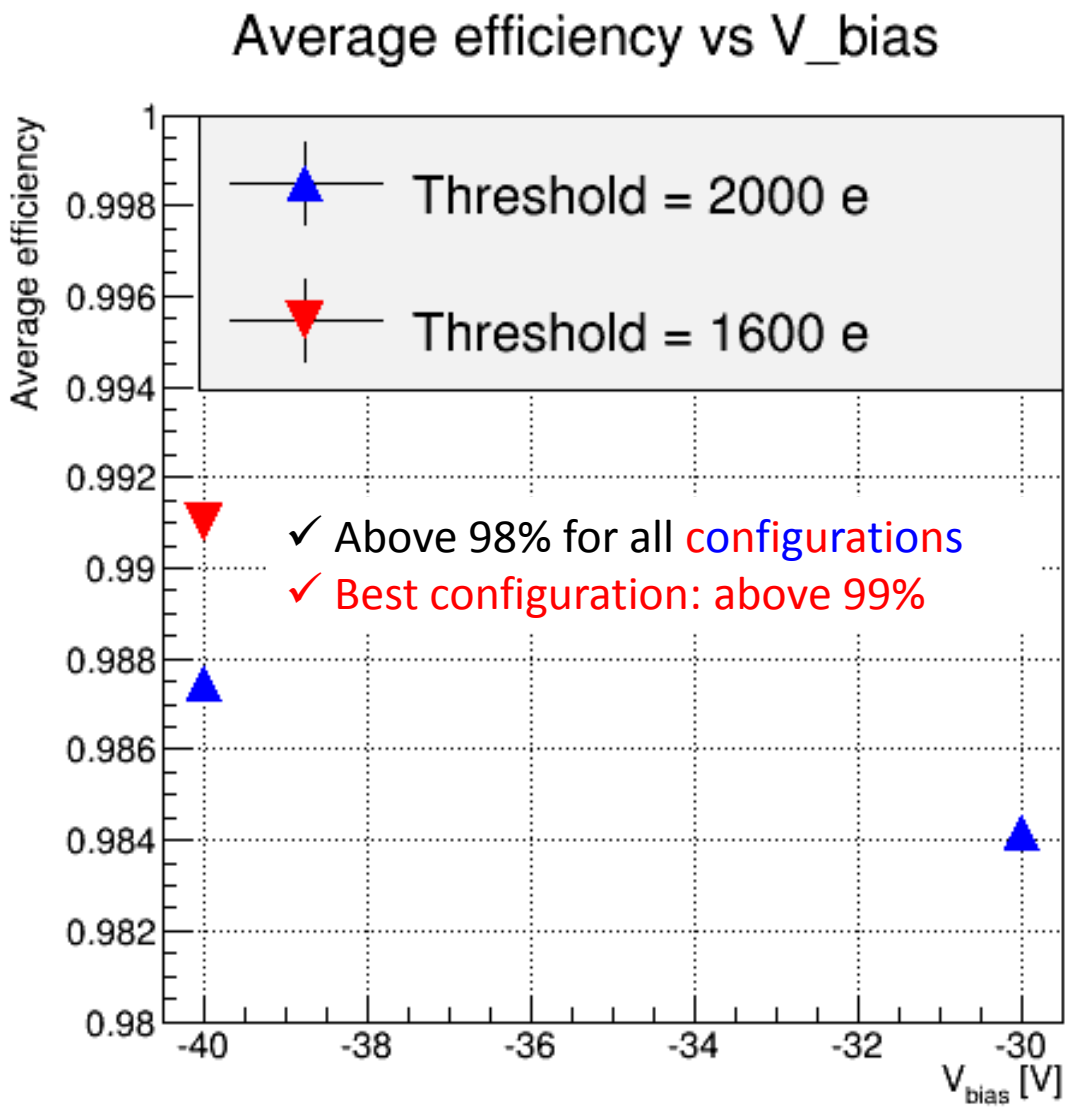
Multiplicity	Number of GRs	pixel-to-trench distance (μm)
1	0	100
1	1	100
1	2	100
4	3	200
1	5	300
1	10	400

Type	Energy (eV)	$\sigma_e(cm^2)$	$\sigma_h(cm^2)$	$\eta(cm^{-1})$
A	E_C -0.42	9.5×10^{-15}	9.5×10^{-14}	1.613
A	E_C -0.46	5.0×10^{-15}	5.0×10^{-14}	0.9
D	E_V +0.36	3.23×10^{-13}	3.23×10^{-14}	0.9

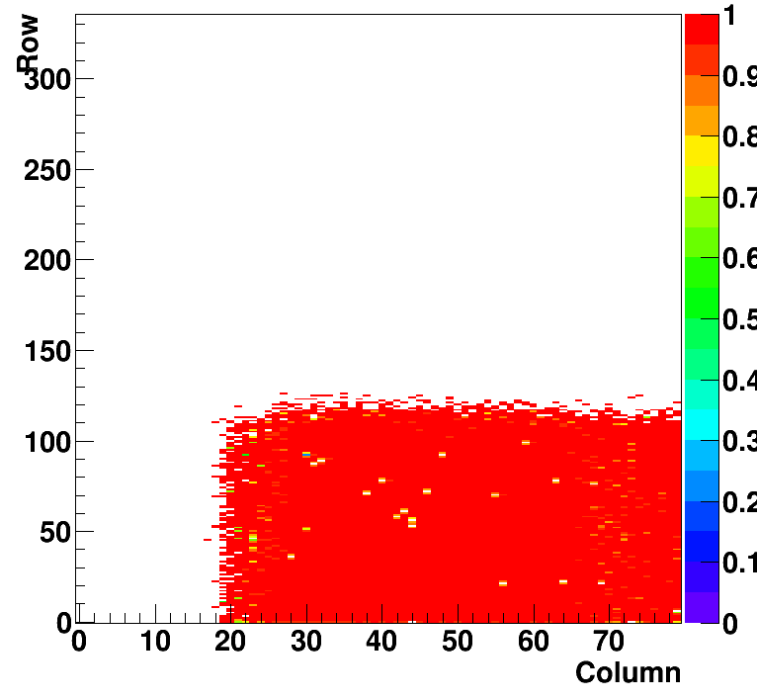
Table 4: Relevant parameters for acceptors (A) and donor (D) deep levels in the bandgap, describing the radiation damage.

Qox = 10^11 cm2, 3x10^12 cm2

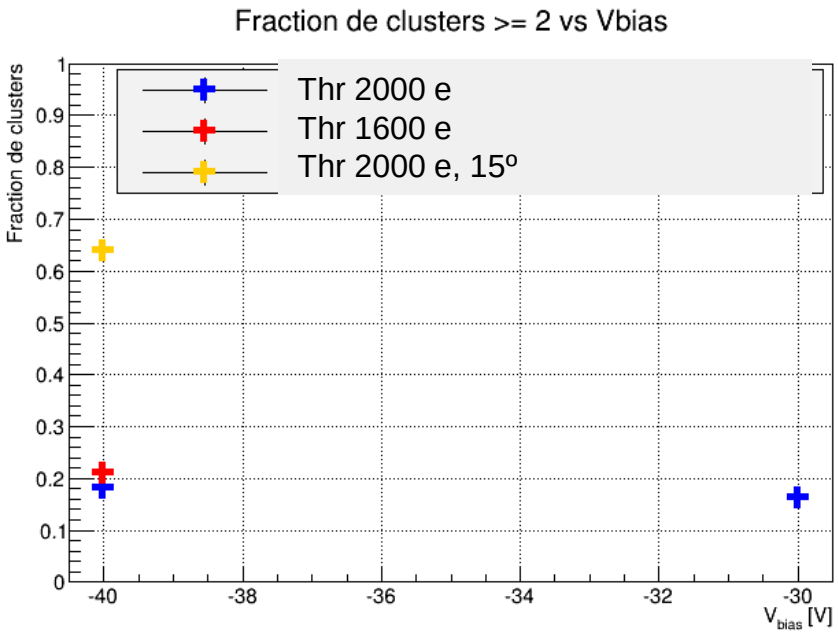
Global hit efficiency

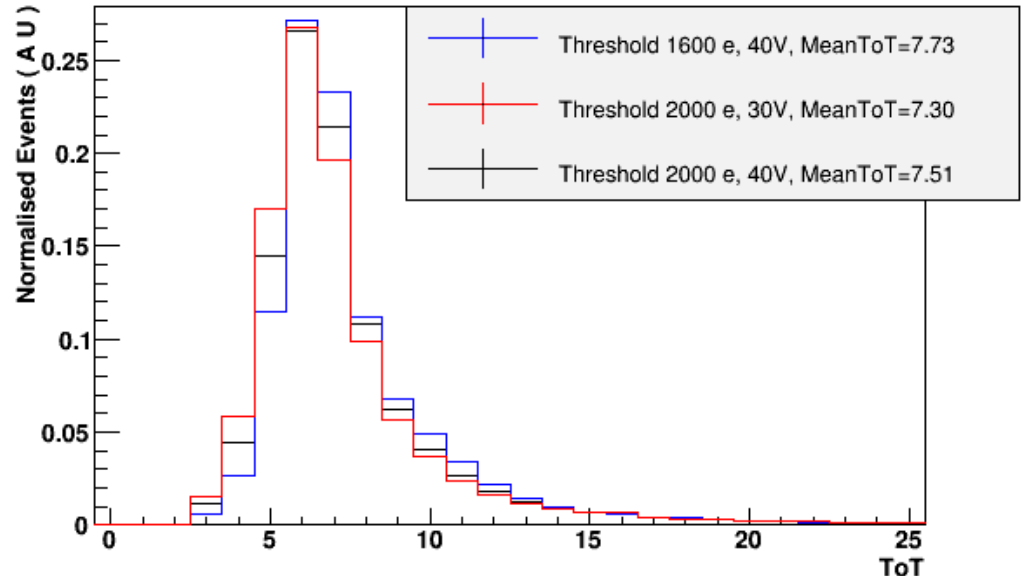


Example of eff. map

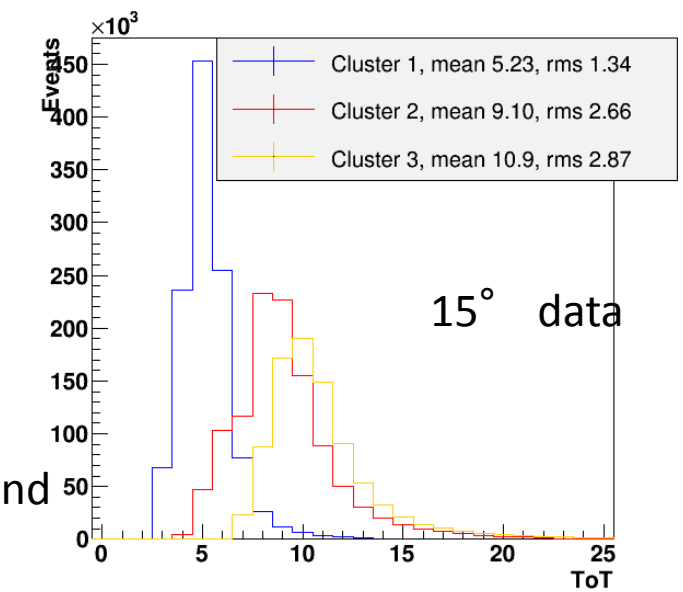


Cluster and collected charge properties





- Lower threshold and larger bias voltage ➔ larger clusters
- 15° data ➔ more than 60% of clusters with more than 1 pixel
- Lower threshold and larger bias voltage ➔ more charge
- 15° data ➔ significant correlation between cluster size and cluster charge



Setup

Mainframe Crate: **CAEN SY4527**

16-boards capacitance, controlled by A4528 CPU Full

HV board: **A1541N**

No. of Channels 32 (Common Floating Return)
Output Voltage 0÷500 V
Max. Output Current 10 mA
Voltage Set Resolution 10 mV
Voltage Monitor Resolution 1 mV
Current Set Resolution 200 nA
Current Monitor Resolution 10 nA
VMAX hardware 0÷500 V common for all the board channels
VMAX hardware accuracy 1 V
VMAX software 0÷500 V settable for each channel
VMAX software resolution 1 V
Ramp Up/Down 1÷50 Volt/sec, 1 Volt/sec step
Voltage Ripple < 10 mVpp (Max) full load
Maximum output power 5 W per channel
Power consumption A1541: 320 W @ full power
A1541L, A1541S: 240 W @ full power
A1541D: 120 W @ full power

Readout: **ATLAS USBPix**