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Perspective of 65 nm CMOS technology for radiation-tolerant electronics in high energy physics

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Due to the possibility of offering stronger data processing ability, 65 nm CMOS technology is being studied for the perspective of replacing the widely used 130 nm CMOS technology in CERN Large Hadron Collider (LHC). For electronics working under High Energy Physics (HEP) environments, the target has now been raised up to 1 Grad(SiO2) for the electronics in the LHC upgrade, which is the estimated deposited dose in 10 years after upgrade. Besides of that, it has been reported in 130 nm transistors that the heavy ion strike may induce the soft breakdown of the gate oxide, and then the driving currents of the transistors were highly reduced. It is not certain that if 65 nm transistors can successfully overcome these threats, and the suitability of this technology to the extreme HEP environments has to be evaluated.

In this paper, the radiation tolerance of a commercial 65 nm technology was verified by 3 MeV protons and heavy ions, to evaluate the long-term degradation and the possible existence of the micro-dose effect correspondingly. From the irradiation results, the 65 nm CMOS transistors showed severe long-term degradation especially in the drain saturation current. The good news is that the transistors did not behave any sudden loss of driving current even after multiple strikes of heavy ions at the gate oxide.

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