

AGIPD: A High Frame Rate Detector for the European XFEL

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The AGIPD (Adaptive Gain Integrating Pixel Detector) collaboration - consisting of Deutsches Elektronensynchrotron (DESY), University of Hamburg, University of Bonn and the Paul-Scherrer-Institute (PSI) - is currently developing a 2D hybrid pixel detector system capable to fulfill the requirements of the European XFEL (Eu-XFEL) that is currently being built in Hamburg (Germany) and where the first light is foreseen for the 1st January 2017.

At the Eu-XFEL photons will arrive in bunch trains every 100 ns (or at a rate of 10MHz). Each train consists of 2700 bunches that arrive within 600 ns (i.e. a bunch spacing of 220 ns, meaning 4.5 MHz frame rate) followed by 99.4 ns without pulses. Each single pulse consists of 1012 X-ray photons arriving in less than 100 fs and in an energy range between 250 eV up to 25 keV. In order to cope with the large dynamic range, the first stage of each pixel in the AGIPD ASIC is a charge sensitive preamplifier with three different gain settings that are dynamically switched during charge integration. Dynamic gain switching allows to have single photon resolution in the high gain stage and to cover a large dynamic range of 104-12.4 keV photons in the low gain stage with a linearity better than 1%. The high frame rate (4.5 MHz) requires a storage of the signal in the pixel before the readout takes place during the gap between bunch trains. The full scale chip (AGIPD1.0), received at the end of 2013, is a 64 x 64 pixel matrix. Each pixel (Area 200 x 200 μm^2) is equipped with 352 storage cells. The single module system is composed by 8 x 2 AGIPD chips and the 1M system, that is actually in construction and is foreseen to be ready during summer, consists of 4 quadrants of 4 modules each, for a total of 16 modules. First measurements show that the goal of a dynamic range of 104-12.4 keV and a noise of 270 el. has been achieved. In this presentation a general overview of the AGIPD 1M system will be given. The focus will be on the characteristics of the ASIC including first experimental results. We will present the current status and give an overview over the foreseen upgrade of the readout chip.

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