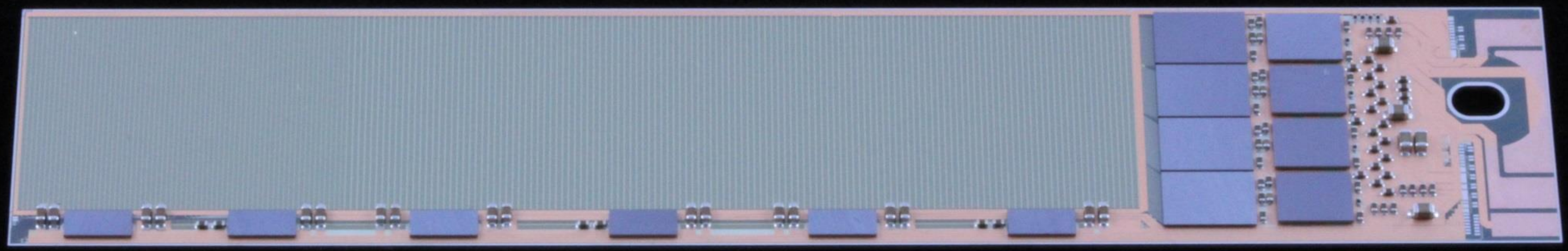
The Belle II DEPFET Pixel Detector

B factories
- motivation for upgrade

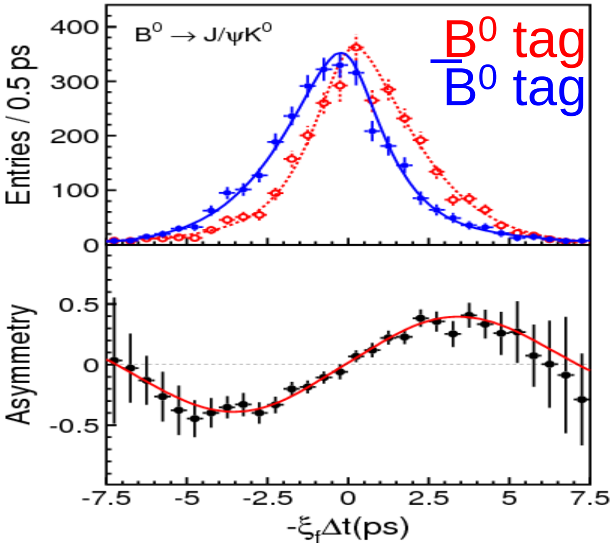
SuperKEB
Belle II



The DEPFET Pixel Detector
-principle & properties
-module concept
-ASICs
-material
-system aspects (cooling)
-Gated operation
Status & Conclusions

B-factory Detectors a huge success!

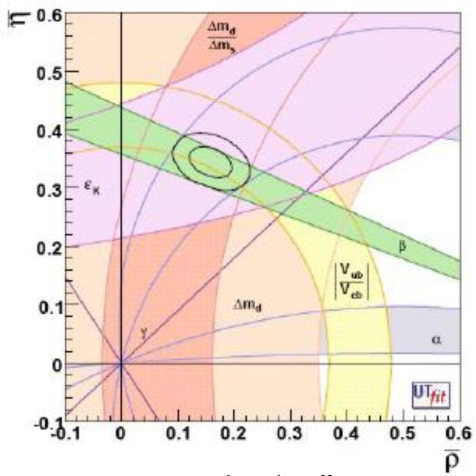
- Measurements of CKM matrix elements and angles of the unitarity triangle
- Observation of direct CP violation in B decays
- Measurements of rare decays (e.g., $B \rightarrow \tau\nu$, $D\tau\nu$)
- $b \rightarrow s$ transitions: probe for new sources of CPV and constraints from the $b \rightarrow s\gamma$ branching fraction
- Forward-backward asymmetry (A_{FB}) in $b \rightarrow sll$ has become a powerfull tool to search for physics beyond SM.
- Observation of D mixing
- Searches for rare τ decays
- Observation of new hadrons



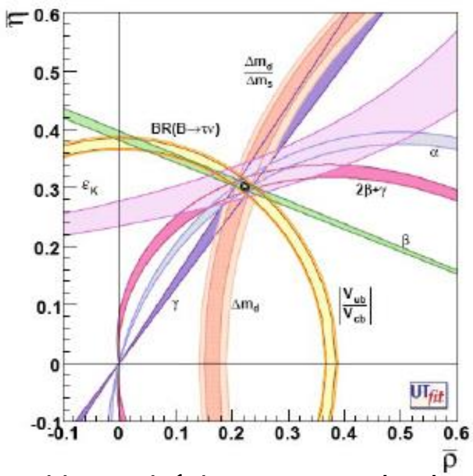
Motivation for upgrade:

Measure CKM elements as precisely as possible
Overconstrain unitarity triangle
Look for deviations from SM

=> Need about 50 ab^{-1}

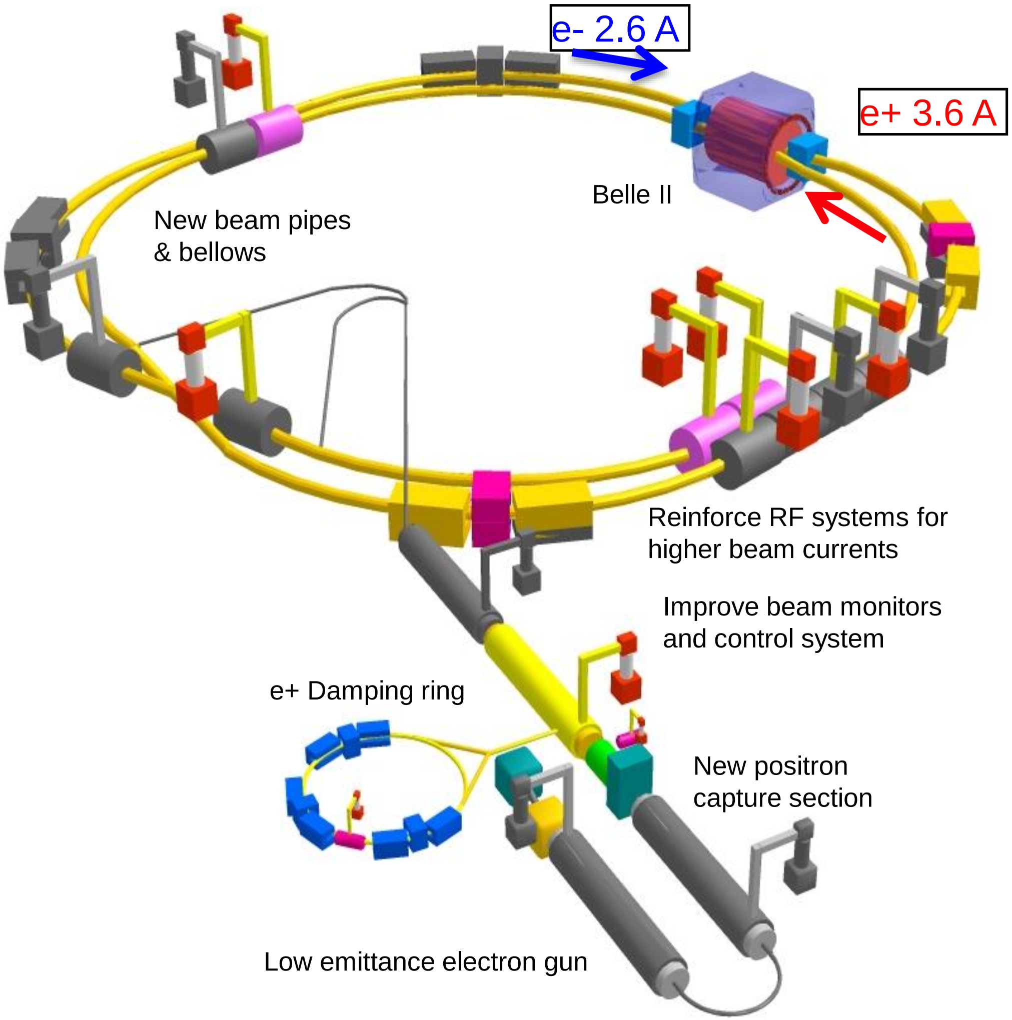


Babar/Belle



With 50 ab^{-1} (same central values)

KEKB to SuperKEKB



Upgrade KEKB to reach
$L = 8 \times 10^{35}\ cm^{-2}s^{-1}$

(40 x luminosity of KEKB)

Nano Beams: 10µm x 60nm
Increase beam current (x2)

Reduce asymmetry (boost)

KEB:
$\beta\gamma = 0.42$ (8 GeV, 3.5 GeV)

SuperKEKB:
$\beta\gamma = 0.28$ (7 GeV, 4 GeV)

Requirements for the Belle II detector

Critical issues at L= 8 x 10^{35}/cm^2/sec

- **Higher background (×10-20)**

  - radiation damage and occupancy
  - fake hits and pile-up noise in the EM Calorimeter

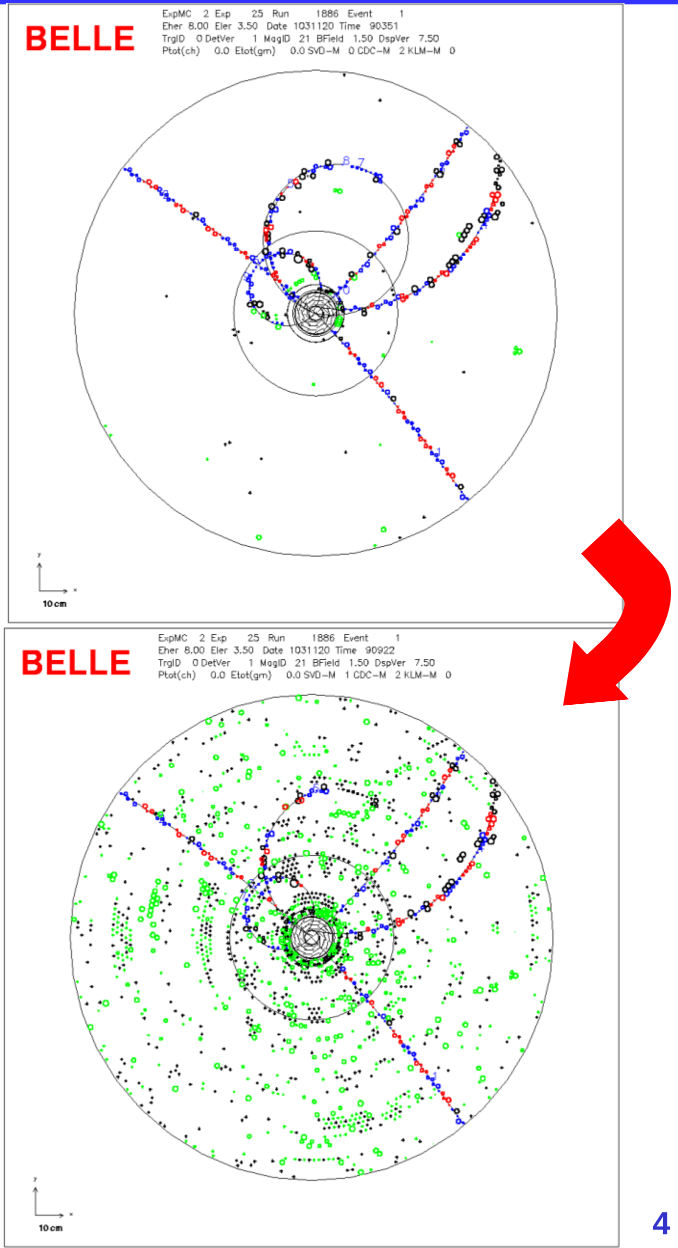
- **Higher event rate (×10)**

  - higher rate trigger, DAQ and computing

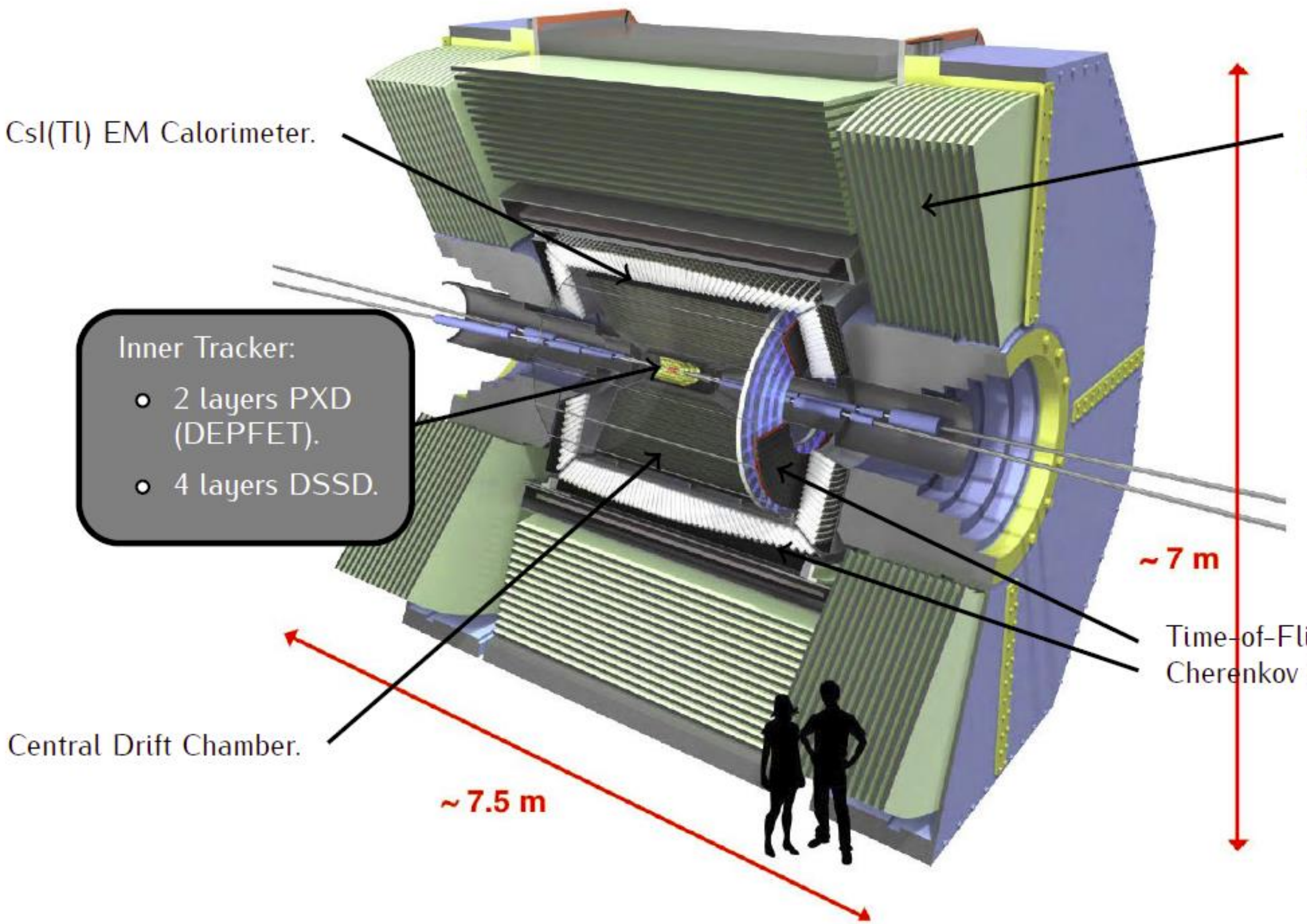
- **Special features required**

  - $\gamma\beta$ reduced by a factor of 2: compensated by improved vertexing

Result: significant upgrade of detector needed

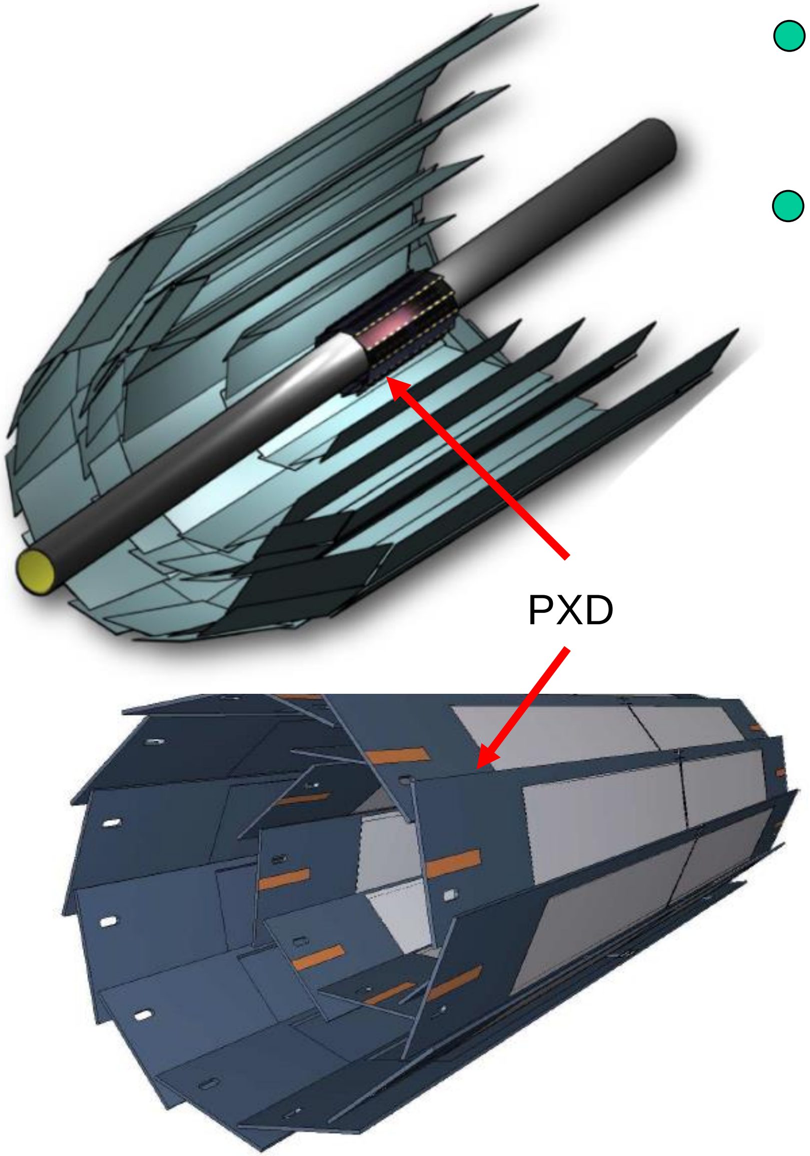


Belle II



CsI(Tl) EM Calorimeter.
RPC μ & K_L counter:
Scintillator + Si-PM
Inner Tracker:
2 layers PXD (DEPFET).
4 layers DSSD.
~ 7 m
Time-of-Flight, Aerogel
Cherenkov Counter.
Central Drift Chamber.
~ 7.5 m

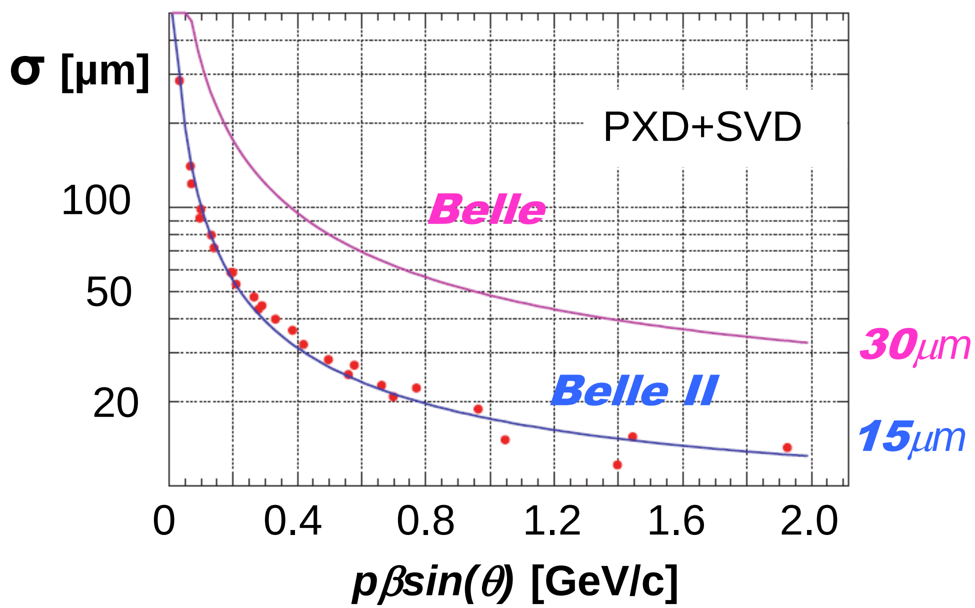
Silicon Tracking System @ Belle II



- SVD: 4 layer Si strip detector (DSSD)
  (R = 3.8, 8.0, 11.5, 14.0 cm)

- PXD: 2 layer Si pixel detector (DEPFET technology)
  (R = 1.4, 2.2 cm)
  monolithic sensor
  thickness 75 µm (!),
  pixel size 50 x 55 µm² to 50 x 85µm² (depending on layer and z)

Significant improvement in z-vertex resolution



DEPFET

Each pixel is a p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

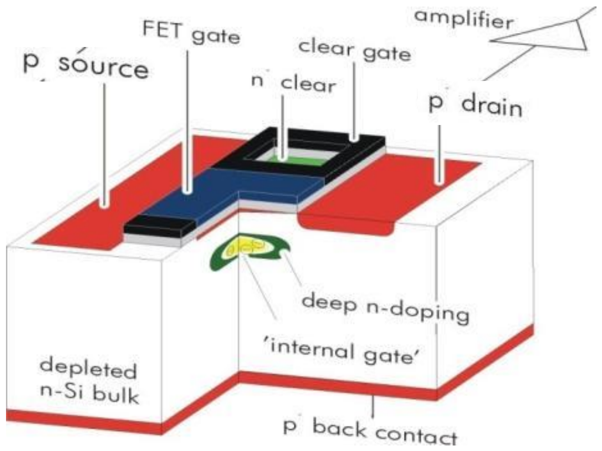
Accumulated charge can be removed by a clear contact ("reset")

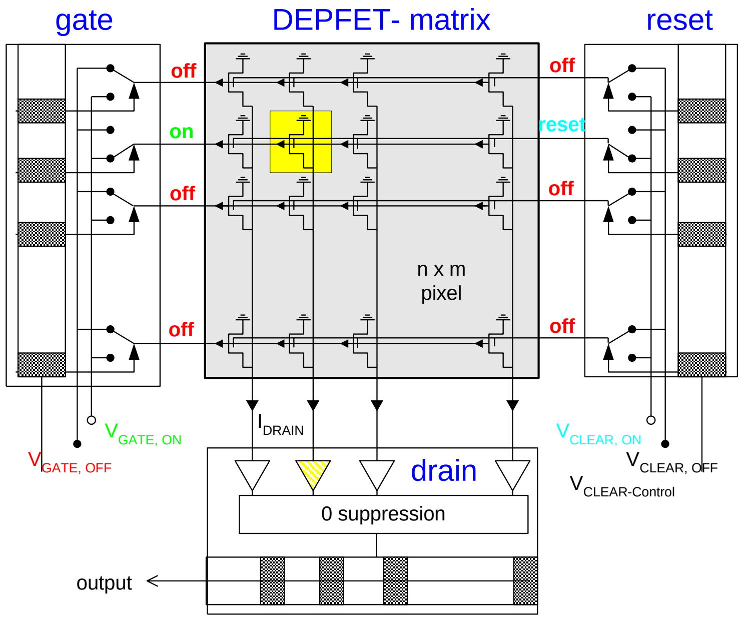
Fully depleted:
⇒large signal, fast signal collection

Low capacitance,
internal amplification: => low noise

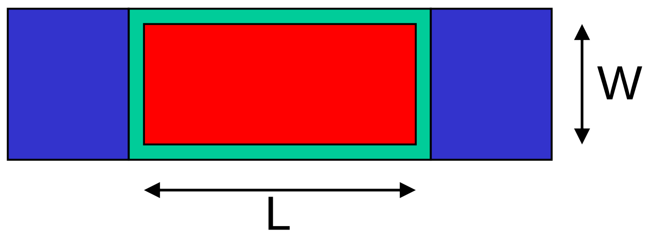
High S/N even for thin sensors

Rolling shutter mode (column parallel) for matrix operation
⇒20 µs frame readout time
=> Low power (only few lines powered),

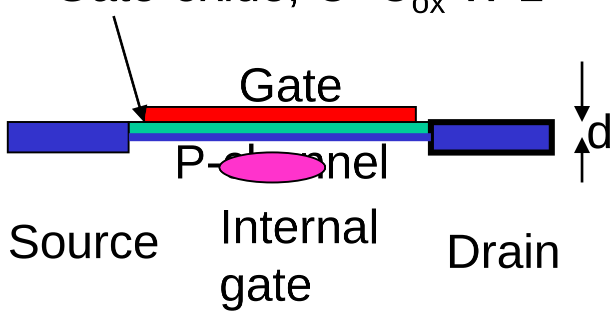




How does the DEPFET work?



Gate-oxide; $C = C_{ox} W L$



A charge q in the internal gate influences a mirror charge αq in the channel
($\alpha < 1$, for stray capacitance)
This mirror charge is equivalent to a change of the gate voltage:

$\Delta V = \alpha q / C = \alpha q / (C_{ox} W L)$

FET in saturation:

$$I_d = \frac{W}{2L} \mu C_{ox} (V_G - V_{th})^2$$

$$I_d = \frac{W}{2L} \mu C_{ox} \left(V_G + \frac{\alpha q_s}{C_{ox} W L} - V_{th} \right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Transconductance:

Charge factor:

$$g_m = \frac{dI_d}{dV_G} = \frac{W}{L} \mu C_{ox} (V_G - V_{th})$$

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha \mu}{L^2} \left(V_G + \frac{\alpha q_s}{C_{ox} W L} - V_{th} \right) = \alpha \sqrt{2 \frac{I_d \mu}{L^3 W C_{ox}}}$$

$$g_m = \sqrt{\frac{2 W \mu C_{ox} I_d}{L}}$$

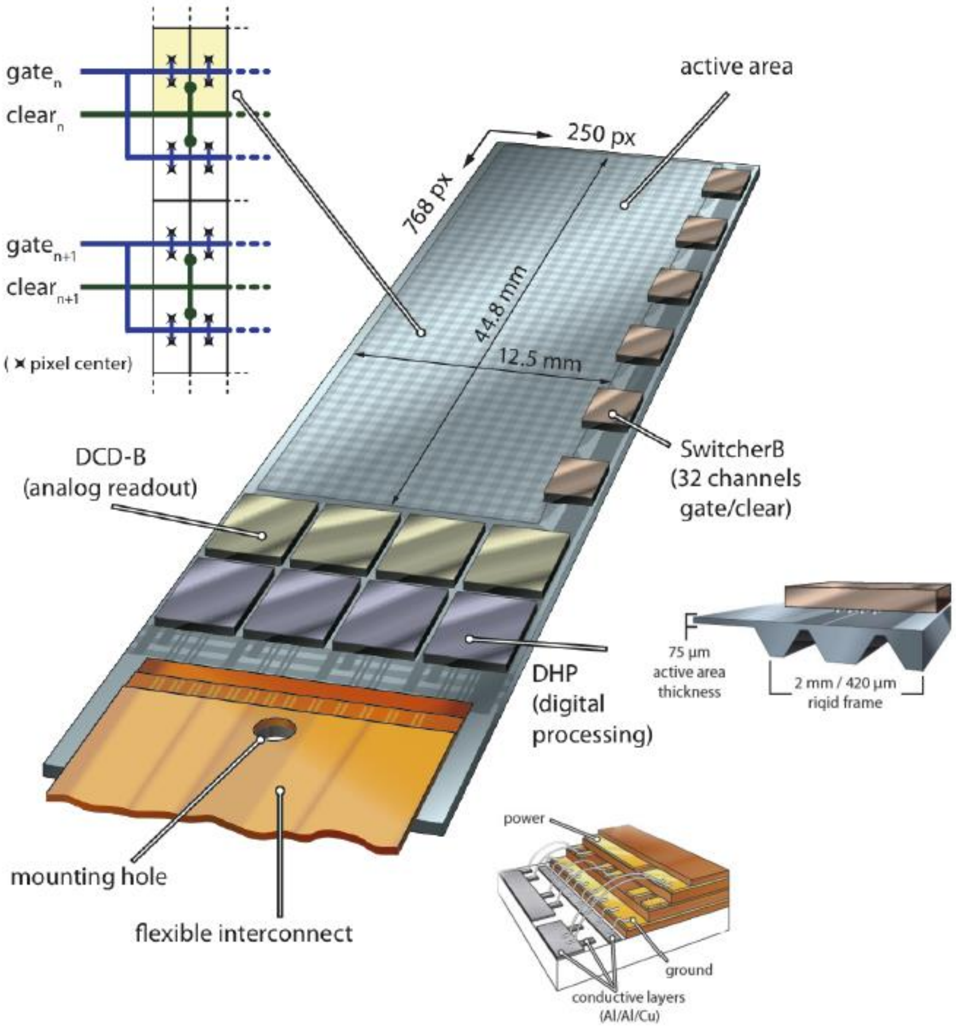
$$g_q = \alpha \frac{g_m}{W L C_{ox}} = \alpha \frac{g_m}{C}$$

Sensor Module/Ladder

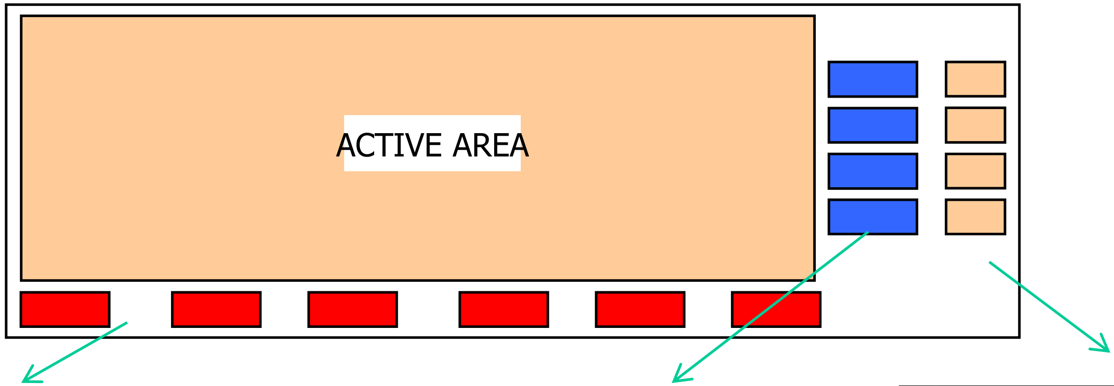
Each ladder made of two modules

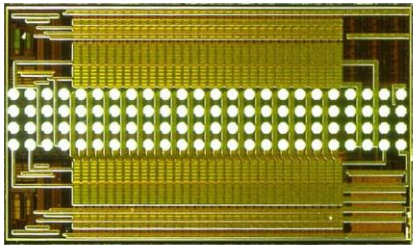
Module: monolithic piece of silicon
- sensor
- support for ASICs (bump bonded)
- 3 metal layers for electrical connection of ASICs

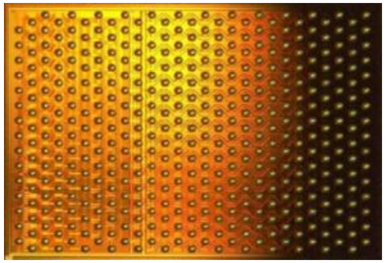
	Layer 1	Layer 2
Module	8	12
Radii	14 mm	22 mm
Ladder Size	15x136 mm^2	15x170 mm^2
Pixel Size	50x55 μm^2 50x60 μm^2	50x70 μm^2 50x85 μm^2
Pixels	250x1536	250x1536
Thickness	75 μm	75 μm

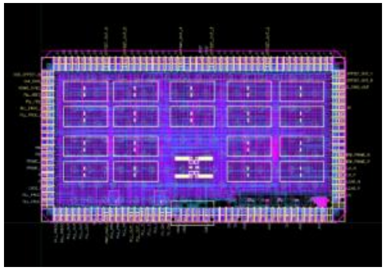


ASICs for control and readout









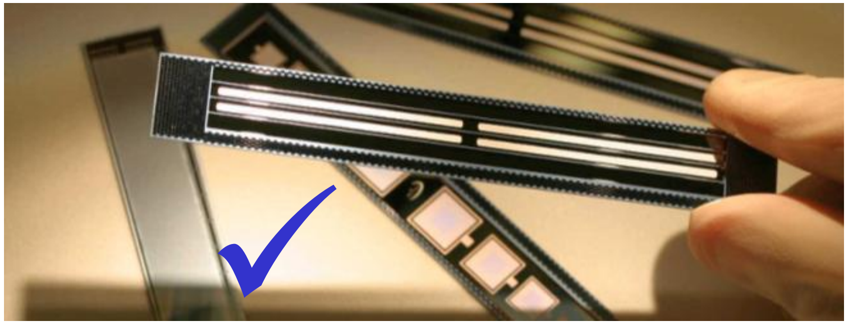
Switcher
Control of gate and clear
32 x 2 channels
Switches up to 30V
AMS 0.18 µm HV technology
Tested up to 36 Mrad

DCDB
Amplification and digitization of DEPFET signals
256 input channels
8-bit ADC per channel
92 ns sampling time
UMC 180nm
Rad hard design

DHP
Signal processor
Common mode correction
Pedestal subtraction
0-supression
Timing and trigger control
TSMC 65nm
Rad hard

All three chips fabricated and tested, final submission done/prepared

Sensor Thinning



Need thin (50µm-75µm) self supporting all silicon module

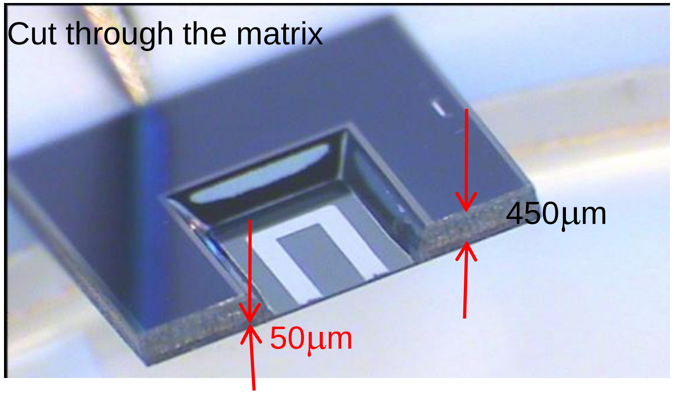
Process backside e.g. structured implant

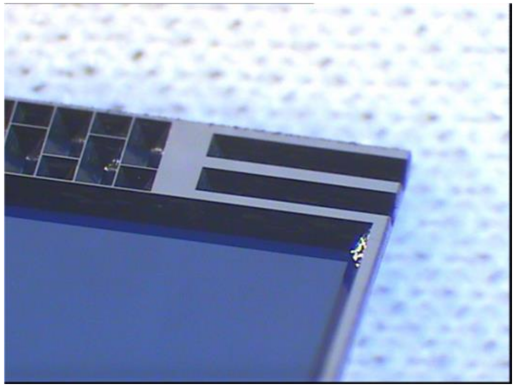
Wafer bonding SOI process

Thinning of top wafer (CMP)

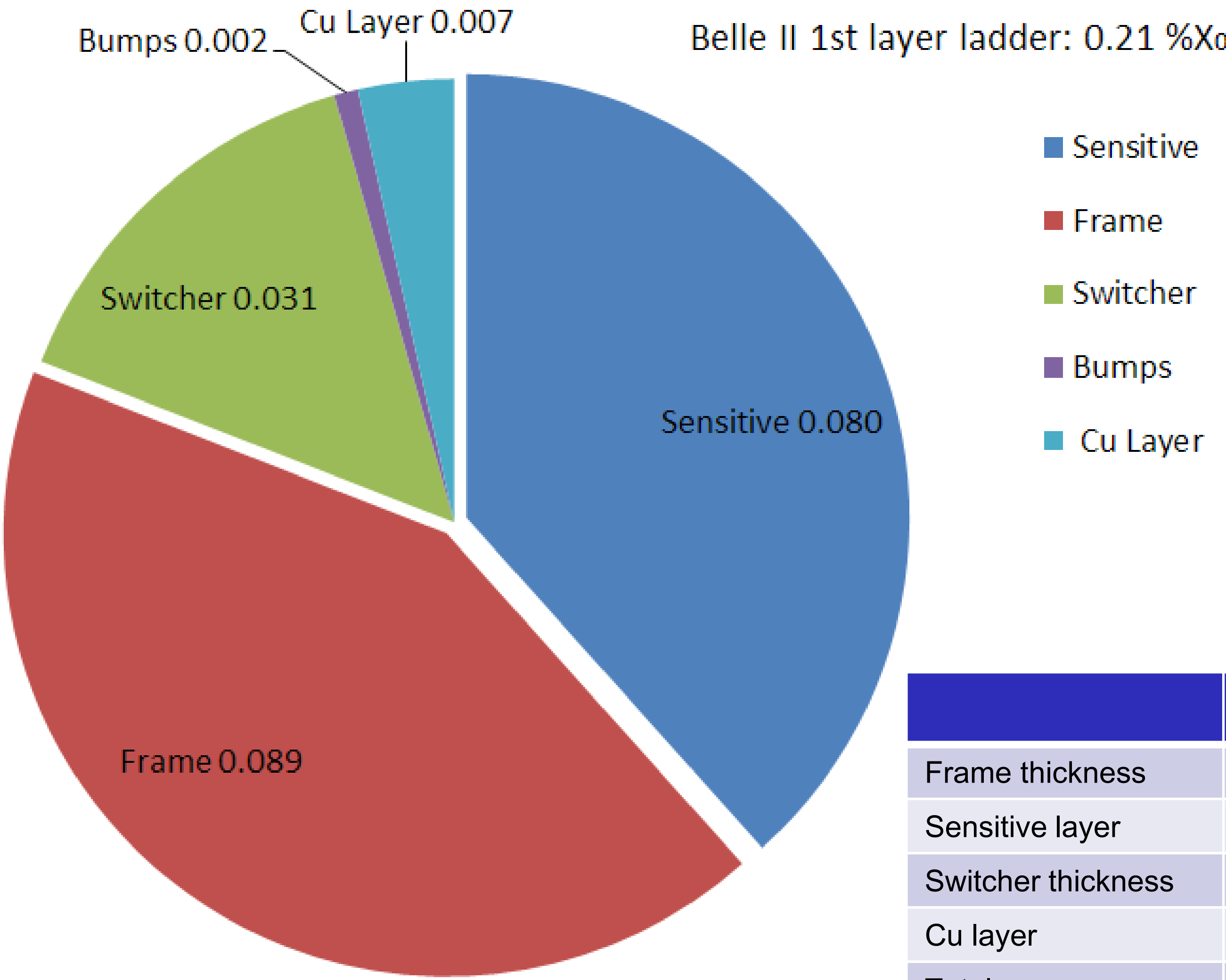
Processing

etching of handle wafer (structured)



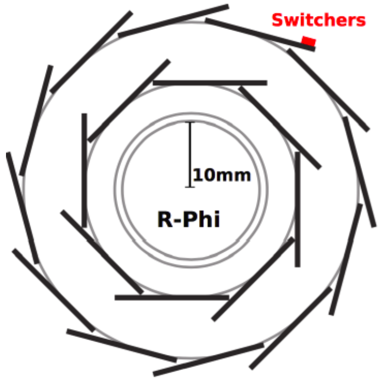


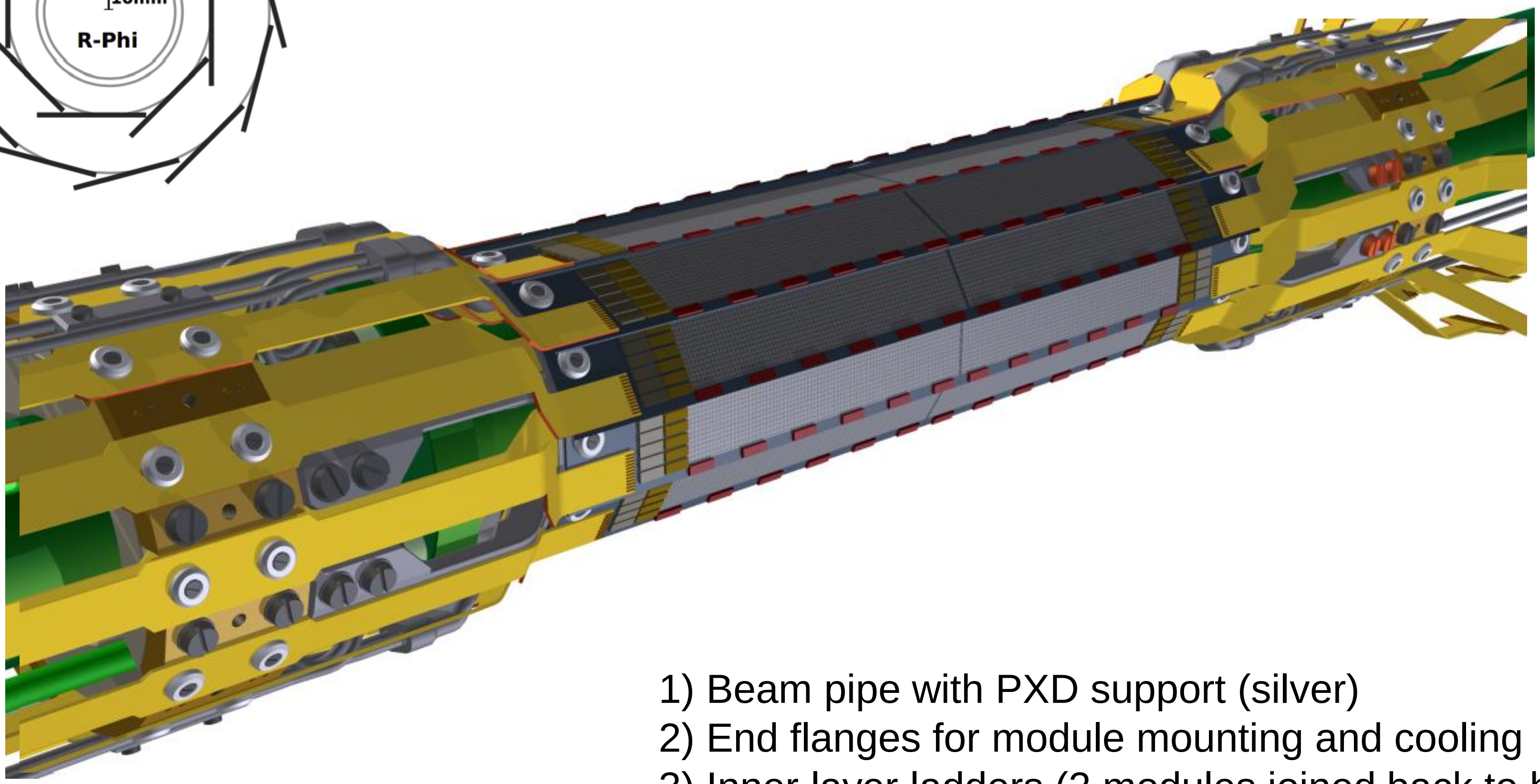
Material Budget (single layer)



	Belle II
Frame thickness	525 µm
Sensitive layer	75 µm
Switcher thickness	500µm
Cu layer	only on periphery
Total	0.21 %X0

Support

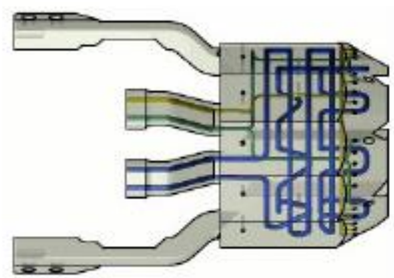




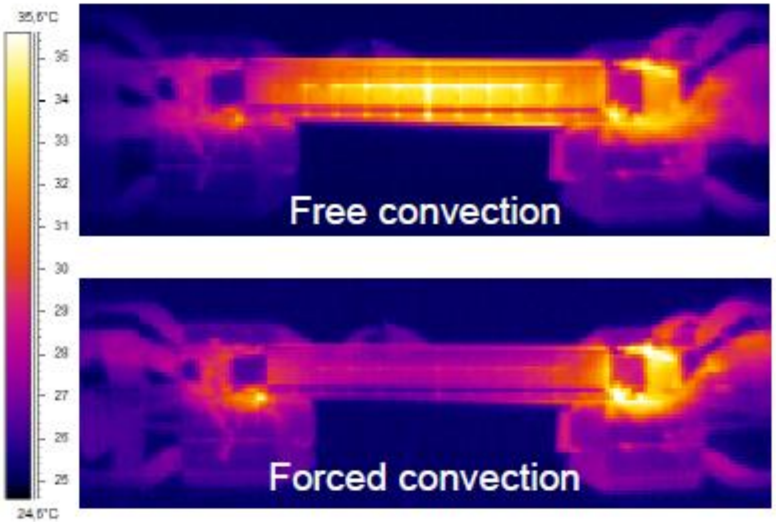
1) Beam pipe with PXD support (silver)
2) End flanges for module mounting and cooling
3) Inner layer ladders (2 modules joined back to back)
4) Outer layer ladders (2 modules joinded back to back)

Cooling

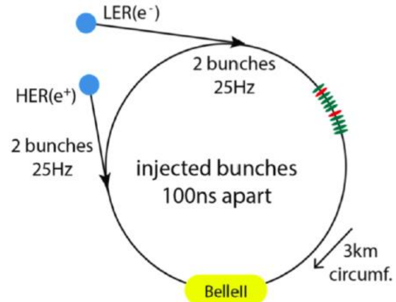
CO_2 cooling for the electronics outside the detector acceptance (320W)
Cold N_2 flow to cool sensors and switcher electronics (40W, 150mW/cm²)

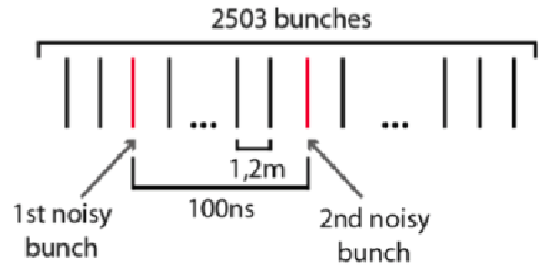


- Stainless steel
- Fast sintering
- Blue: CO2 channels
- Yellow: Air channels



Injection Noise & Gating





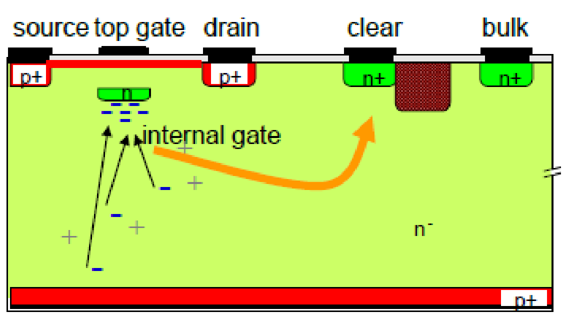
Continuous injection with 50 Hz
Every 20 ms two bunches are topped up
'cooling' time: ca 4ms
'noisy' bunches pass the interaction region every 10µs

DEPFET frame readout needs 20µs (and covers a time interval of 40 µs)
=> Sensor filled with hits from freshly injected bunches => ~ 20% dead time (4ms/20ms)

Gating : Sensor is made blind for a short time during high background (noisy bunch)
Signals detected in the clean period before are preserved

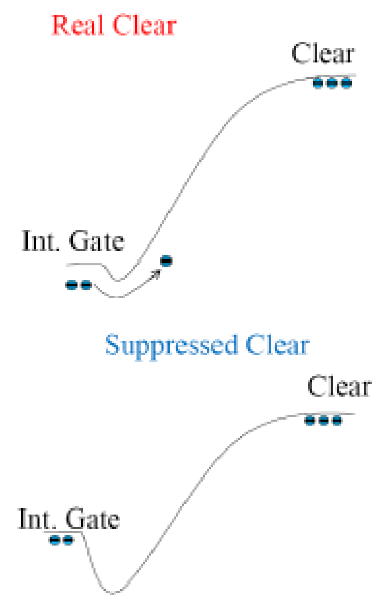
In normal clear operation the gate is pulsed negatively (repels electrons)

The clear contact is pulsed positively (attracts electrons from internal gate and bulk underneath)



In gated mode the gate is not pulsed and remains attractive for electrons.

The clear is pulsed positively, and attract electrons from the bulk underneath

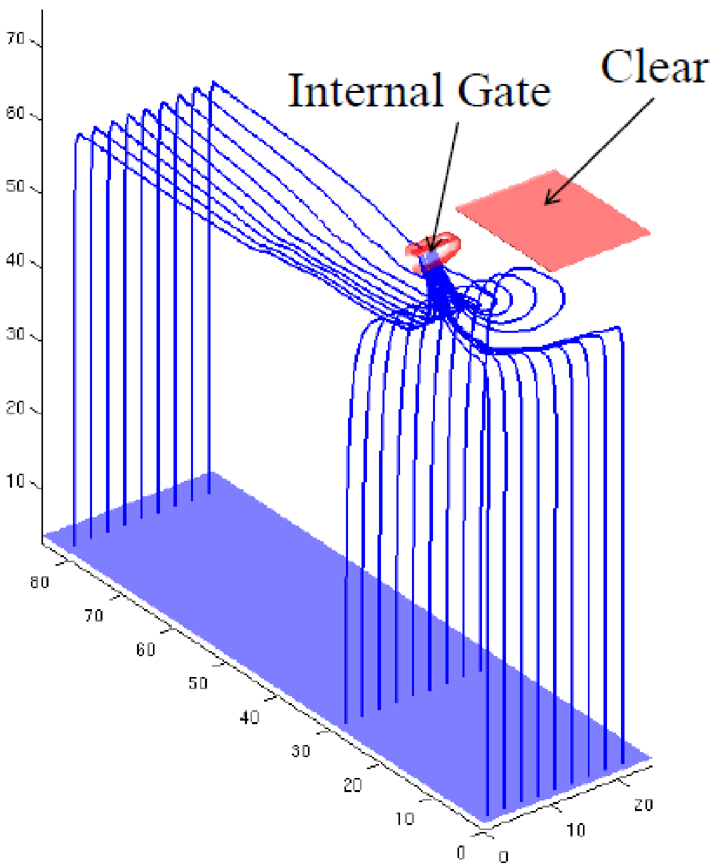


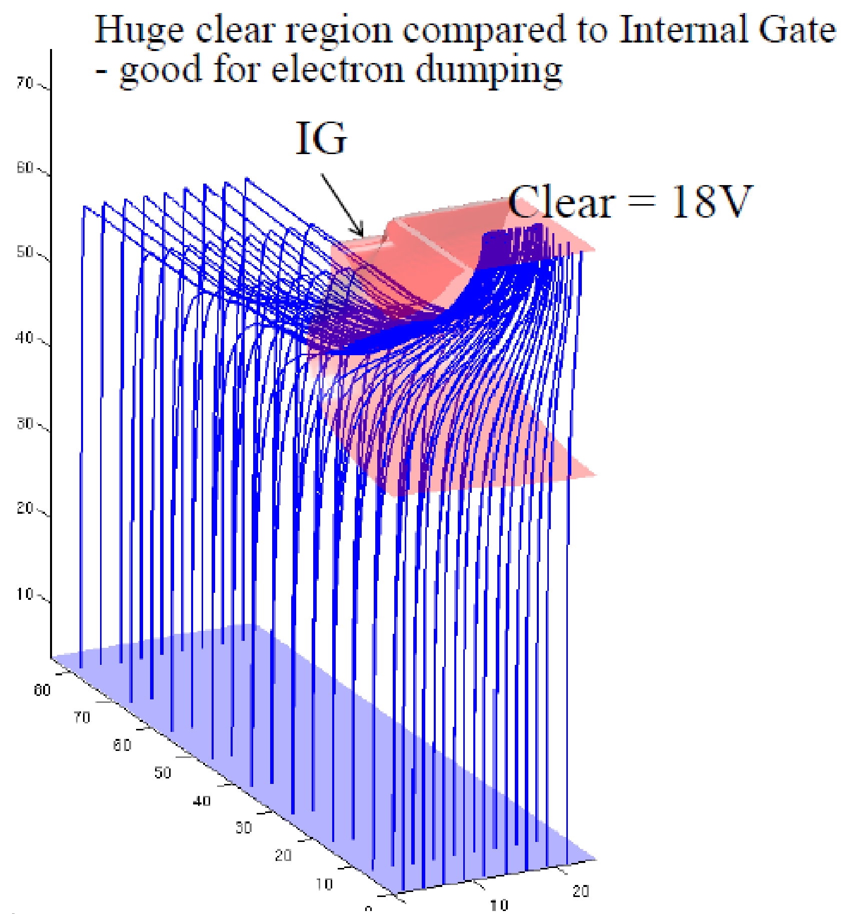
Electron drift directions

Normal operation:
Signal charge drifts into internal gate

Gated Mode
Charges from background drift directly to clear gate

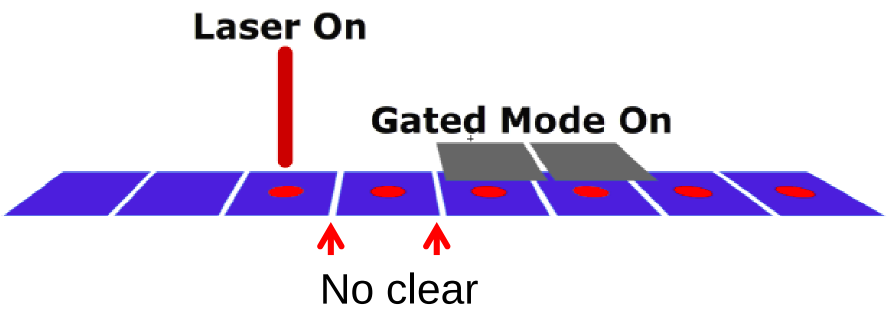
Signal already stored in internal gate is protected

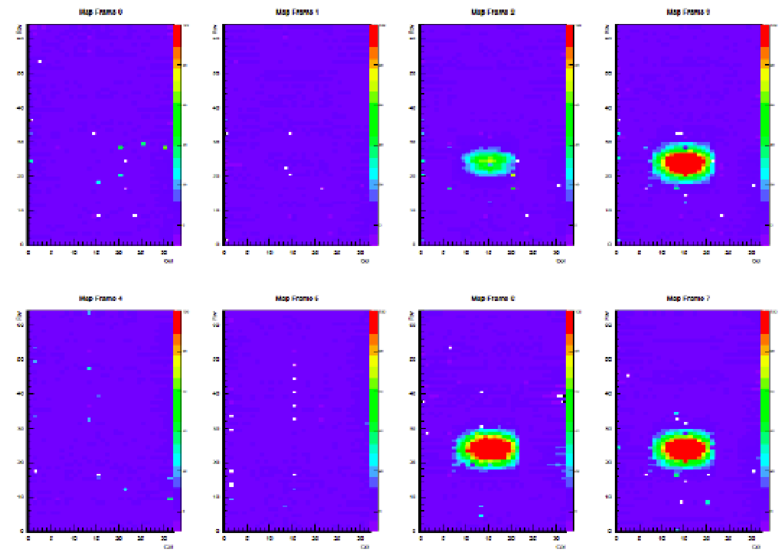




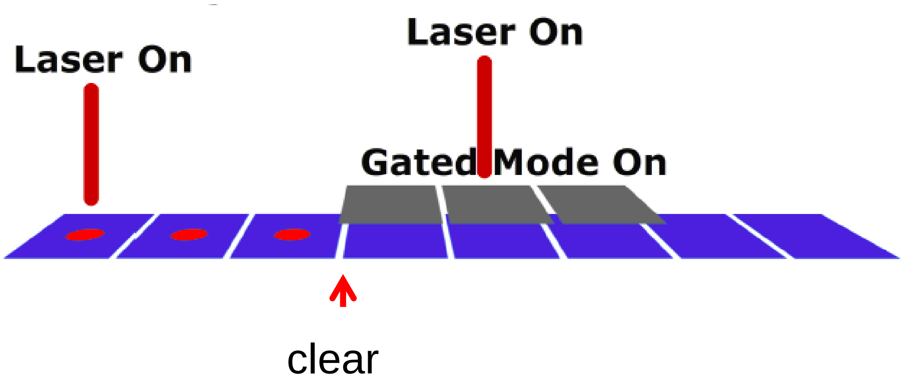
Test with laser

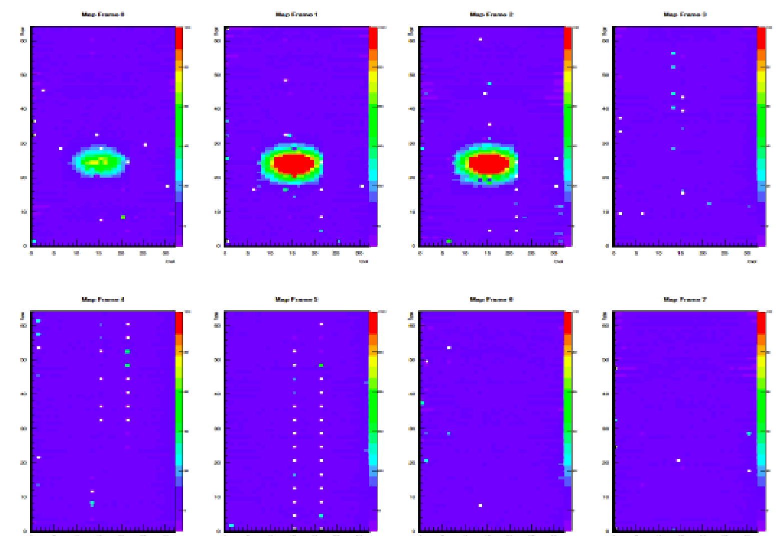
Protection of signal charge





Rejection of backround charge



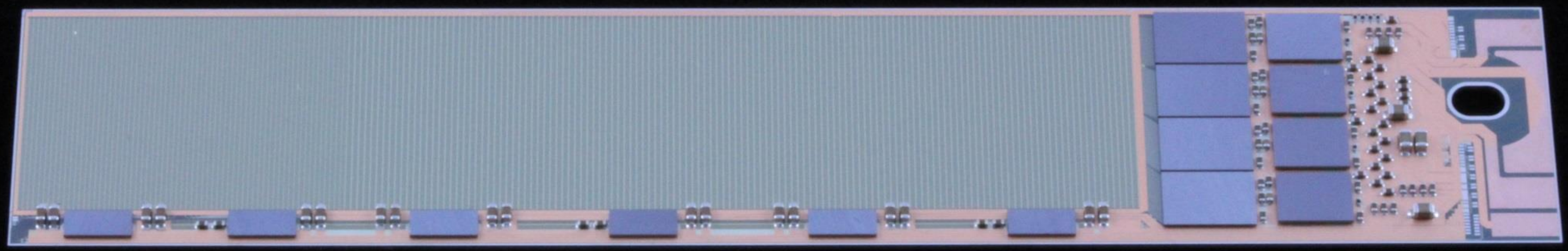


Conclusions & Status

The Belle II Detector at SuperKEKB will be equipped with a DEPFET pixel detector

75 µm active silicon thickness, 0.21% X0

Production of 30 wafers with 6 modules each (one inner ladder, two outer ladders)
All wafers processed up to metal 1
3 'pilot' wafers finished (metal 1-3, thinning and cutting)
3 modules equipped with ASICs and SMD



This month: tests in the lab and with beam

Completion of 27 remaining wafers in 2016

BEAST II test detector (2 ladders + SVD ladders + rad detectors) in Belle II in 2017

Installation of final PXD detector end of 2017

First physics beam in 2018