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Study of built-in amplifier performance on HV-CMOS sensor for the ATLAS Phase-II Strip Tracker Upgrade

Saturday 26 September 2015 19:16 (1 minute)

The presentation will focus on the performance of analog readout electronics (built-in amplifier) integrated on the high-voltage (HV) CMOS silicon sensor chip, as well as its radiation hardness.

Since a CMOS sensor has a ten times lower total collected charge from MIP than for conventional planar sensor, it is crucial to integrate a low noise built-in amplifier on the sensor chip to improve the signal to noise ratio of the system.

As part of the investigation for the ATLAS strip detector upgrade, a test chip that comprises several pixel matrices with different geometry, as well as standalone amplifier and built-in amplifier in pixel arrays has been fabricated in a 0.35 .m high-voltage CMOS process.

Measurements of the gain and the noise of both the standalone amplifiers and built-in amplifiers in pixel arrays respectively were performed before and after gamma radiation up to 100Mrad. A special interest is the variation of the noise as a function of the sensor capacitance.

We optimized the configuration of the amplifier for a fast rise time to adapt to the LHC bunch crossing period of 25 ns, and measured the timing characteristics including jitter.

Our results indicate an adequate amplifier performance for monolithic structures used in HV-CMOS technology. The results are incorporated in the next submission of a large-structure chip.

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Session Classification: After dinner POSTER session, with drinks: (All presenters are requested/encouraged to attend their posters; All participants are requested to participate the session, with drinks!)

Track Classification: Pixels (including CCD's) - Charged particle tracking