Charge collection and non-ionizing radiation tolerance of CMOS Pixel Sensors using the 0.18 μm CMOS process

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Outline

- Introduction
- Charge collection simulation
- Prototype design
- Summary and outlook

Introduction — CEPC

- **CEPC: Circular Electron Positron Collider, as a Higgs Factory, proposed by the Chinese high energy physics community in 2012.**

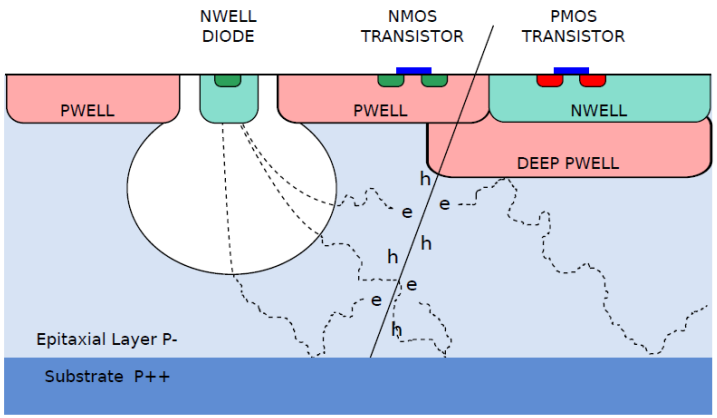
- **Stringent requirements on the vertex detector：**
  - Spatial resolution near the interaction point σ_{sp} ~ 3 μm → high granularity (small pixel size)
  - Material budget ≤ 0.15% X_0/layer → monolithic pixel sensors

    (sensor + embedded electronics, thinned down to e.g. 50 μm) + air cooling (power dissipation ≤ 50 mW/cm^2)
  - Low detector occupancy below 0.5% → fast readout (~ 20 μs) + high granularity
  - Radiation tolerance (pre.): Total Ionizing dose ~1 MRad/y

    Non-ionization energy loss ~10^{12} n_{eq}/cm^2/y
- **Sensor options:** many technologies from ILC/CLIC could be options, i.e. **CMOS Pixel Sensor (CPS),** SOI, DEPFET, 3D, etc.

  But, power pulsing will NOT work at the CEPC → low power consumption

Introduction — CMOS Pixel Sensor



ALICE ITS Upgrade TDR 2013

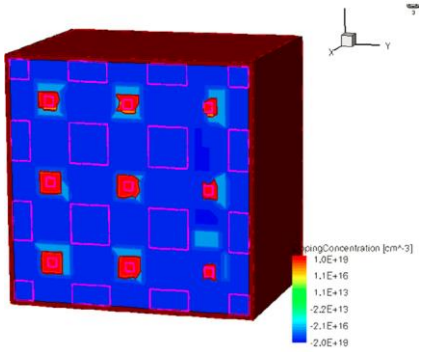
- **Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process → low material budget, low power consumption, low cost …**
- **Ultimate (Mimosa 28) installed for STAR PXL, technology for ALICE ITS Upgrade**

- **Selected TowerJazz 0.18 µm CIS technology for R&D, featuring:**
  - Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area
  - Feature size of 0.18 µm and 6 metal layers: high-density and low power
  - Thick (18 – 40 µm) and high resistivity (≥1 kΩ•cm) epitaxial layer
  - Thin gate oxide (< 4 nm): total ionizing dose

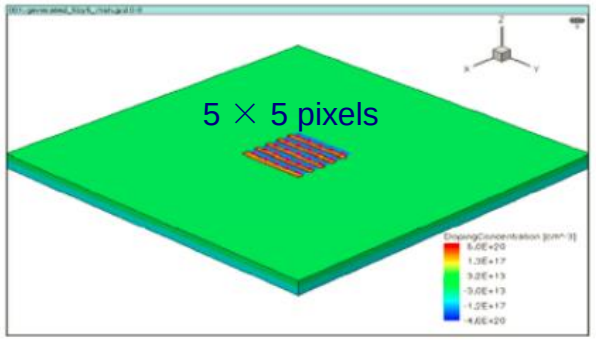
Charge collection simulation

- **Motivation:**
  - Guide the diode geometry optimization and study radiation damage with different types of epitaxial layer
- **Simulated structure**
  - Building the 3-D device structure with Sentaurus-TACD tool
  - Setting boundary: extending the auxiliary silicon surrounding the device volume to hundreds of micro-meters, which approximates the real device condition, replacing:
    - **Reflective boundary condition (default) → overestimated signals.**
    - Introducing four **SiO_2 belts surrounding the detector** volume and **artificially high recombination velocity** at the interface → **unreliable result**.

Simulated structure using SiO2 belts



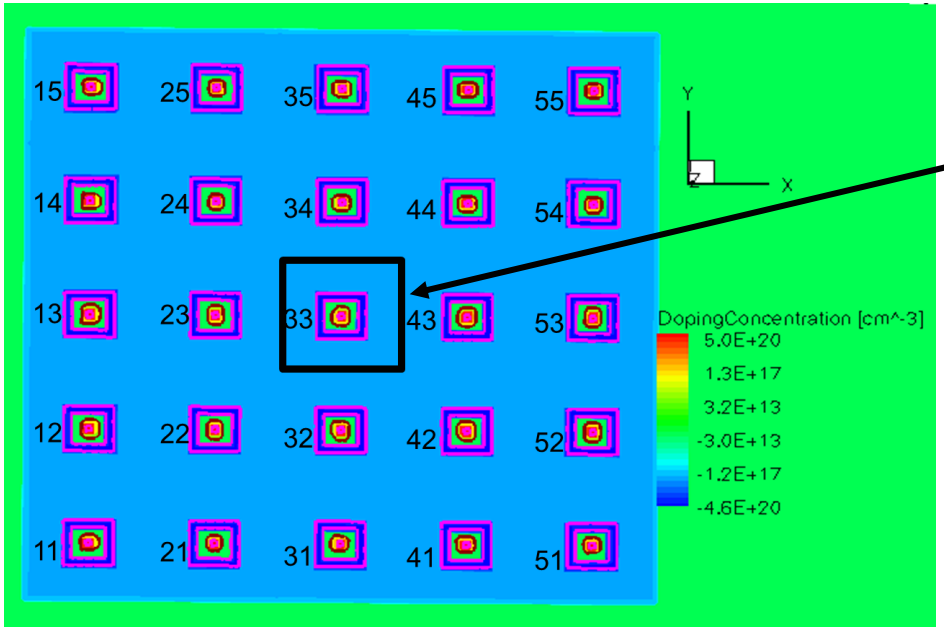
Simulated structure in this work



Charge collection simulation

- **Simulation with different parameters**
  - Hit position
  - Diode geometry
  - Thickness and resistivity of the epitaxial layer
  - Radiation damage

Top-view of the simulated 5 × 5 cluster

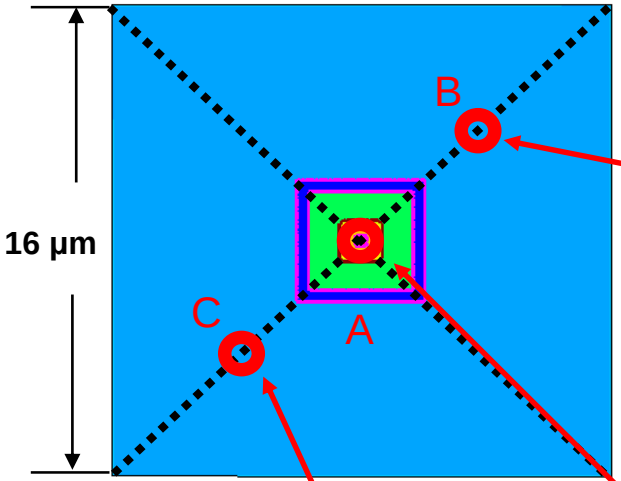


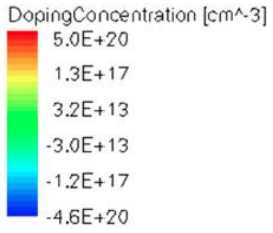
Shooting MIP particle vertically at the central pixel and calculate the collected charge in neighboring pixels

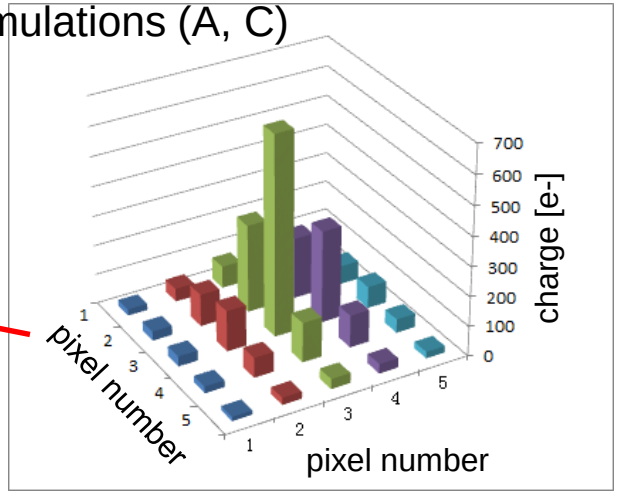
pixel size: 16 μm × 16 μm

Charge collection vs. hit position

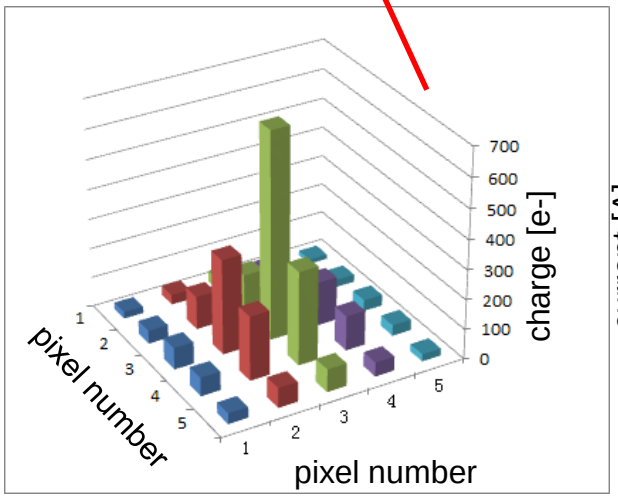
- **The symmetrical pixel model makes the charge collection distribution symmetrical**
  - Two different hit positions selected in the following simulations (A, C)

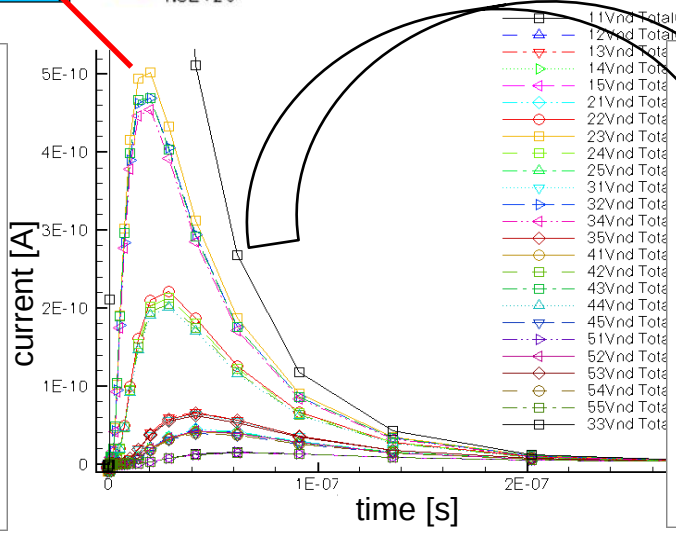


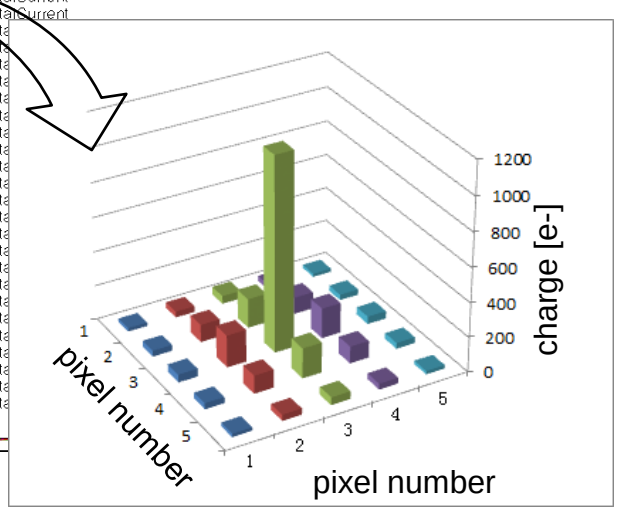




integrating current



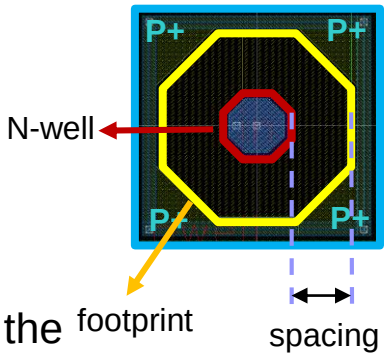


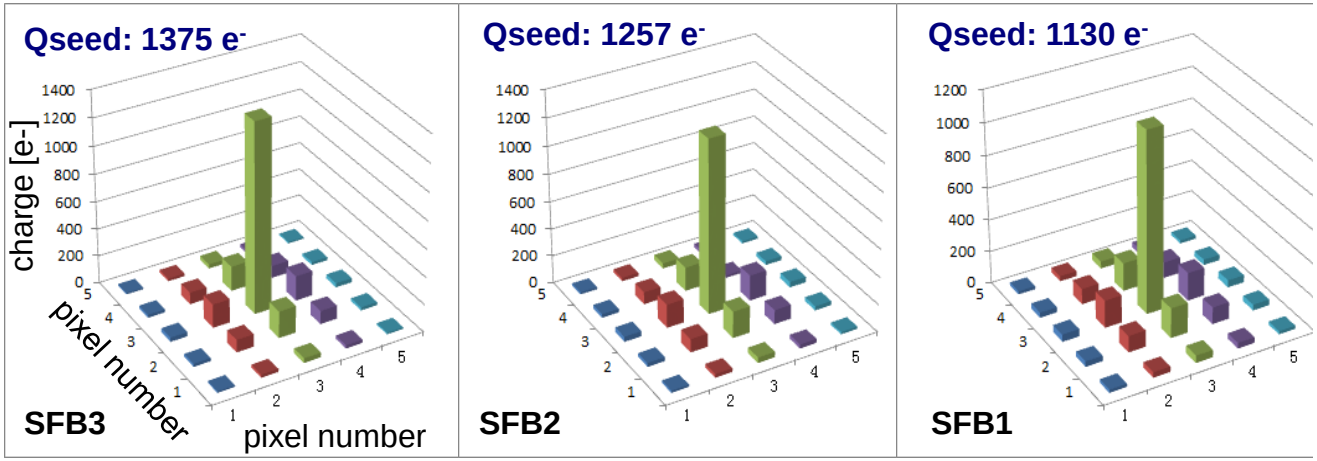


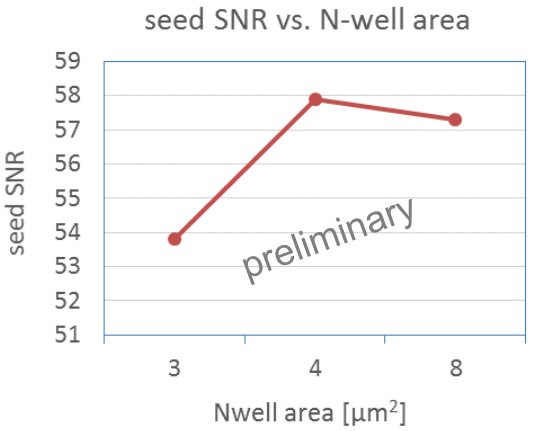
Charge collection vs. diode geometry

- **Design remarks on sensing diode area**
  - should be small for the sake of low C, low noise, high gain

    because $V_{sig} = Q_{coll}/C$; $N \propto C$
  - BUT not too small to preserve charge collection efficiency (important against NI irradiation)
  - spacing (free of p- and n-wells) between the diode n-well and the surrounding p-well affects CCE







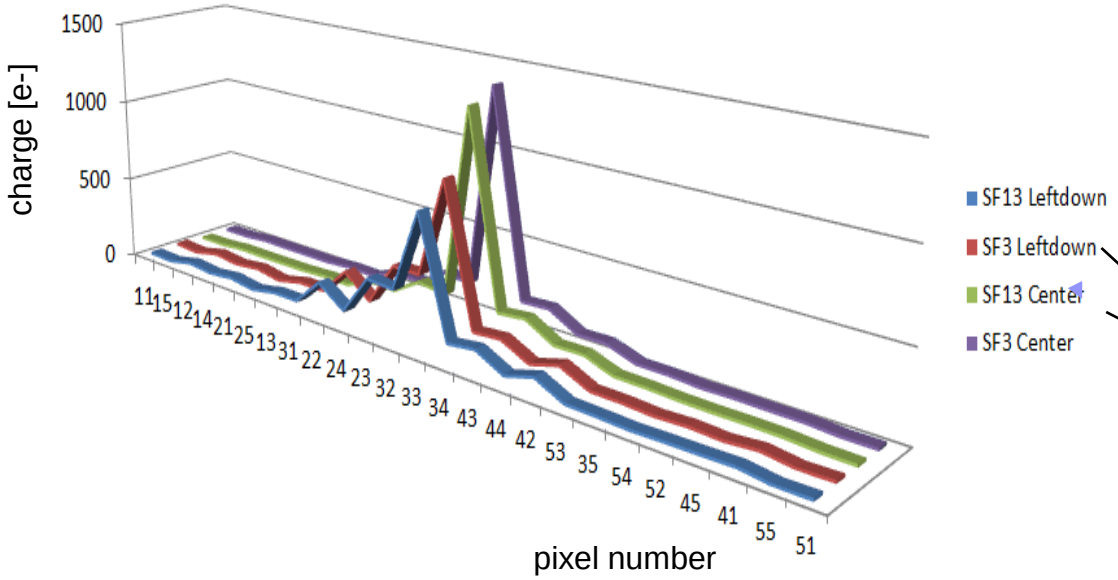
SFB1/2/3 pixel have the same area of footprint, but different area of N-well, SFB3 > SFB2 > SFB1

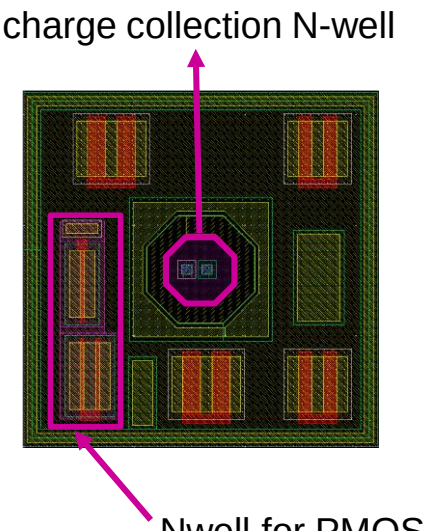
The collected charge of seed pixel increase with N-well area, but SNR does NOT

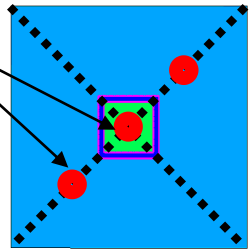
Charge collection with competitive N-well

- **PMOS within the pixel introduces a competitive N-well to the charge collection N-well; using the deep P-well is expected to shield the competition**

Sector	Diode area	Footprint area	Structure
SFB3	8 μm²	20 μm²	2T_nmos
SFB13	8 μm²	20 μm²	2T_pmos





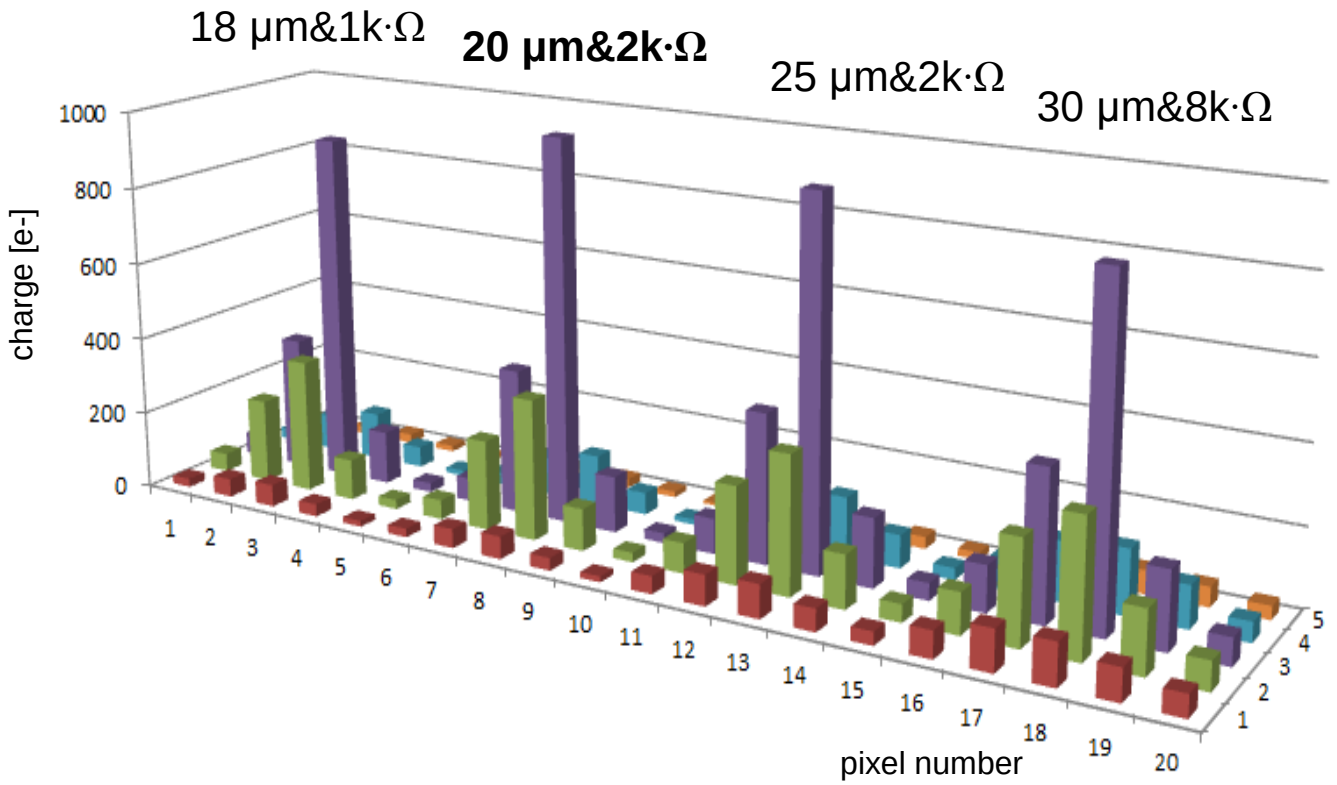


hit position on the central pixel

With the shielding of deep P-well, the competition of PMOS on charge collection is almost negligible ➔ allow full CMOS within the pixel

Charge collection with different epitaxial layers

- **Pixel cluster with four different epitaxial layers**
  - With the same pixel structure (SFB3)



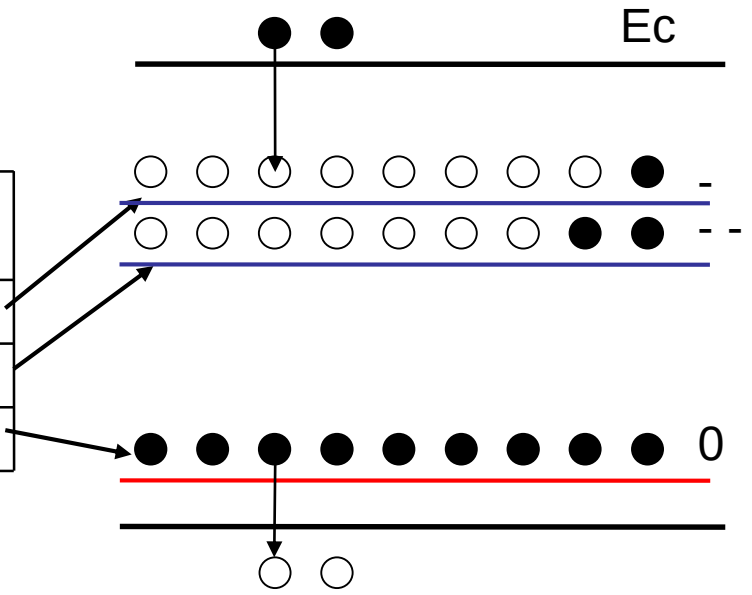
Total charge increases with the thickness and resistivity of the epi-layer, so the charge sharing → figure out an optimal configuration

Radiation damage simulation

- **Radiation damage can be simulated in Sentaurus Device by modelling behavior of trap levels directly**
- **Perugia P-type model**
  - 2 Acceptor levels: Close to midgap
    - Leakage current, negative charge (Neff), trapping of free electrons
  - Donor level: Further from midgap
    - Trapping of free holes

Perugia radiation damage model for P-type*

Type	Energy (eV)	Trap	σ_e (cm^2)	σ_h (cm^2)	η (cm^{-1})
Acceptor	Ec-0.42	VV	$2.0*10^{-15}$	$2.0*10^{-14}$	1.613
Acceptor	Ec-0.46	VVV	$5.0*10^{-15}$	$5.0*10^{-14}$	0.9
Donor	Ec+0.36	CiOi	$2.5*10^{-14}$	$2.5*10^{-15}$	0.9



IEEE Trans. Nucl. Sci., vol. 53, pp. 2971–2976, 2006

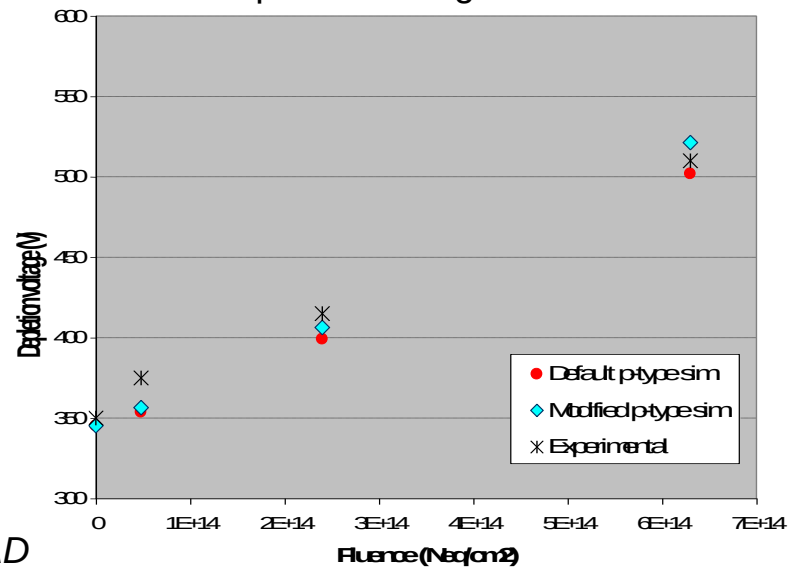
Radiation damage simulation

- **Modified P-type model used in this work**
  - Depletion voltage matches experiment

Modified P-type model[+]

Type	Energy (eV)	Trap	σ_e (cm^2)	σ_h (cm^2)	η (cm^{-1})
Acceptor	Ec-0.42	VV	$9.5*10^{-15}$	$9.5*10^{-14}$	1.613
Acceptor	Ec-0.46	VVV	$5.0*10^{-15}$	$5.0*10^{-14}$	0.9
Donor	Ec+0.36	CiOi	$3.23*10^{-13}$	$3.23*10^{-14}$	0.9

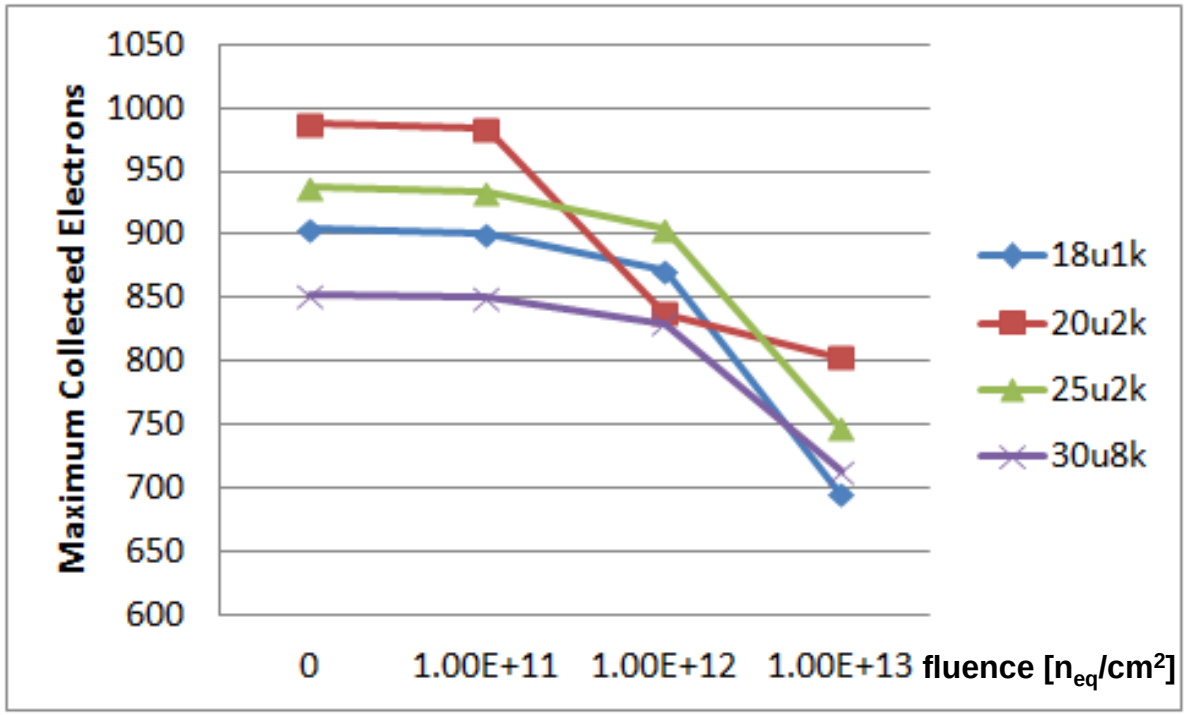
Depletion voltage vs. fluence[+]



[+]*David Pennicard, Radiation Damage in Sentaurus TCAD*

Charge collection with radiation damage

- 4 irradiation fluence with 4 epitaxial layer



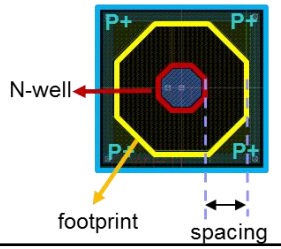
The performance requires further investigation

Prototype design

- **Goal：sensing diode optimization**

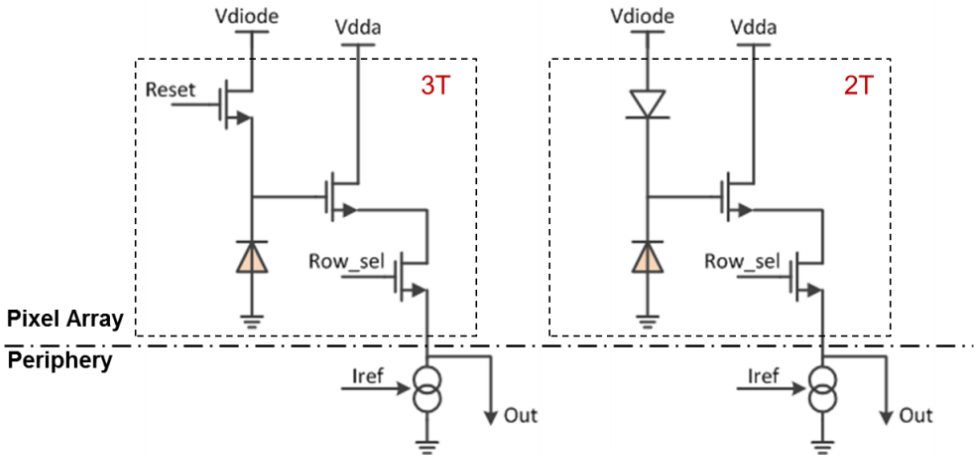
  ➔ improves SNR ➔ enhances detection efficiency

- **Design remarks：**
  - includes 16 pixel configurations
    - diode area, footprint
    - pixel structure
    - transistor type



Sector	Diode area	Footprint	Structure
SFB1	3 μm^2	20 μm^2	2T_nmos
SFB2	4 μm^2	20 μm^2	2T_nmos
SFB3	8 μm^2	20 μm^2	2T_nmos
SFB4	3 μm^2	15 μm^2	2T_nmos
SFB5	4 μm^2	15 μm^2	2T_nmos
SFB6	8 μm^2	15 μm^2	2T_nmos
SFB7	3 μm^2	11 μm^2	2T_nmos
SFB8	4 μm^2	11 μm^2	2T_nmos
SFB9	8 μm^2	11 μm^2	2T_nmos
SFB10	3 μm^2	8 μm^2	2T_nmos
SFB11	4 μm^2	8 μm^2	2T_nmos
SFB12	8 μm^2	8 μm^2	2T_nmos
SFB13	8 μm^2	20 μm^2	2T_pmos
SFB14	4 μm^2	8 μm^2	2T_pmos
SFB15	8 μm^2	20 μm^2	3T_nmos
SFB16	4 μm^2	8 μm^2	3T_nmos

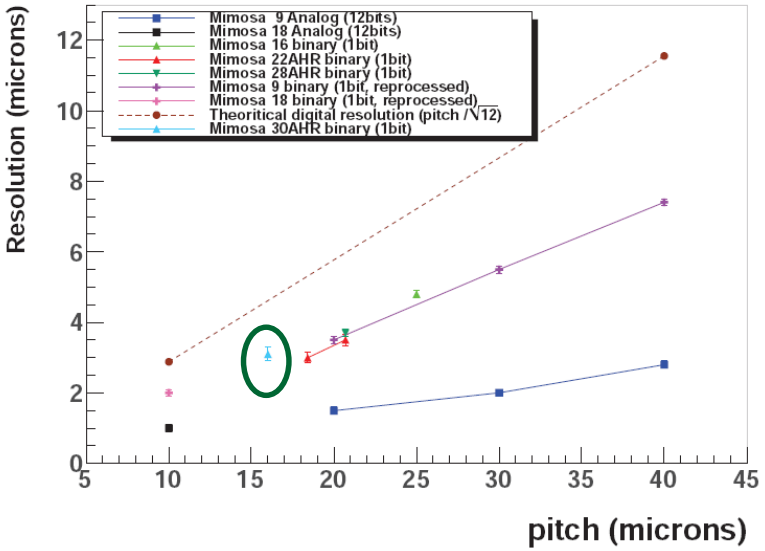
Source Follower (SF) pixels



Prototype design (continued)

- **Design remarks：**
  - Influence of pixel pitch
    - pixel size affects resolution, CCE and radiation tolerance
    - innermost layer σ_{sp} ~ 3 μm ➔ pitch ≤16 μm (binary readout)
    - including 2 pixel sizes: 16 μm × 16 μm, 33 μm × 33 μm
  - Remarks on depletion voltage
    - Apply highest possible voltage on sensing diode
    - Apply reverse substrate bias
      - reduces capacitance
  - Influence of thickness and resistivity of the epitaxial layer
    - Including four types of epi-layer:
      18 μm +1 kΩ·cm; 20 μm + 2 kΩ·cm; 25 μm + 2 kΩ·cm; 30 μm + 8 kΩ·cm

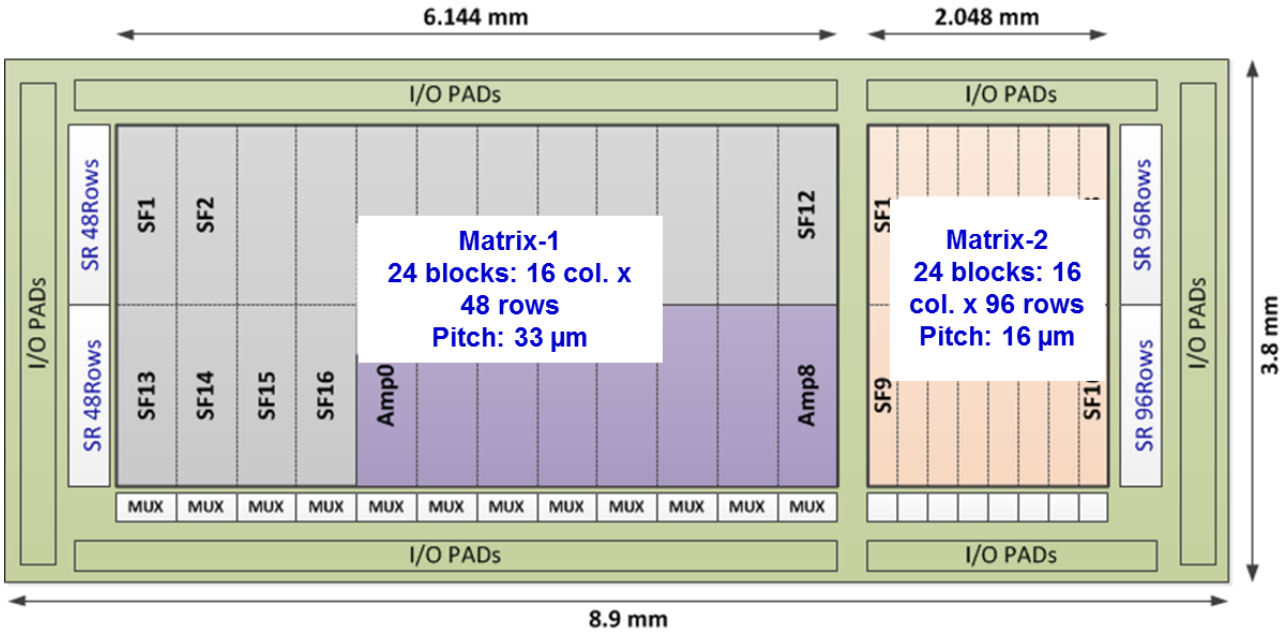
spatial resolution vs. pixel pitch



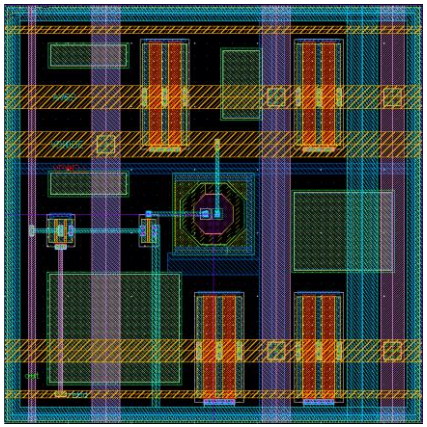
Y. Voutsinsa, et al., Vertex Detectors 2012

Prototype design (continued)

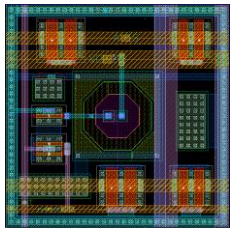
- **Chip floor plan**
  - Contains two matrices, Matrix-1 with 33 × 33 μm² pixels, Matrix-2 with 16×16 μm² pixels. Each matrix includes 16 SF (source follower) blocks for sensor optimization
  - Each block has 16 parallel analog outputs (16 columns)
  - Matrix-1 includes 8 blocks with in-pixel pre-amplifier



33 μm pixel

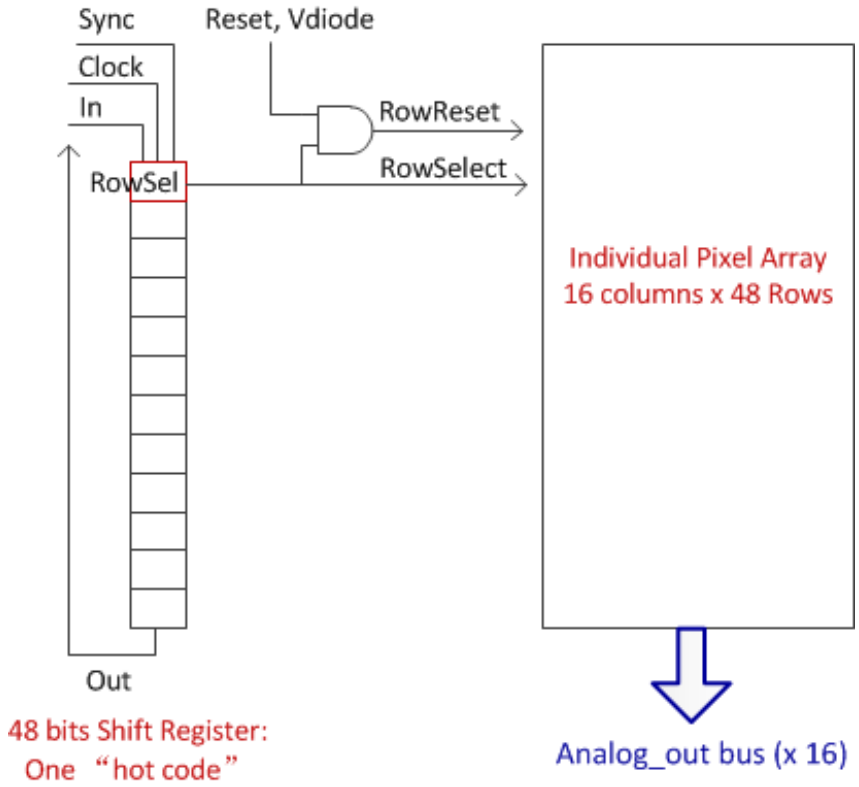


16 μm pixel



Prototype design (continued)

- **SF pixel array steering：**
  - selecting one row, 16 columns read out in parallel
  - each row needs one clock cycle，readout time of a frame is 24 μs @ 2MHz



Summary and outlook

- **Performed preliminary TCAD simulation to understand the impacts on charge collection, including:**
  - collection diode geometry
  - epitaxial layer
  - non-ionizing radiation damage
- **First prototype designed with the TowerJazz 0.18 μm CIS technology; TCAD simulation results to be verified with future measurements**

- **To include more pixel geometries and ionizing radiation damage effects in simulation**
- **First submission expected mid of October, followed by detailed charge collection efficiency measurements**

Thanks for your attention !

Charge collection with radiation damage

- **4 irradiation fluence with 4 epitaxial layer**