Development of n-in-p pixel modules for the ATLAS upgrade at HL-LHC

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Introduction

- Performance of n-in-p planar pixel sensors with different thickness:
  - Charge collection
  - Hit efficiency
  - Power dissipation

- Optimization of punch-through structures based on beam-test studies

- Pixel sensors designs with 50 µm x 50 µm pitch for new chips in 65 nm technology under development by the RD53 Collaboration

- Performance studies of FE-I4 modules inclined at high-\(\phi\) to simulate the operation of 50 µm x 50 µm pixels at high pseudo-rapidity
Thin n-in-p pixel sensor production at VTT

- n-in-p pixels on FZ and MCZ material
- 100 µm and 200 µm thickness
- Flip-chipping performed at VTT after removal of support wafer

- 125 µm edge implemented in FE-I3 and FE-I4 sensors
- 50 µm implemented only in FE-I3 sensors
Charge collection properties of thin n-in-p pixel sensors

Charge collection after irradiation for 100 μm thin sensors

Charge collection after irradiation for 200 μm thin sensors

S. Terzo Ph.D. thesis, TUM
Pixel performance as a function of thickness

At $\phi=(4-6) \times 10^{15}$ $n_{\text{eq}} \text{cm}^{-2}$ FE-I4 modules with 150 and 200 $\mu$m thick reach hit efficiencies of about 97% at $V_{\text{bias}}=500$V.

FE-I4 modules with 100 $\mu$m with thick sensors start to saturate to this value already at $V_{\text{bias}} = 250-300$V.

Lower operational bias voltages result for thinner sensors in an improvement in the power dissipation performance.

S. Terzo Ph.D. thesis, TUM
Limiting effects on hit efficiency at high fluence

- Hit efficiency measured with ADVACAM sensors, 100 µm thin, interconnected to FE-I3 and FE-I4 chips
- Average hit efficiency lower for FE-I4 compatible sensors with respect to FE-I3, due to the fact that the Punch Through Structure occupies a higher fraction of the pixel cell area

**Graph:**
- Hit efficiency [%] vs Bias voltage [V]
- Points for different thicknesses and fluences:
  - FE-I4 100 µm, \( \Phi = 2 \)
  - FE-I3 100 µm, \( \Phi = 5 \)
  - FE-I4 100 µm, \( \Phi = 5 \)

**Legend:**
- Full pixel area
- Central pixel area
- \( [\Phi] = 10^{15} \) n_{eq}/cm^2

**Beam tests:**
- Beam test at CERN-SPS with 120 GeV pions
- Beam test at DeSY with 4 GeV electrons

**Dimensions:**
- FE-I3 module, \( \Phi = 5 \times 10^{15} \) n_{eq} cm\(^{-2} \), 300V
  - 50 µm x 400 µm
- FE-I4, 500V
  - 50 µm x 250 µm
Production of n-in-p pixels on 6” wafers at CIS

- First 6” wafer production at CIS on p-type material, 16 kΩ cm
- Wafer thickness 265-270 μm (thinning and polishing performed at Rockwood)
- FE-I4 Single chip sensors with different cell design plus FE-I4 quad modules

FE-I4 sensor with three different punch-through structures implemented in groups of 10 columns, standard pitch 50 μm x 250 μm

FE-I4 sensor with punch-through structure common to four pixels, pitch 25 μm x 500 μm

- Project partially funded by RD50
- BCB coating for sensor-chip isolation and interconnection to FE-I4 chips performed by IZM-Berlin
Optimization of the Punch Through Structure

- Results of beam test performed at DESY with 4 GeV electrons
- Single chip module irradiated at KIT with 25 MeV protons at a fluence of $3 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
- Common punch-through structure to four pixels optimized for small pitches

![Diagram of punch-through structure](image)

- Common PT for four pixels, $25 \times 500 \mu m^2$ pitch
- Standard PT, $50 \times 250 \mu m^2$ pitch

Test-beam data analysis by N. Savic
Comparison of performance of different punch-through designs

CIS3 sensors (270 um thick) irradiated at $3 \times 10^{15}$ $n_{eq}$ cm$^{-2}$ at KIT
Comparison of performance of different punch-through designs

CIS3 sensors (270 um thick) irradiated at $3 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$ at KIT

Highest eff. for common PT at 500V = $(99.4 \pm 0.3)\%$
New design for sensors compatible with the RD53 chip

- New read-out chip for the future generation of pixel modules developed by the RD53 Collaboration
- 50 µm x 50 µm pitch for the chip, probably with bumps placed on a regular grid

- Two different versions of sensors for RD53A chip with 50 µm x 50 µm pitch:
  - Common punch – through with bias rail running over implants to minimize hit efficiency loss after irradiation
  - Without any bias rail structure → not measurable before interconnection to the chip
Sensors compatible with 65 nm CMOS

- **25x100 µm² pitch**

- Pixel staggered in such a way to be compatible with a regular 50x50 µm² grid on the chip side
- Still realizable with a standard UBM size = 20 µm
- Design based on an existing prototype produced at CIS with 25 x 500 µm² pitch, FE-I4 compatible

- No increase of cross-talk observed in 25x500 µm² FE-I4 compatible sensors:
  - direct measurements with ATLAS RCE read-out system
  - Analysis of cluster size in beam test data
Hit efficiency for 50 μm pitch at high pseudo-rapidity

- **Aim:** study the performance of 50x50 μm² pitch sensors at high η

- **Solution:** use FE-I4 modules at high φ (80° → η=2.5) almost parallel to the beam but rotated by 90° with respect to their normal pixel orientation in the detector

- **Samples:** 100 μm thick planar sensor (VTT)

- **No tracking information from EUDET telescope used (problems encountered in reconstruction)**

- **Very long cluster expected along z for high φ = 80° (η=2.5), use them as “tracks”**
Performance at high $\eta$: Cluster Multiplicity

- Module Tuning:
  - Threshold 1 ke
  - Charge calibration 6 ToT at 4 ke
- Measured cluster width in Y (along 50 $\mu$m pitch direction) 2-3 units less than pure geometrical expectations
- Difference is due to ~1 degree misalignment and threshold effects in the entrance and exit pixels

$$\epsilon_{\text{pix}} = 1 - \sum_{c=1}^{N} \frac{h_{\text{miss}}^{c}}{w_{x}^{c} - 2}$$

Good single hit efficiency with 100 $\mu$m thin sensors with 50 $\mu$m pitch: $(99.6-99.7)\%$
Performance at high pseudo-rapidity after irradiation (I)

- Study the performance of planar pixel modules after irradiation in a beam test at DESY with 4 GeV electrons
- FE-I4 module, CIS production, irradiated to a fluence of $2 \times 10^{15} n_{eq} \text{cm}^{-2}$
- Same inclination as not-irradiated one, high $\phi = 80^\circ$ ($\eta=2.5$)

- Cluster width distribution from 200V to 800V
- Expected cluster size from geometry ~24 due to the double sensor thickness than in the previous study
- Maximum separation of 10 pixels allowed in the analysis
Performance at high $\eta$ after irradiation (II)

- Grazing angle technique is also a powerful method to investigate charge collection at different depths of irradiated sensors.
- Charge collection vs pixel number and depth at 300 V up to 800 V for a cluster width of 24.
- Module tuned with a threshold of 1000e.

Before irradiation constant charge is observed at different depths except for the entrance and exit pixels, where pixels are only partially crossed.
Performance at high $\eta$ after irradiation (III)

- Grazing angle technique is also a powerful method to investigate charge collection at different depths of irradiated sensors.

- Charge collection vs pixel number and depth at 300 V up to 800 V for a cluster width of 24.

- Module tuned with a threshold of 1000e.

- Single pixel hit efficiency for cluster size=24 at different bias voltages.

- (81.5-93.4)% single hit efficiency for the $V_{\text{bias}}$=800V in the full depth range.
Summary and Outlook

- Excellent performance of thin n-in-p pixel sensors demonstrated before and after irradiation up to a fluence of $5 \times 10^{15} \text{n}_{\text{eq}} \text{cm}^{-2}$

- Design of pixel sensors compatible with RD53 chip has been optimized based on beam test analysis of different biasing structures

- Tracking with 50x50 $\mu$m$^2$ pitch at high eta investigated by using FE-I4 pixel modules at high-$\phi$ before and after irradiation. This technique also provides a tool to study charge collection at different depths in the silicon bulk

- Productions of thin n-in-p pixel sensors are on-going at CIS (100-150 $\mu$m thickness) and ADVACAM (50-100-150 $\mu$m thickness) to expand the irradiation and testing program up to a fluence of $10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$
Additional material
Possible effects of timing on charge distribution

- Charge collection properties at different depths probably slightly affected by time-walk effects due to different carrier velocity and longer collection path for electrons.

- Slower signals close to the backside causes later crossing of pixel threshold and a decrease of ToT values. This is also visible in a higher average value of the Level1 distribution close to the backside (delay in unit of 25 ns with respect to the trigger signal).

![Graph showing possible effects of timing on charge distribution.](image-url)
Quad sensors and SCMs

- 4 rows of ganged pixels
- Standard punch-through structures
- 3 rows of ganged pixels
- Common punch-through structures for 4 pixels
- FE-I4 SCM with reduced GR structures
On-going productions of thin n-in-p pixel sensors

- Explore the thickness range 50-150 µm to investigate the optimal thickness for the different pixel layers
- Compare different processing methods
- Test new pixel cell designs with common PT structures
New thin production at CIS - Technology

- relatively simple technology without using support / handling wafers
  - anisotropic wet etching (KOH) on <100> wafers
  - Experience with this technology at CIS for MEMS/pressure sensors production

- First R&D production on 4” p-type FZ wafers; process contributed by CIS; target thickness 100 and 150 µm

- Starting thickness 525 µm

- Front-side processing up to nitride deposition and patterning

- Back-side p+ implantation, top-side p-spray → common annealing step

- Metallization on the front and back side

- UBM (electroless Nickel at CiS or standard one at IZM)

- dicing
New thin production at CIS - Technology

- relatively simple technology without using support / handling wafers
  - anisotropic wet etching (KOH) on <100> wafers
  - Experience with this technology at CIS for MEMS/
    pressure sensors production

Completion expected at the end of November 2015
Second production of active edge pixels at ADVACAM

**Wafer layout of the new production**

- **6” SOI wafers**: active edge process for all the structures
  - In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD,
  - Geneva University for medical applications
- 50, 100, 150 µm sensor thickness: 5 FZ p-type wafers for each thickness
FE-I4 Single Chip Modules

**FE-I4 with 50 µm edge, one GR, no punch-through structure**

**FE-I4 with 100 µm edge, Bias Ring, new external punch-through structure**

**FE-I4 with 100 µm edge, Bias Ring + Guard Ring, std punch-through structure**

**FE-I4 with 100 µm edge, Bias Ring, std punch-through structure**