

From 2010-2014 the EU funded AIDA-WP3 project invest established a network of groups working collaboratively on advanced 3D integration of electronic circuits and semiconductor sensors for applications in Particle Physics. The main motivation came from the severe requirements on pixel detectors for tracking and vertexing at future Particle Physics experiments at LHC, Super-B factories and Linear Colliders. To go beyond the state-of-the-art, the main issues are studying low mass, high bandwidth applications, with radiation hardness capabilities, with low power consumption, offering complex functionality, with small pixel size and without dead regions. The interfaces and interconnects of sensors to electronic readout integrated circuits are a key challenge for new detector applications.

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## INTRODUCTION

The main objective of AIDA WP3 [1] was the demonstration of the feasibility of 3D interconnection for applications in Particle Physics. This was the to be achieved by the fabrication of pixel detectors and readout electronics, interconnected by advanced 3D integration technologies. WP3 was pursuing different technological approaches to 3D integration; depending at what stage the TSVs (Through Silicon Vias) are fabricated. These approaches can be categorized in the "via last" (vias are etched and filled during the CMOS processing) and "via first/middle" techniques (vias are processed after the completion of the CMOS processing). Also, the pitch of the bonding interconnection between the layers of these 3D devices may vary from moderately large values (of the order of 100  $\mu\text{m}$ ) to more aggressive ones (from a few tens of  $\mu\text{m}$  down to few  $\mu\text{m}$ ). Different applications drive the choice of a more or less dense version of 3D integration.

3D integration is driven by several motivations in order to improve the performance of sensors used in particle physics. One is the optimisation of the routing of the service connections of the sensors. Classical hybrid pixel sensors have their I/O pads on the sensors (= front) side making the connection difficult and resulting in large dead space and material overhead. This can be solved by routing the I/O contacts to the back side of the readout electronics which can be accomplished using few vias at the periphery of the chip. In this case interconnection density is low and large diameter vias can be used.

A more challenging goal is the reduction of the pixel size. This needs high interconnection density (sensor – readout) and reduces the area available for in pixel readout circuitry. Additional space can be gained by stacking layers of electronics on top of each other. This has the additional advantage that different technologies optimized for different tasks (sensing, analogue amplification, digital data processing) can be used. In these cases high density interconnection technology and low diameter vias are required.

## Subprojects of AIDA WP3

The AIDA project was structured in 7 sub-projects each investigation a different technological approach to 3D integration:

1. Interconnection of the ATLAS FE14 chips to sensors using bump bonding from IZM (large interconnection pitch) (Bonn University and CPPM, Marseille).
2. Interconnection of MEDIPIX3 chips to pixel sensors using the CEA-LETI process (CERN, Geneva).
3. Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (Tohoku-Microtec or others) (NFN Pavia and IPHC-IRFU Strasbourg).
4. Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process (LAL, LAPP, LPNHE and MPP).
5. Interconnection of ATLAS FE14 chips to sensors using SLID interconnection from EMFT (MPP Munich, Glasgow, LAL Orsay; Liverpool and LPNHE).
6. 3D interconnection of 2 layers of Geiger-Mode APD arrays with integrated readout in Tezzaron Chartered technology (University of Barcelona).
7. Interconnection of the two layers of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology (RAL, Uppsala).

Some of these projects used almost mature technologies while others focused on more challenging approaches which have more risks but on the other hand pave the way for more advanced possibilities in future applications. While CEA-LETI and IZM offer rather mature processes possible for large pitch detectors and large diameter TSVs to be used at the chip periphery, EMFT and T-MICRO processes aim for a smaller interconnection pitch and fine, high aspect ratio TSVs which could eventually be used in the central pixel area of a chip. All these processes are via last, with the via etching done in a post processing step on (almost) standard ASICs. Tezzaron is the only vendor offering a via first/middle process with the via etching being integrated in the ASIC fabrication process. These sub-projects will be described in more detail in the next sections. As discussed in the following, some of them also had to adjust their goals, taking into account the availability and the reliability of 3D technologies and their evolution during AIDA.

## 1. Bonn/CPMM

The goal of this activity was to develop a 3D integration technology applicable to the innermost pixel layer of the ATLAS detector at High Luminosity LHC. The Bonn/CPMM sub-project proposed to produce real chip/sensor assemblies to test an interconnection technique allowing the access to the wire bond pads of the 3D structures after flip chip bonding.

This was accomplished using a via last TSV process from IZM on ATLAS FE-13 pixel readout wafers [2]. Processing of these tapered TSV (100 $\mu\text{m}$  diameter) at wafer level was successfully achieved (Fig. 1). Demonstrator modules featuring planar sensor bump bonded to 90 $\mu\text{m}$  thin FE-13 with TSVs were built. The operation of TSV modules using the connection on the back-side of the chip, i.e. the TSV interconnection, was demonstrated for the first time in HEP.



Fig. 1: Cross section of a tapered via etched into a FE13 chip. The outer diameter is about 100 $\mu\text{m}$ . The connection to the metal circuitry of the chip is achieved by a Cu-plug

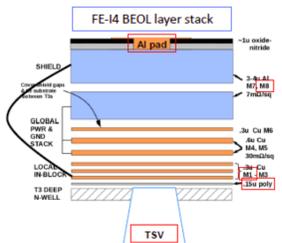


Fig. 2: The FE14 chip has the M8 metal layer (with the bon pads) connected to M1. Hence the TSV can be connected directly to this layer without need of a plug.

As next step, IZM is currently processing the new generation ATLAS pixel readout chip for the IBL and HL-LHC, the FE-14B. The FE-14B wire bonding pads have been designed TSV compatible so that a front-side processing step will not be needed. This is unlike the process of the FE13 where a copper plug had to be placed in the via to connect it to the chip's circuitry (Fig. 2).

## 2. CERN

The project used Medipix3 chips as the platform for 3D integration development. The aim of the project was to utilize an existing mature TSV technology made available by CEA-LETI as a part of their open 3D initiative. The LETI via-last process offers vias of about 40  $\mu\text{m}$  diameter and 3:1 aspect ratio (Fig. 3).

The post-processing at CEA-LETI was performed on wafers with the Medipix3 chips. CERN has received full assemblies of ASICs with pixel sensors from VTT/ADVACAM. In an X-ray imaging laboratory experiment, the CERN team was able to correctly read out via LETI TSVs a 110  $\mu\text{m}$  thick Medipix3.1 chip bump bonded to a 300  $\mu\text{m}$  thick 'edgeless' Si sensor from ADVACAM (see flat field corrected image in Fig. 4). The chip had a full redistribution layer on the back side and it was mounted on a standard PCB. This development is a very important achievement as it points the way forward to tiling large areas seamlessly.

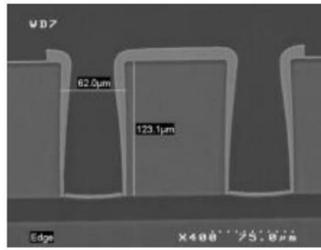


Fig. 3: Cross section of a via processed at CEA-LETI (Image courtesy CEA-LETI)



Fig. 3: Image acquired with a 110  $\mu\text{m}$  thick Medipix3.1 chip with LETI TSVs bump bonded to a 300  $\mu\text{m}$  thick 'edgeless' Si sensor.

A 2<sup>nd</sup> run with LETI proved that the process is able achieve a yield of ~50% for perfect chips. In a 3<sup>rd</sup> run the MEDIPIX chips were thinned to 50 $\mu\text{m}$  before the TSVs were successfully processed.

## 3. INFN/IPHC

The initial goal of the INFN/IPHC proposal in the framework of the AIDA WP3 was the design and fabrication of a three-tier pixel sensor resulting from the vertical interconnection of a dual-layer CMOS readout circuit to a third CMOS layer optimized for particle sensing or to a fully depleted edgeless or 3D detector [3].

The 3D front-end electronics consisted of an analog layer (including a charge preamplifier, an RC-CR shaper, a circuit for polarity selection, a discriminator and a DAC for threshold correction) and a digital layer (including logic blocks for data sparsification and a circuit for gain calibration) provided by Globalfoundries (CMOS 130nm) and interconnected by Tezzaron through copper-to-copper bonding and thermo-compression techniques. The design of the 128 x 32 matrix has been completed. Simulation results were compliant with application to small pitch (50 $\mu\text{m}$ ), low power pixel detectors in HEP experiments. This design appeared to be very appealing, because of the promising results obtained with a multiproject wafer run organized by the 3D-IC consortium before the beginning of AIDA [7]. Numerous chips were fabricated in this run, and, despite several fabrication problems, provided a proof-of-principle of the potential performance advantages associated with this 3D integration process. However, access to the technology, that was to be granted through a few brokers around the world (CMP in Europe, MOSIS in the US), was not actually provided during the time frame of AIDA.

Alternatively a preliminary test of the Tohoku-Microtec vertical integration process was performed on pre-existing readout chips (128x32 channels) and high resistivity n-on-n pixel sensors. The interconnected front-end chip/pixel detector pairs was tested with <sup>90</sup>Sr/<sup>90</sup>Y to evaluate the interconnection yield. The fraction of failing interconnection was found to vary considerably from chip to chip. In the four tested samples, respectively, 1%, 2%, 8% and 24% of the interconnections were found not to work properly. Despite the fact that Tohoku-Microtec is located in Japan, the entire process, including procedures, took about three months, of which about one half for device processing. Again the weak point of the project was the Tezzaron 3D integration process which was to be used for the fabrication of the front-end chip. The design of the chip, which was virtually ready for submission, could never be sent to the foundry.

Because of these problems IPHC and INFN agreed to change the scope of the project and perform small pitch interconnection tests with Fraunhofer IMS in Duisburg. Test vehicles were chips with CMOS sensors with MIMOSA-like analog readout electronics fabricated in an engineering run with Tower/Jazz. The plan is to fabricate a 3D structure with two layers of CMOS sensors with 10 mm pitch interconnections achieved by a SLID (Solid-Liquid InterDiffusion) process (Fig. 4)

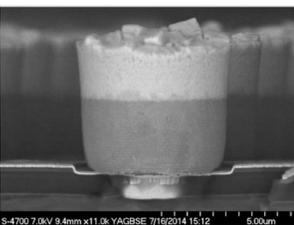
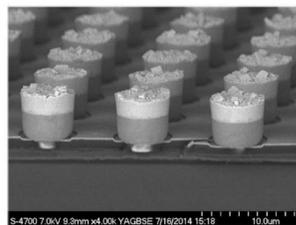


Fig. 4: Images of bumps for the SLID interconnection at IMS. The diameter of a bump is 5  $\mu\text{m}$ , the pitch 10  $\mu\text{m}$



## 4. LAL, LAPP, LPNHE

The original plan was to interconnect ASICs processed in TSMC 65nm technology to edgeless sensors produced by CIS and/or VTT. The chips should be processed with TSVs either in the periphery (for backside connectivity) or pixel by pixel (in case a high density via technology becomes available). Interconnection should exploit the possibilities offered by the vendor which, in case of CEA-LETI ranges from solder bonding with 50 $\mu\text{m}$  pitch to Cu-Cu thermocompression with much higher density. However, this was based on the assumption that TSMC 65nm will become available to the community through a CERN frame contract. Since this was delayed and accomplished only in mid 2014, the project could not be realized within AIDA.

## 5. MPP

Like sub-project 2 MPP aimed for the interconnection of the new FE-14 ATLAS chip to a compatible sensor by using 3D technologies developed by the Fraunhofer EMFT [4] in Munich. The interconnection is based on the SLID process by EMFT, which has the potential of leading to high density 3D devices, achieving 20  $\mu\text{m}$  pitch or less (Fig. 5). First studies of SLID with the ATLAS FE13 chip were successful, achieving 100% interconnected pixels (Fig. 6) [5].

However, in the TSV process the tungsten filling failed. In contrast to the FE13 the TSVs in the FE14 need to be connected to metal one. Unlike in the case of wide vias in project 2 it turns out to be difficult for the narrow large aspect ratio vias of EMFT. More R&D is required.

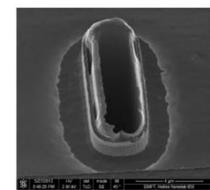


Fig. 5: Photo of a tungsten filled TSV by IZM. The dimensions are 10 $\mu\text{m}$  x 60 $\mu\text{m}$ .

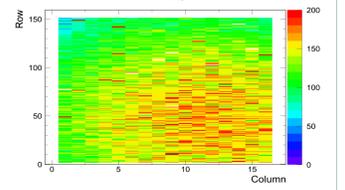


Fig. 6: Hit map of a pixel sensor connected to the FE13 chip using SLID interconnects. 100% of the interconnections work.

## 6. UB

This aim of this project was to increase the fill factor of Geiger mode APDs (GAPD) by interconnecting two tiers of GAPDs using the Tezzaron via first process. Though the design of the chip was ready it could not be completed due to the unavailability of the Tezzaron process.

## 7. RAL/Uppsala

The goal of this project was to fabricate 3DIC stacked ASIC with analogue and digital pixel readout cells interconnected using the Fraunhofer EMFT SLID process. Wafers with 40x40 pixel readout chips were built based on the existing Hexitec CZT readout circuitry [6]. A second digital chip contained an ADC in each pixel and the digital readout circuitry. There is one TSV interconnect from the analogue pixel on the top layer to the digital on the bottom layer and one for each I/O connection as all readout is from the top layer. The chips were tested separately and are fully functional.

EMFT has processed TSVs in these wafers up to the SLID interconnection level. EMFT delivered a wafer of SLID bonded ASICs. There are 9 chips on the wafer SLID bonded together. However, the full SLID wafer was visibly very poorly bonded and the yield appeared to be very low. Only 6 devices remained connected together after dicing but these did not look good visually.

In a different project a four-side-butable version of the Hexitec chip using rather large TSVs in the periphery. The vias had a diameter of 70  $\mu\text{m}$  and were etched in 120  $\mu\text{m}$  thick silicon. The TSV metal filling was copper connected to the Hexitec Al pad. The processing was performed by T-Micro in Japan. The assembly shown in Fig. 7 was successful. Some problems occurred due to a rather high contact resistance in the I/O pads and bending of the thinned ASICs.

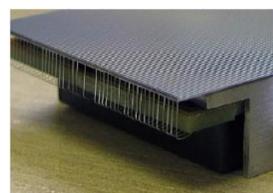


Fig. 7: Hexitec 4S chip with wirebond connections at the backside of the chip. TSVs connect these bonds to the I/O pads on the frontside.

## Conclusions

The WP3 sub-projects sampled different technologies with different challenges. It could not be expected that all of them progress at the same pace. Some sub-projects were investigating 3D technologies which have the potential to lead to high-density interconnection but still had technological challenges. Others used more mature technologies but opened viewer possibilities for improvements of the detector performance. Obviously those projects turned out to be the most successful ones. This was the case for the CERN subproject using a technology offered by CEA-LETI. Large diameter TSVs provided access from a metal redistribution layer on the backside to the chip's IO pads. Other subprojects focusing on similar technologies (large low aspect ratio vias at the periphery for backside connectivity) were quite successful as well (Bonn/CPMM using the FE13 chip with Fraunhofer IZM technology, RAL/Uppsala with T-Micro). Basically the TSV technology is available and can be applied as a via last technology to almost any ASIC. Here, interconnection technology is not a real challenge, standard bump bonding can do the job.

On the other hand, projects which aimed for high density interconnections with high aspect ratio, narrow vias were less successful. For the interconnection standard bump bonding had to be replaced by more advanced technologies. The SLID technology was tried in three projects with mixed results. A successful SLID interconnection could be demonstrated by the MPP project using a process by Fraunhofer EMFT. However the yield is low and results could not (yet) be reproduced by RAL/Uppsala using the same process. A third project (INFN/IPHC-IRFU) which uses a SLID technology by Fraunhofer IMS has not been evaluated yet. Equally narrow TSVs were used with mixed results. While EMFT failed with the tungsten filling of narrow vias in the MPP project the identical technology worked for RAL/Uppsala. This indicates that the process is not yet fully stable.

The most advanced 3D processes use via first technologies. Here one is bound to a specific ASIC technology and a vendor supporting this process. This was offered by Tezzaron. Since this was the most advanced technology accessible at the time it was mandatory within the framework of this project to assess this technology. A 'proof of principle' of the process could be achieved, nevertheless it became obvious that it is technically still very difficult and at the end it took more than four years to produce chips with very low yield [7].

Via last processes with large TSVs in the periphery are mature in a sense that only minor R&D is needed. They could be envisaged as baseline technology for new detectors in the next decade. For the more advanced technologies more basic R&D has to be performed. The most advanced via first processes need a more stable industrial basis.

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