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# First results of a Double-SOI pixel chip for x-ray imaging

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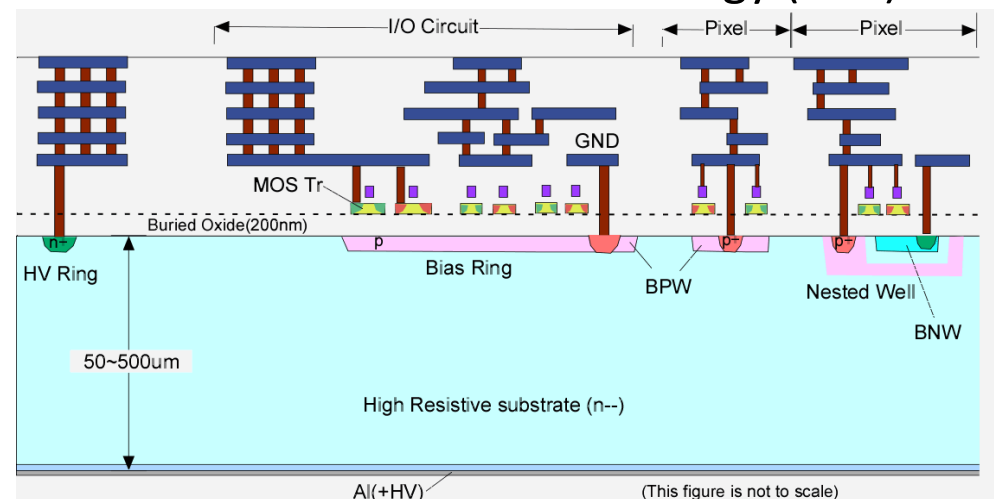
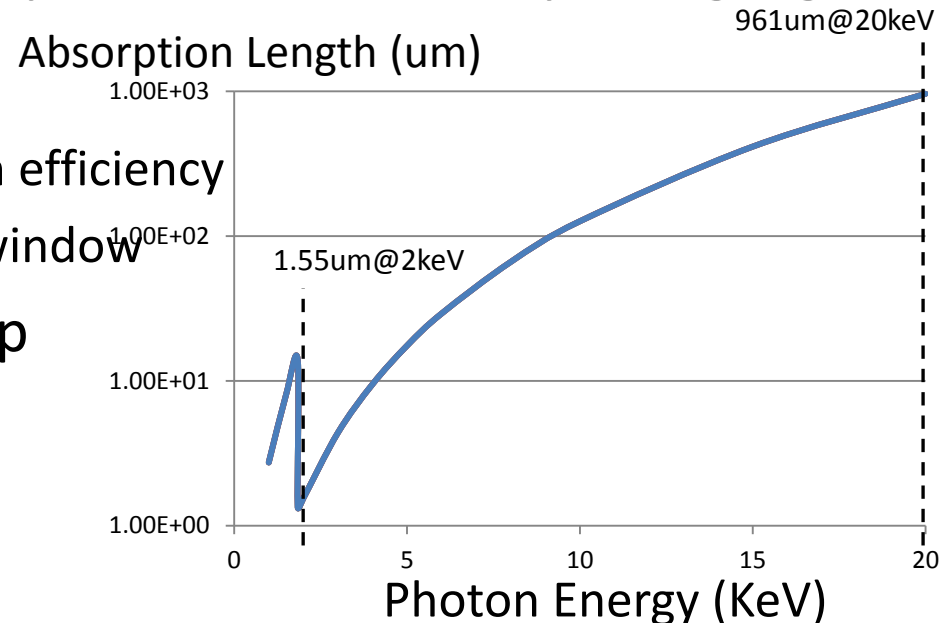
*10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Xi'an, Sep. 2015*

# Outline

- Introduction
  - Merits of SOI technology
  - Specifications of target
- Description of the prototype chip
  - Double-SOI
- Test results
  - I-V curve of sensor
  - Suppression of back-gate effect
  - Analog waveform fidelity
  - Digital crosstalk
  - Threshold scan and noise
  - Laser test
- Summary and outlook

# SOI technology offers great potential for X-ray imaging

- Full depleted substrate
  - Thickness up to 700um, quantum efficiency
  - Back illuminated, thin entrance window
- High density electronics on-chip
  - 0.2um full CMOS
  - 1 poly & 5 metal layers
- High density interconnect
  - Substrate contact size 0.3um
  - Pitch down to 2.2um



A schematic view of SOI structure

# Proposed applications in material science

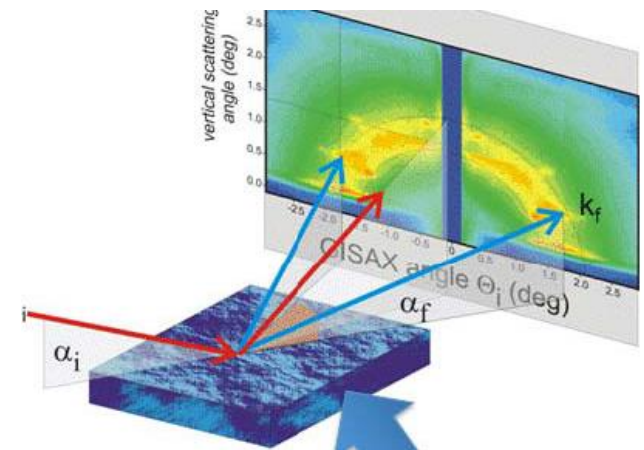
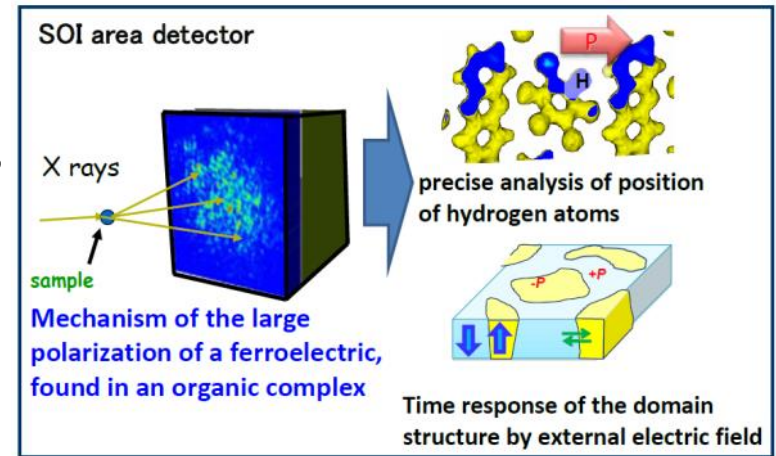
by Prof. Shunji KISHIMOTO (PF, KEK).

- New ferroelectric materials study requires measurement of the intensity of specific diffraction spots with

- 30um square pixel;
- 1k frame/s;
- 14-bit counter each pixel;

- Determination of structure change of cell membrane

- Grazing-incidence small-angle X-ray scattering (GISAXS);
- Minimum area 20~30mm<sup>2</sup>;
- 2.1~4.5keV, thin entrance window < 1um;



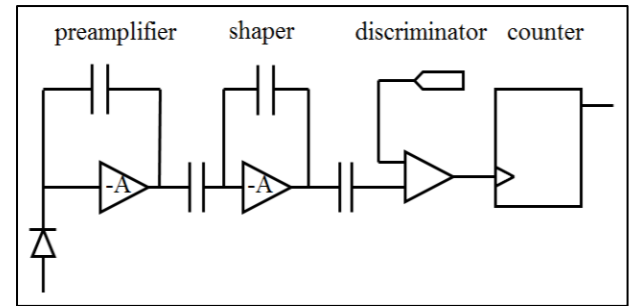
- Specifications of target

- 2~4keV ← Excellent S/N ratio
- 1MHz counting rate
- 1k frames/s
- 14-bit counter
- 30\*30  $\mu\text{m}^2$  pixel ← Very compact layout

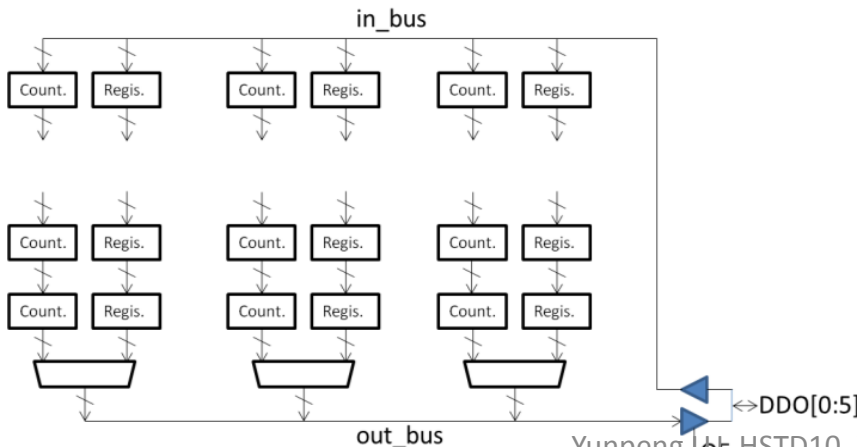
Low noise, high speed, and fine pitch counting-type SOI chip,  
which has never been achieved so far!

# CPIXTEG3b & Double-SOI

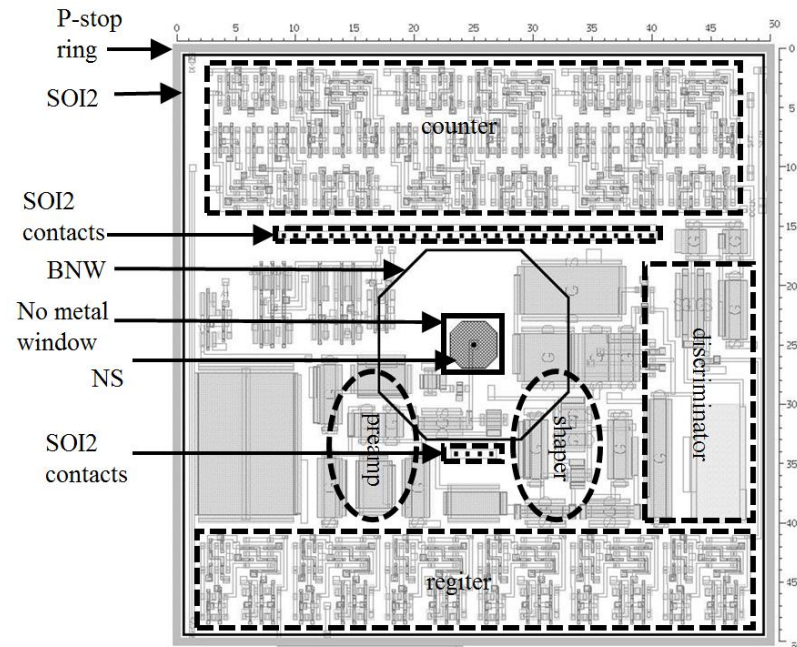
- The basic information of prototype chip CPIXTEG3b
  - A series of chips CPIXTEG1,2,3,3b
  - N-in-P sensor, 310um thick
  - Charge Amplification with constant feedback
  - Diode-biased inverter as the discriminator
  - 6-bit ripple counter & 6-bit register
  - Data chain organized in column
  - 50um \* 50um pixel layout
  - 64\*64 pixel array
  - **Double-SOI shielding**



Signal processing chain in-pixel

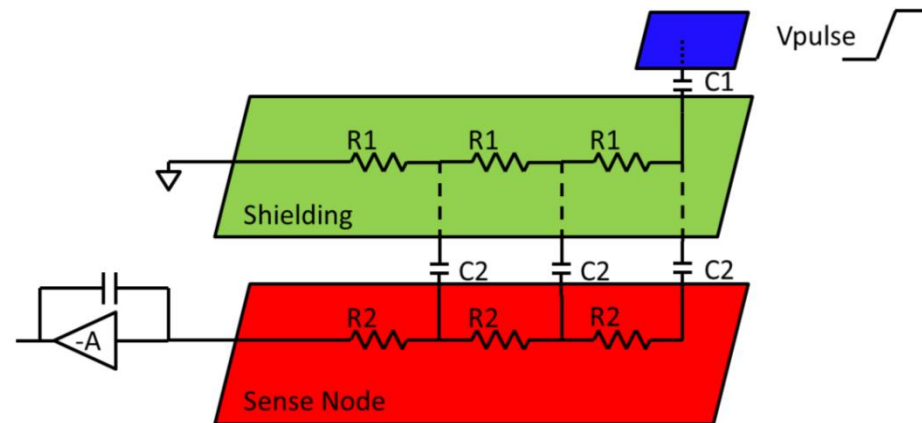
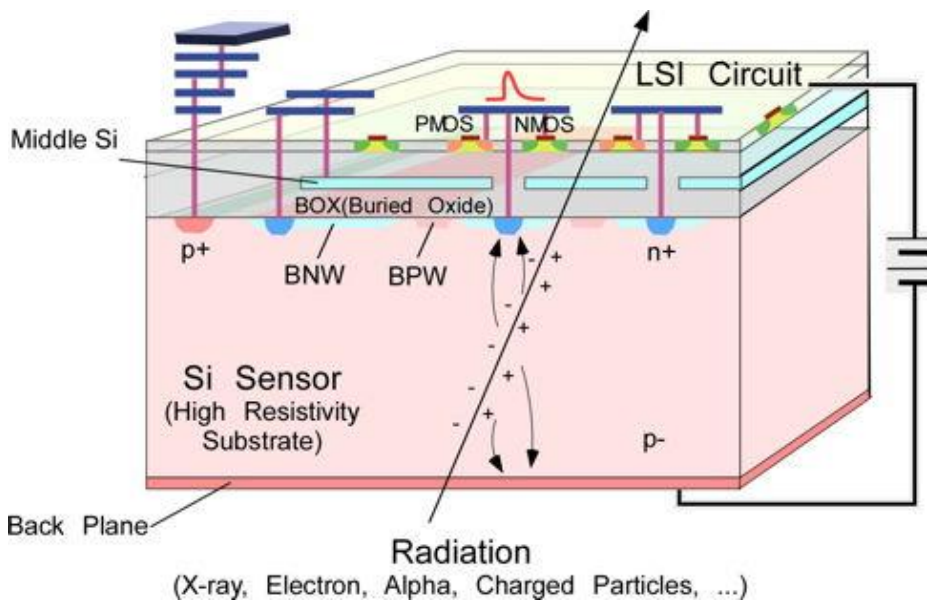


Data chain organized in column



Pixel layout

- Double-SOI is a critical ingredient to the success of counting-type pixel.
  - Sensor and transistors in pixel are intimately close to each other;
  - A shielding layer needed to suppress the back-gate effect and crosstalk;
  - Sheet resistance of SOI2 dictated a careful study of shielding mechanism
  - Joint efforts by SOI researchers and Foundry.

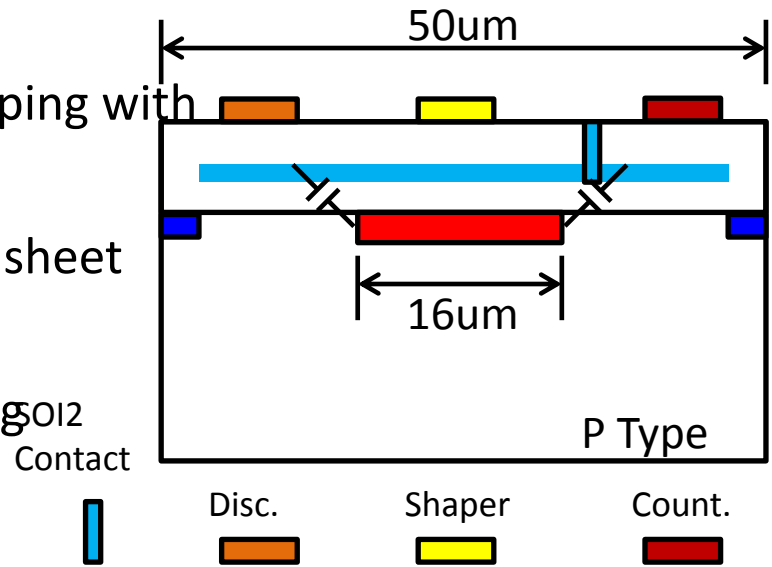


A simplified scenario of crosstalk

Detailed study on SOI shielding was reported at  
[International Workshop on SOI Pixel Detector \(SOPIX 2015\)](#)

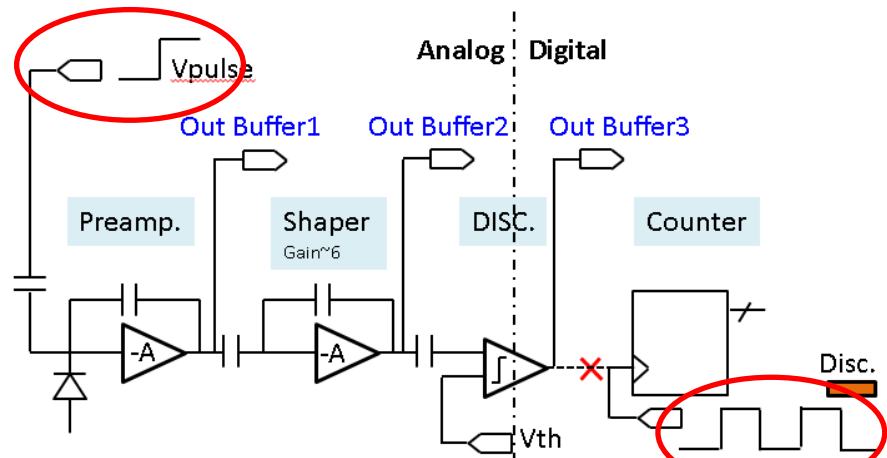
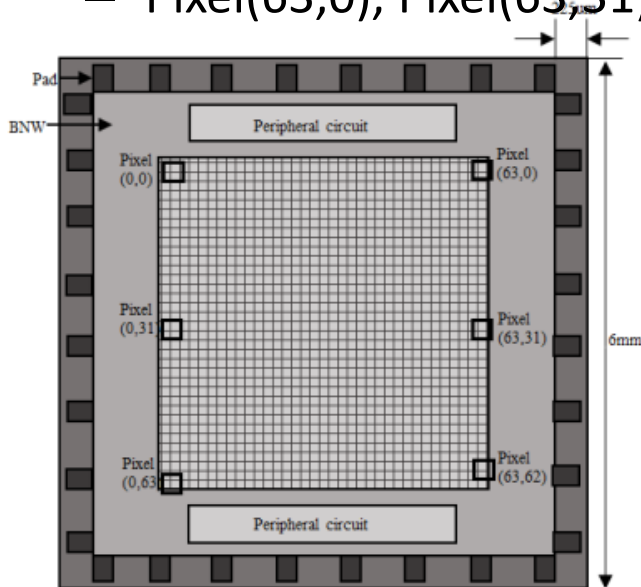
- Design optimization:

- Small electrode (16um) to avoid overlapping with digital parts;
- Dense SOI2 contacts to compensate the sheet resistance SOI2 layer
- Local bypass capacitor on SOI2 grounding
- P-stop ring isolating pixels



- Broke up pixels for test

- Pixel(0,0), Pixel(0,31), Pixel(0,63) for crosstalk measurement;
- Pixel(63,0), Pixel(63,31), Pixel(63,62) for evaluation of back-gate effect.

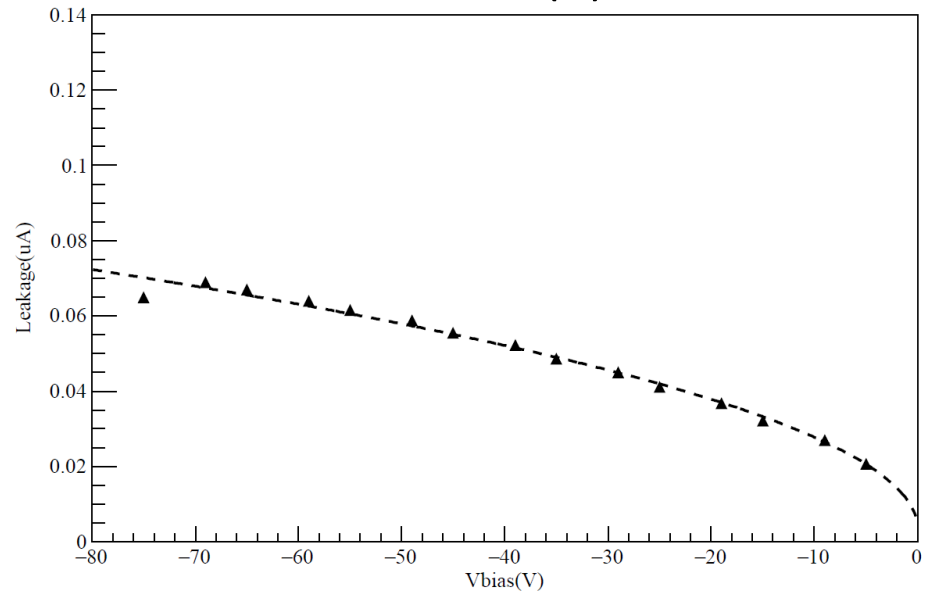
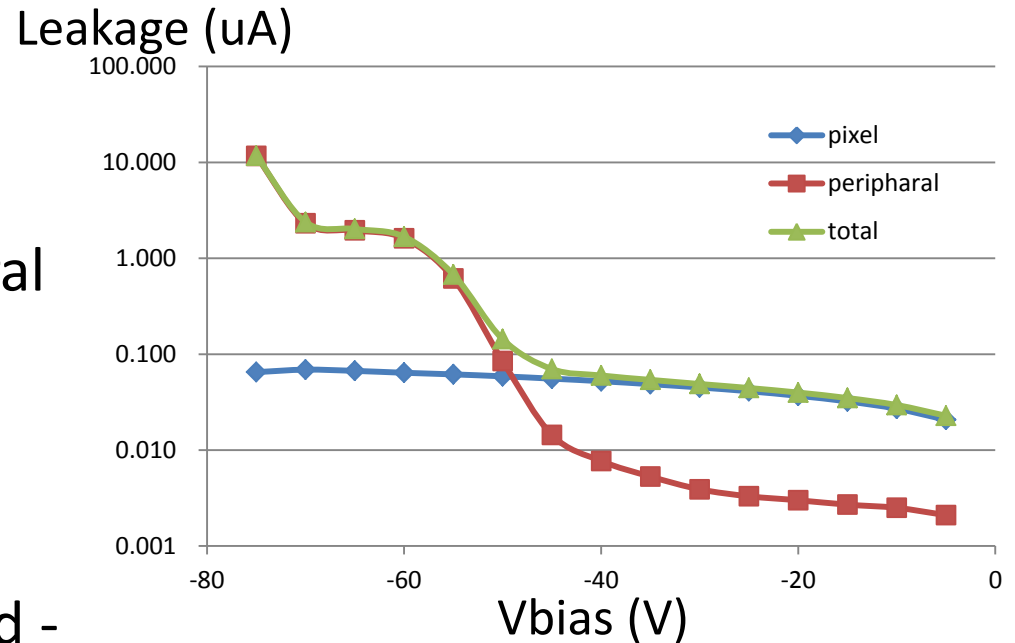


Pixel(0,63) used to measure the analog and digital crosstalk separately



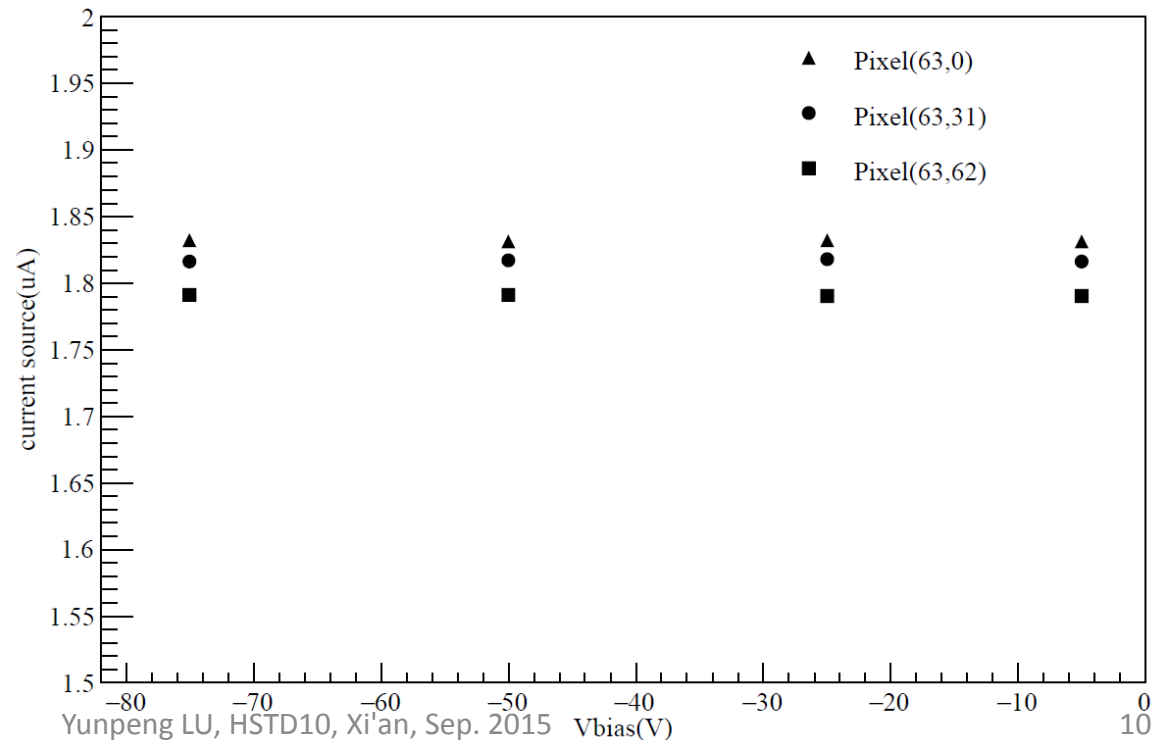
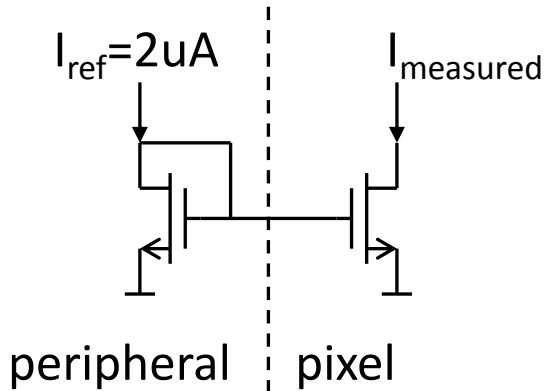
# I-V curve of sensor

- Total leakage - the peripheral
- Data points agreed with  $\sqrt{V_{bias}}$ ;
- 70nA/10mm<sup>2</sup>@room temp.
- Measurement failed beyond -80V due to a large peripheral;
- Multi-Guardring will be adopted in the next submission.



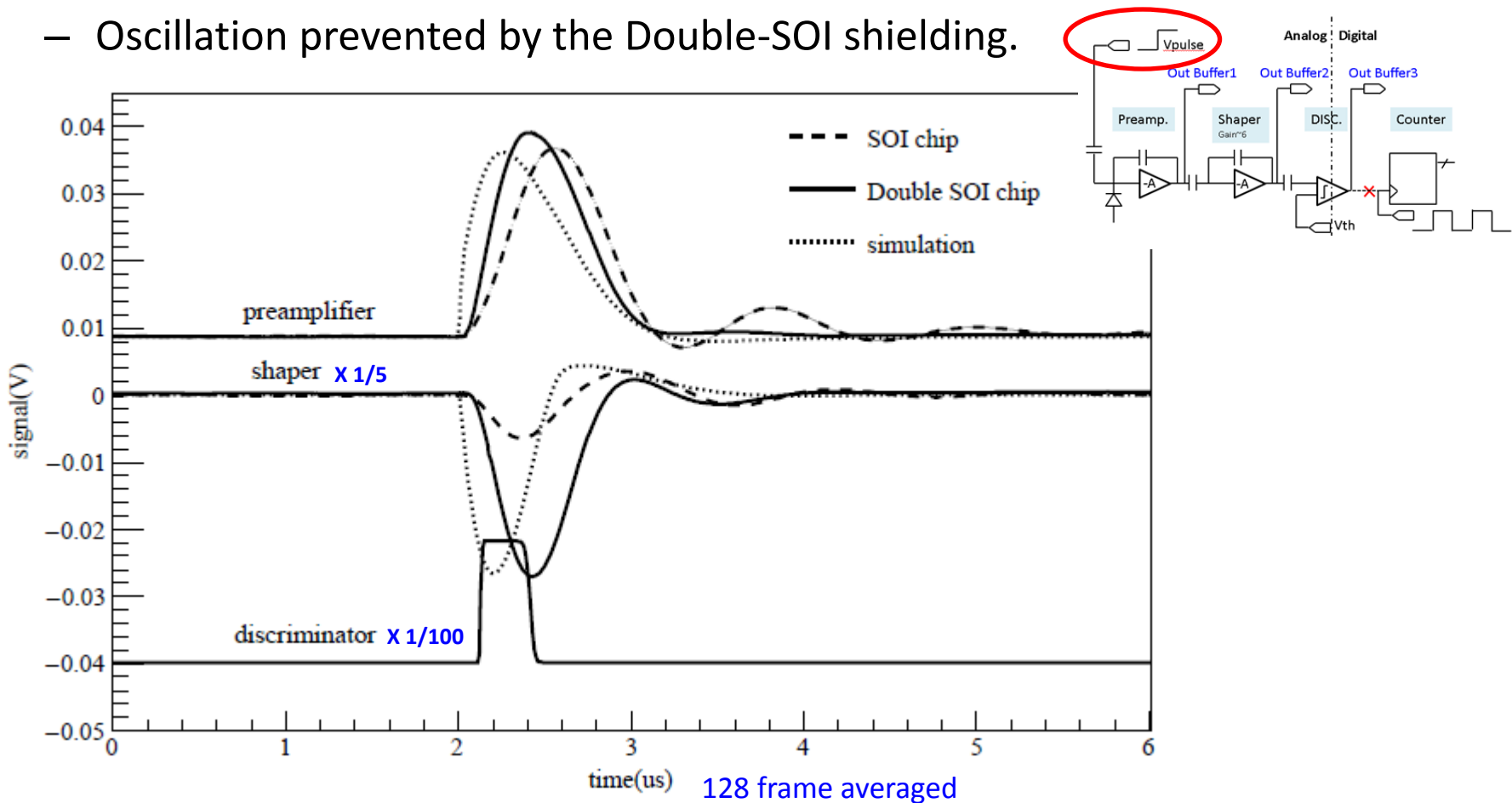
# Evaluation of back-gate effect

- Current mirror measured with different bias applied to backplane;
  - Input transistor in peripheral area, output transistor in pixel;
  - No change discernible as the  $V_{\text{bias}}$  increased up to -75V;
  - Suppression of back-gate effect proved.



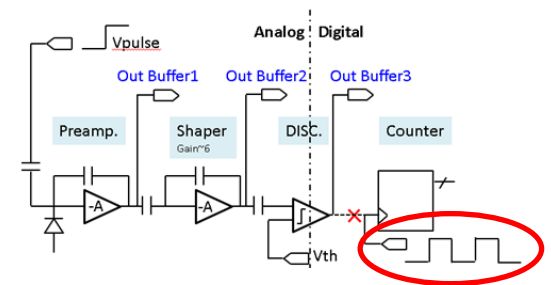
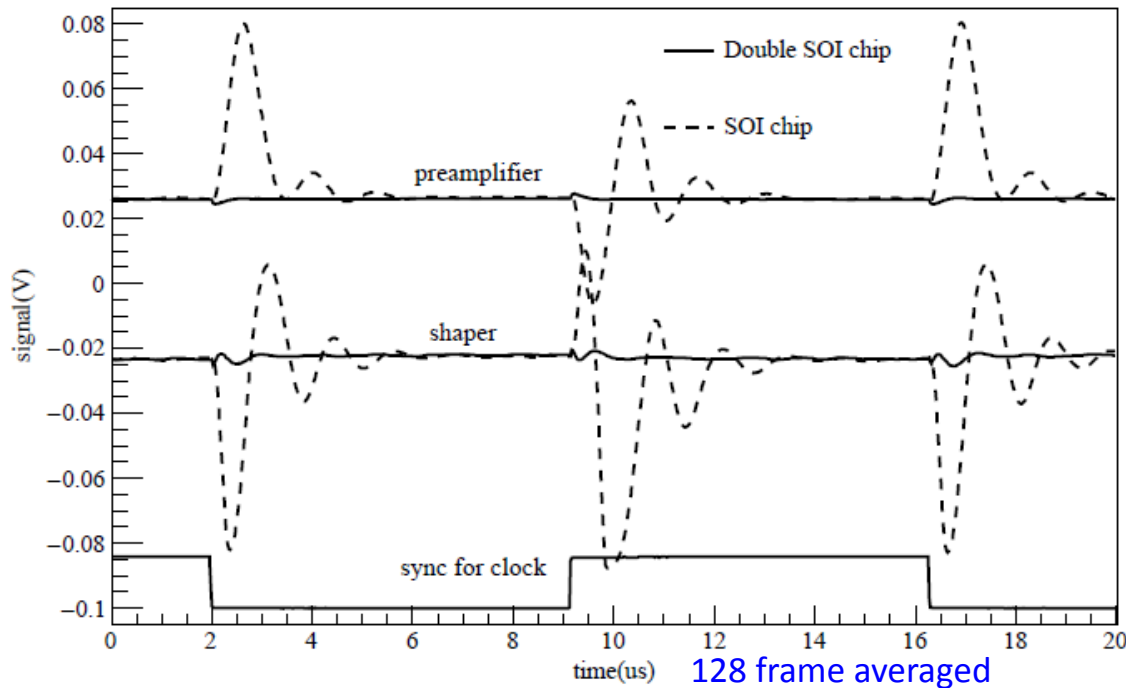
# Analog waveform inspection

- Calibration signal equivalent to  $1920e^-$
- Compared with a regular SOI chip (single SOI layer)
  - Oscillation prevented by the Double-SOI shielding.



# Crosstalk from counter

- **Compelling proof of shielding effectiveness**
  - 5mV @ shaper output for DSOI chip (74 e<sup>-</sup> referred to input charge), negligible when superimposed with noise (ENC ~ 113e<sup>-</sup>)
  - 95mV for regular SOI chip

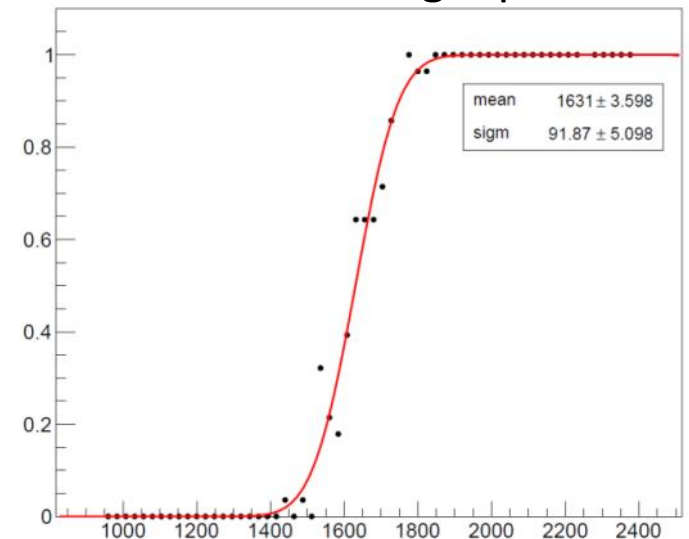


(peak to peak)	Double -SOI	Regular SOI
Preamp output	3.7mV	60mV
Shaper output	<b>5mV</b>	<b>95mV</b>

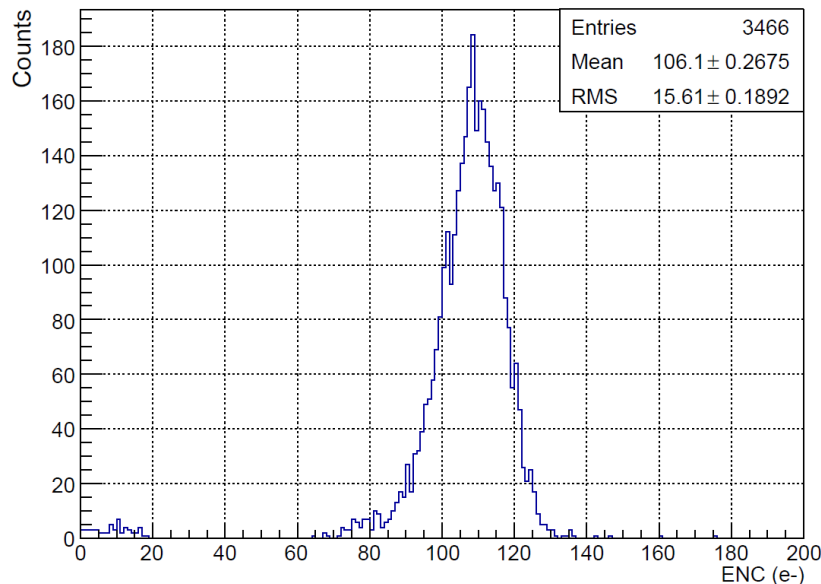
# Threshold scan and noise

- **Preliminary!**
- Threshold dispersion before tuning
  - RMS  $97e^-$  @  $1760e^-$
- ENC noise
  - Average  $106e^-$
- The whole pixel array is operational.

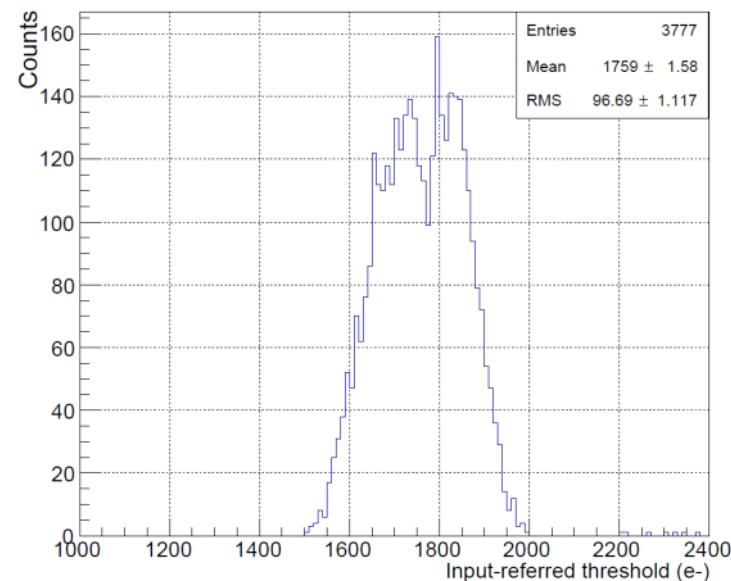
S-curve of single pixel



Charge injected ( $e^-$ )



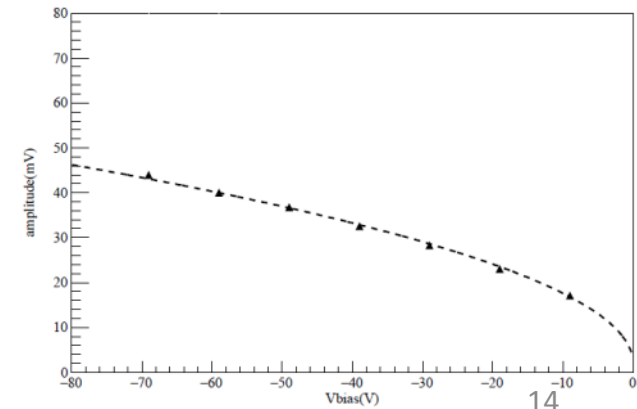
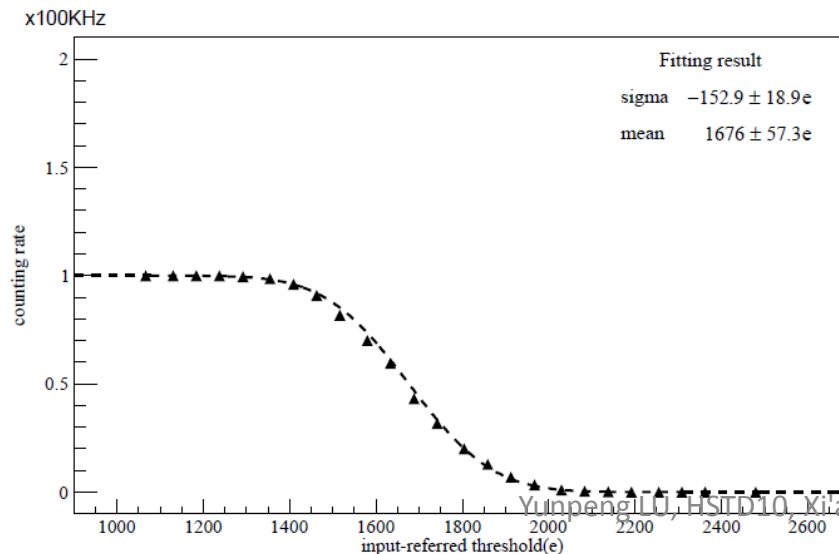
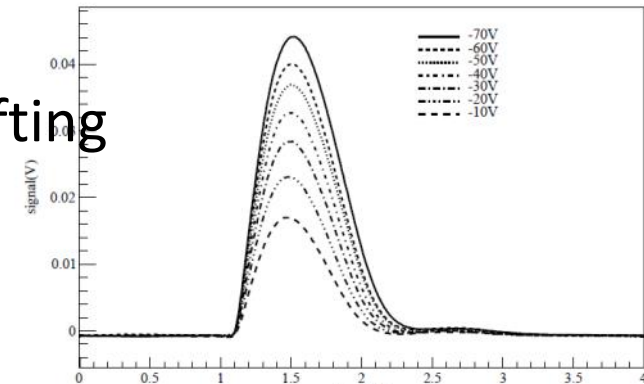
ENC noise distribution



Threshold dispersion

# Laser test

- Infrared laser beam
  - 1064nm, simulating MIP tracks in silicon;
  - Sub-ns pulses duration and 1MHz repetition;
- Signal amplitude increased as a function of  $V_{bias}$ 
  - Proportional to  $\sqrt{V_{bias}}$ ;
- Counting rate decreased as the threshold lifting
  - S-curve fitting resulted in  $153e^-$ ;
  - $1676 e^-$  generated by single laser pulse



# Summary and outlook

- SOI is an attractive technology to X-ray imaging
  - Fully depleted, high density electronics and interconnection
- Fine pitch, low noise and high speed counting-type SOI pixel is targeted on
  - for low energy x-ray diffraction and scattering experiments.
- The prototype chip CPIXTEG3b for the first time demonstrated that the counting-type SOI pixel is practical.
  - Crosstalk issue solved.
- X-ray test is planned in Oct. at KEK P.F.
- Next submission in Feb. 2016
  - Optimization for compact layout and low noise;

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