A 4 x 8-Gbps VCSEL Array Driver ASIC and integration with a custom array transmitter module for the LHC front-end transmission

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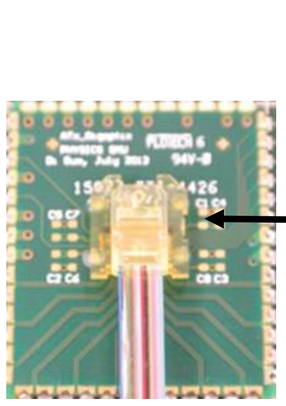
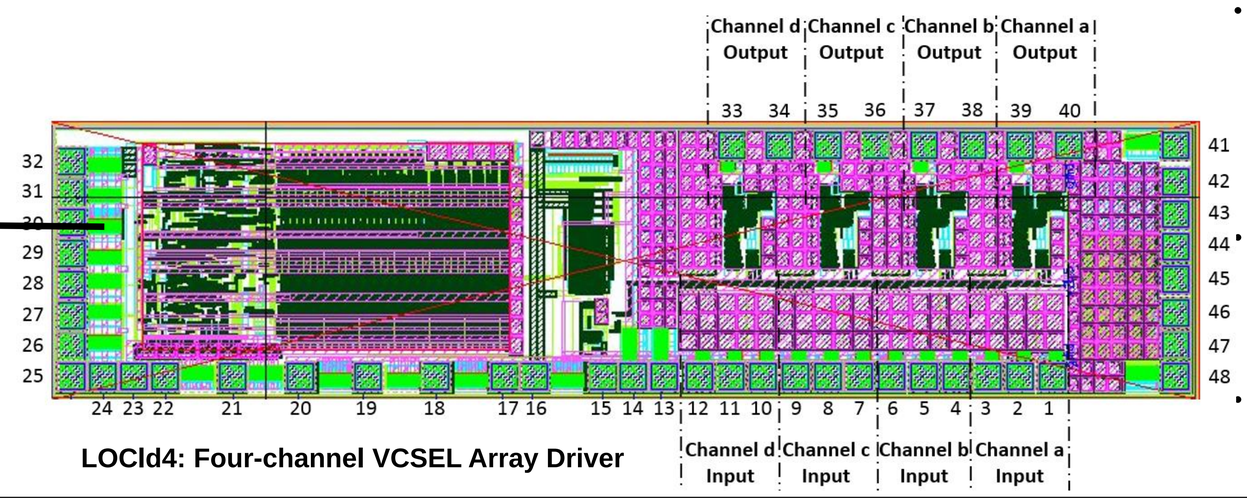
Introduction



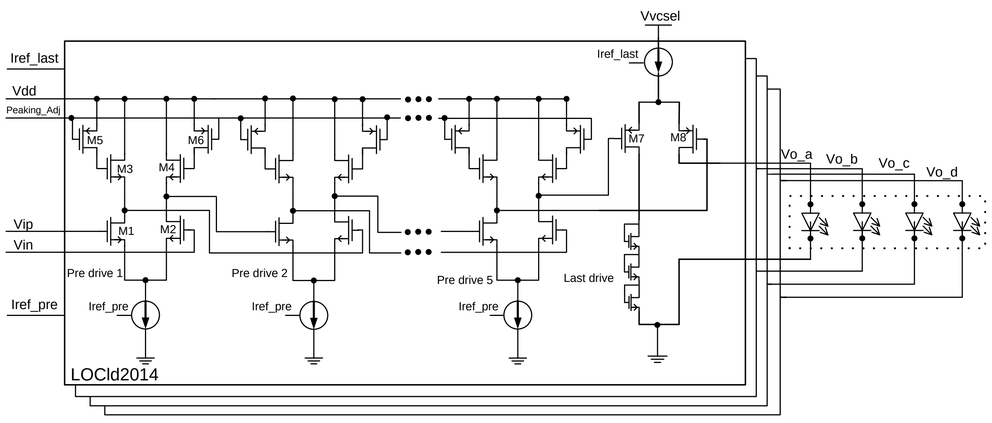
ATx Module



LOCld4: Four-channel VCSEL Array Driver

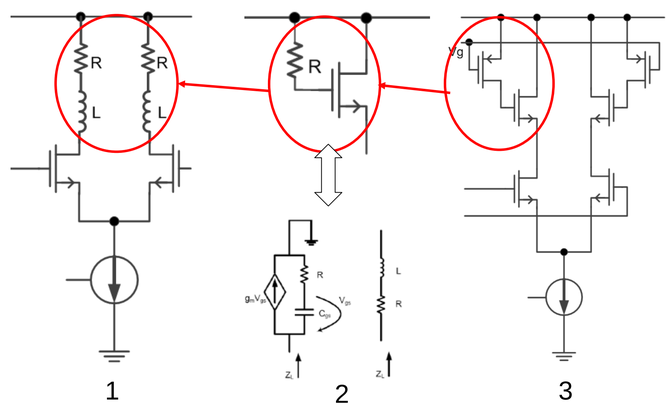
- The LOCld4 is a 4-channel, 4 x 8-Gbps VCSEL array driving ASIC with balanced differential output structure, fabricated in a commercial 0.25-um Silicon-on-Sapphire (SOS) CMOS technology, aimed for the LHC front-end transmission. This is the first VSCEL array driver ever fabricated at this aggregated bandwidth targeting the high-energy physics experiments.
- The ATx module is a custom, compact 12-channel array optical transmitter module integrating array optical components with the VCSEL array and the array driving ASIC using the active-alignment method. The LOCld4 is integrated within the ATx module and fully tested.
- The LOCld4 die measures 3000 um x 722 um. The ATx module measures 19 mm x 22 mm x 4.3 mm (thickness including optical components)

The design of the LOCld4



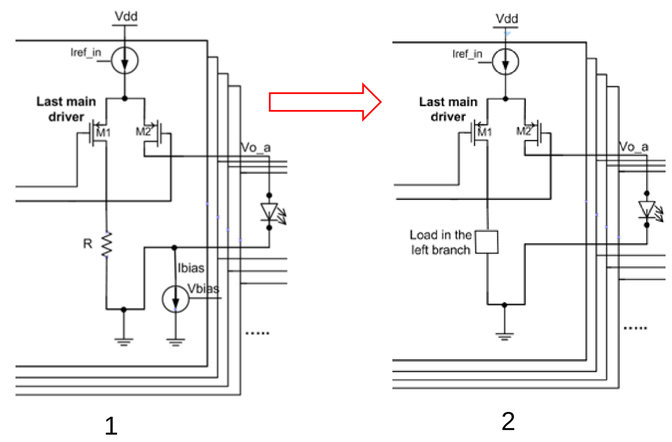
The schematic diagram of the LOCld4

- Each channel of the LOCld4, the 4-channel, 4 x 8-Gbps VCSEL array driving ASIC, consists of five pre-drivers and one last driver. Each channel receives a low-swing CML signal (differential p-p 200 mV), outputs 7.5 mA modulation current and 6.25 mA bias current in the anode-driving way to be compatible with the commercial common-cathode VCSEL array.
- Programmable active-shunt-peaking technique is used to extend the bandwidth in five pre-driving stages.
- A novel structure of the last driver removes the ordinary extra bias-circuit, and delivers both bias and modulation current with balanced branches to effectively minimize the switching signals on the power supply and crosstalk.



Active shunt peaking structure in the pre-drivers

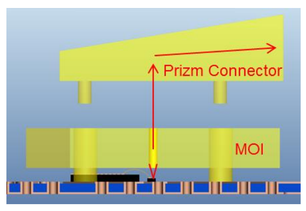
- The inductance load, so-called shunt peaking technique, creates one more pole in the transmission equation of the common-source amplifier to broaden the bandwidth, as shown in picture1.
- The passive inductance load is replaced by an MOS and resistor (active inductance), as shown in picture 2, for the area-saving consideration.
- Another PMOS is used to replace the resistor in the active inductance. The equivalent resistance of the PMOS is controlled by the V_g, which enables the programmable active-shunt-peaking.

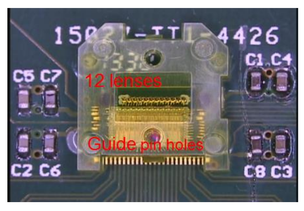


Balanced differential structure in the last driver

- Picture 1 shows the conventional way of delivering bias and modulation current. An extra bias circuit is added at the output branch, which breaks the balance of the last differential stage. It increases the switching components at the power source, which further induce the ground bounce noise and the crosstalk.
- Picture 2 shows the balanced differential structure in the LOCld4. The MOS of last driver delivers the bias and modulation current simultaneously, and the load of the left branch is deliberately designed to make it balance with the external branch where the VCSEL is connected as the load.

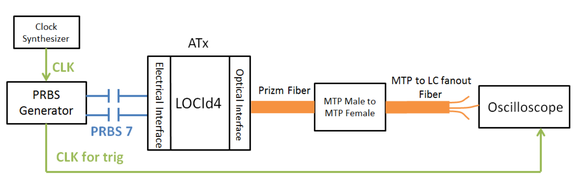
Integration with the custom array module(ATx) and test results

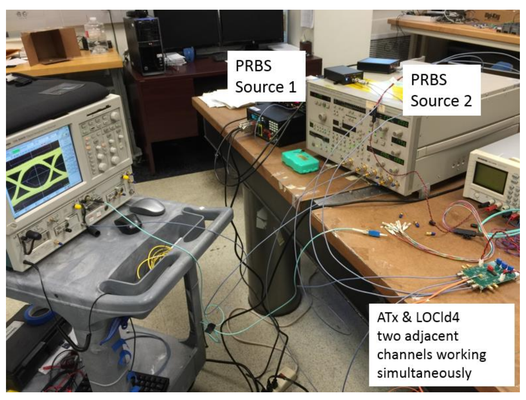




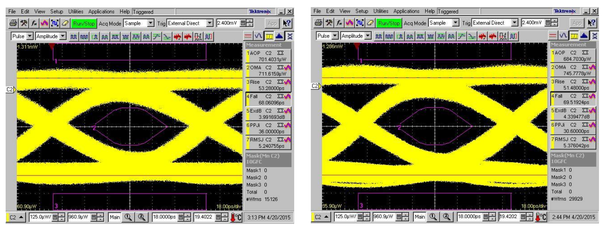
Light path of the array optical transmitter(ATx) module and the module picture

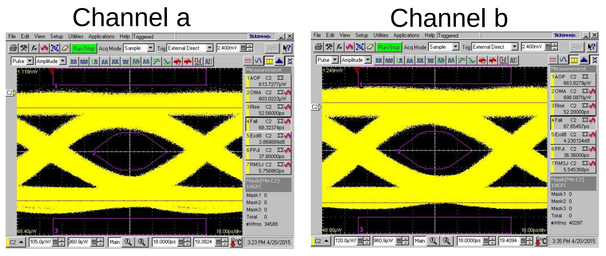
- One of the most difficult factor in the VCSEL array driver development is the tests, due to the high-density high-precision structure of the VCSEL array.
- The custom ATx module, utilizing the generic mechanical optical interface (MOI) and optical turn fiber ribbon (Prizm Connector) to couple out the parallel lights, enable the optical tests of the LOCld4 in the lab.
- The VCSEL array die and the VCSEL driver die (LOCld4) are assembled under the MOI, as shown in the upper right picture.



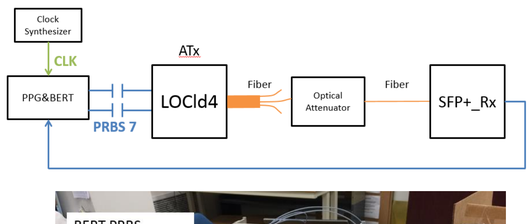


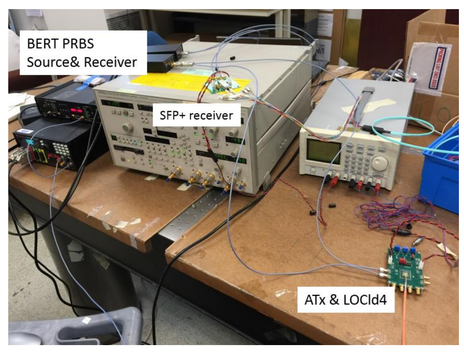
LOCld4 optical eye diagram testing diagram and set up





- With the ATx module, four-channel optical outputs are abled to be coupled out and tested. The optical eye diagram of each channel at 8-Gbps has been measured and passed the eye mask test with adjacent channels working simultaneously.





BER testing diagram and set up

- BER < 1E-12 is achieved at each channel at the rate of 8-Gbps when adjacent channels working simultaneously.

Conclusion

- A 4 x 8-Gbps VCSEL array driver(LOCld4) and a custom array optical transmitter module(ATx) for the LHC front-end transmission is designed and tested.
- All four channels pass the optical eye-diagram mask test at the rate of 8G-bps when adjacent channels working simultaneously with a power consumption of 150 mW per channel (VCSEL power included).

Acknowledgments

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