Vertex and tracking detector R&D for CLIC

10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors

Xi'an, China
September 29th, 2015

Dominik Dannheim (CERN)
on behalf of the
CLIC detector and physics (CLICdp) collaboration
Outline

• CLIC collider
• Requirements for vertex and tracking detectors
• R&D on sensor and readout technology
• Summary
CLIC

- **CLIC (Compact Linear Collider)**: linear $e^+e^-$ collider concept for post HL-LHC phase
- $\sqrt{s}$ from few hundred GeV up to 3 TeV (two-beam acceleration with $\sim 100$ MV/m)
- Physics goals:
  - Precision measurements of SM processes (Higgs, top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics: unique sensitivity to particles with electroweak charge

Possible staged CLIC implementation near CERN

- CLIC accelerating structure
- 48 km tunnel (3 TeV stage)
- 100 MV/m
CLIC machine parameters

<table>
<thead>
<tr>
<th></th>
<th>LHC at 14 TeV</th>
<th>CLIC at 3 TeV</th>
</tr>
</thead>
<tbody>
<tr>
<td>L (cm(^{-2})s(^{-1}))</td>
<td>1x10(^{34})</td>
<td>6x10(^{34})</td>
</tr>
<tr>
<td>BX separation</td>
<td>25 ns</td>
<td>0.5 ns</td>
</tr>
<tr>
<td>#BX / train</td>
<td>2808</td>
<td>312</td>
</tr>
<tr>
<td>Train duration</td>
<td>90 μs</td>
<td>156 ns</td>
</tr>
<tr>
<td>Train repetition</td>
<td>11 kHz</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>~1</td>
<td>0.00078%</td>
</tr>
<tr>
<td>σ(_x) / σ(_y) [nm]</td>
<td>15000 / 15000</td>
<td>≈ 45 / 1</td>
</tr>
<tr>
<td>σ(_z) [μm]</td>
<td>~50000</td>
<td>44</td>
</tr>
</tbody>
</table>

- **drives timing requirements for detectors**
- **very small beam sizes at interaction point**

*Not to scale!*
CLIC vertex-detector requirements

• efficient **tagging of heavy quarks** through precise determination of displaced vertices:

\[ \sigma(d_0) = \sqrt{a^2 + b^2 \cdot \text{GeV}^2 / (p^2 \sin^3 \theta)} \]

\( a \approx 5 \mu m, \ b \approx 15 \mu m \)

→ good single point resolution: \( \sigma_{SP} \approx 3 \mu m \)

→ small pixels \(<25 \times 25 \mu m^2\), analog readout

→ low material budget: \( X \approx 0.2\% X_0 / \text{layer} \)

→ corresponds to \( \sim 200 \mu m \) Si, including supports, cables, cooling

→ low-power ASICs (\( \sim 50 \text{ mW/cm}^2 \)) + gas-flow cooling

• 20 ms gaps between bunch trains → trigger-less readout, pulsed powering

• \( B = 4 \) T → Lorentz angle becomes important

• few % maximum occupancy from beam-induced backgrounds → sets inner radius

• moderate radiation exposure (\( \sim 10^4 \) below LHC!):
  • NIEL: \( < 10^{11} \) n\(_{eq}\)/cm\(^2\)/y
  • TID: \( < 1 \) kGy / year

• **Time stamping** with \( \sim 10 \) ns accuracy, to reject background

→ high-resistivity / depleted sensors, readout with precise timing
• Momentum resolution (Higgs recoil mass, $H \rightarrow \mu \mu$, BSM leptons):
  
  \[
  \sigma(p_T) / p_T^2 \sim 2 \times 10^{-5} \text{ GeV}^{-1}
  \]

  \rightarrow 7 \mu m \text{ single-point resolution}

  \rightarrow \sim 1\% X0 \text{ per layer (low-mass supports, cabling and cooling)}

• few % maximum occupancy from beam-induced backgrounds
  
  \rightarrow \text{Time stamping with } \sim 10 \text{ ns accuracy, to reject background}

  \rightarrow \text{Readout granularity } \sim 50 \mu m \times 1-10 \text{ mm (t.b.c.: large pixels / small strips?)}

Beam-induced background hits from $\gamma \gamma \rightarrow \text{hadrons and incoherent pairs}$:

Barrel

Endcaps

work in progress
CLIC vertex and tracking detector concepts

- Systematic optimization of geometries:
  - background occupancies
  - detector performance
    (flavor tagging, tracking resolution)
- Large coverage: $\theta > 7^\circ$ ($|\eta| < 2.8$)

- Outer tracker:
  - 5 barrel, 7 forward layers
  - $R \sim 1.5$ m, $L \sim 4.6$ m
  - beam pipes with conical sections

- Vertex region:
  - 3 double layers in barrel and endcaps
  - $\sim 1$ m$^2$ area, $\sim 2$G pixels
  - $R_i \sim 30$ mm
    (background-occupancies)
  - spiral endcap geometry
    (air flow cooling)
• Integrated R&D effort, simultaneously addressing CLIC vertex-detector challenges
• Examples for recent developments on the following slides

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Vertex + tracking R&D for CLIC
**Thin-sensors with Timepix r/o**

**Planar sensor assemblies with 55 μm pitch**
- Goal: test feasibility of ultra-thin sensors
- Producers: Micron and Advacam/VTT
- Readout: Timepix / Timepix3
- 50-300 μm sensor, 100-700 μm ASIC thickness
- slim-edge and active-edge layouts
- **Test-beam** campaigns with EUDET/AIDA telescope at DESY and CERN PS/SPS
- ultimate goal: 50 μm sensors on 50 μm ASICs

---

Micron/IZM assembly: 100 μm slim-edge sensor on 100 μm Timepix ASIC

Advacam assembly w. 50 μm active-edge sensor

Micron slim-edge sensor

Advacam edgeless sensor

Guard rings

Floating guard ring

Active edge

100 μm

50 μm sensor

700 μm Timepix

14 mm

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Vertex + tracking R&D for CLIC
Thin-sensors test-beam results

- High efficiency (>99%) for 50 μm sensors
- Large improvement of position resolution with charge interpolation for 2-hit clusters
- 1-hit clusters dominating for thin sensors
  → limits achievable resolution
  → need smaller pixels / enhanced charge sharing

- RMS ≈ 15.2 μm
- 2-hit cluster: σ ≈ 4.1 μm
- telescope pointing resolution ~3 μm not unfolded

- 50 μm sensor
- 2-hit clusters
- 1-hit clusters

- Operating threshold ~860 e⁻

- Work in progress
Hybrid r/o technology: CLICpix

- 65 nm CMOS hybrid r/o chip, targeted to CLIC vertex detectors
- based on Timepix/Medipix chip family, synergy with HL-LHC pixel r/o projects (RD53 collaboration on 65 nm r/o)
- demonstrator chip with 64 x 64 matrix
- 25 μm pixel pitch
- simultaneous 4-bit time (TOA) and energy (TOT) measurement per pixel
  → front-end time slicing < 10 ns
- selectable compression logic: pixel, cluster + column-based
  → full chip r/o in < 800 μs
  (at 10% occup., 320 MHz r/o clock)
- power pulsing scheme
  → $P_{avg} < 50 \, \text{mW/cm}^2$
- standalone lab measurements
  → performance in agreement with simulations
- test assemblies with planar and active HV-CMOS sensors

### CLICpix standalone measurement results:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise time</td>
<td>[ns]</td>
<td>50</td>
<td>-</td>
</tr>
<tr>
<td>TOA accuracy</td>
<td>[ns]</td>
<td>&lt;10</td>
<td>&lt;10</td>
</tr>
<tr>
<td>Gain</td>
<td>[mV/ke$^{-}$]</td>
<td>44</td>
<td>40 $^*$</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>[ke$^{-}$]</td>
<td>44 (configurable)</td>
<td>40 $^*$ (configur.)</td>
</tr>
<tr>
<td>Integr. nonlinearity (TOT)</td>
<td>[LSB]</td>
<td>&lt;0.5</td>
<td>&lt;0.5</td>
</tr>
<tr>
<td>ENC (w/o sensor)</td>
<td>[e$^{-}$]</td>
<td>~60</td>
<td>~55 $^*$</td>
</tr>
<tr>
<td>DC spread σ (uncalibrated)</td>
<td>[e$^{-}$]</td>
<td>160</td>
<td>128 $^*$</td>
</tr>
<tr>
<td>DC spread σ (calibrated)</td>
<td>[e$^{-}$]</td>
<td>24</td>
<td>22 $^*$</td>
</tr>
<tr>
<td>Power consumption</td>
<td>[$\mu$W/pixel]</td>
<td>6.5</td>
<td>7</td>
</tr>
</tbody>
</table>

$^*$ results obtained with electrical test pulses
CLICpix planar sensor assemblies

- Single-chip bump-bonding process for 25 μm pitch developed at SLAC (C. Kenney, A. Tomada)

- Process flow:
  - Spin photoresist
  - Expose with contact aligner
  - Evaporator: 4 μm Indium
  - Lift-off
  - Bumping

- 3 test assemblies produced with 200 μm n-in-p CLICpix sensors from Micron Velopix wafer

  - Unconnected and shorted pixels correlated with defects visible before flipping

Observed on 3 test assemblies:
- 0.2-3% unconnected channels
- 1-2% shorted channels

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CLICpix planar sensor test-beam results

CERN SPS test beam with AIDA telescope:
• Operation threshold \( \sim 1000 \) e\(^-\)
• \( V_{\text{dep}} \sim 35 \) V
• High detection efficiency (>99.5%)
• \( \sim 30\% \) single-pixel clusters at \( V_{\text{dep}} \)
• \( \sim 4 \) \( \mu \)m single-point resolution

In-pixel cluster maps

- 1 pixel clusters
- 2 pixel clusters
- 3 pixel clusters
- 4 pixel clusters

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HV-CMOS active sensor with capacitive coupling

Capacitive Coupled Pixel Detector (CCPD)
- Prototype for ATLAS (FEI4) and CLIC: CCPDv3
- AMS H18 180 nm HV-CMOS process
- Vbias~30-90 V → depletion layer ~10-20 μm
- 2-stage amplifier, capacitive coupling to readout ASIC through thin glue layer (few μm)
- Includes 64x64 matrix (25 μm pitch)
- Glue assemblies with CLICpix readout chips produced
CCPDv3-CLICpix glue assemblies

- Study of glue parameters:
  - Viscosity
  - Bonding force
  - Alignment
  - Glue-layer uniformity

- Cross sections of glue assemblies
  \( \rightarrow \) alignment precision \(~1 \mu m\)
  \( \rightarrow \) glue-layer thickness \(~0.5 \mu m\)
  \( (+2 \mu m \text{ polyimide passivation})\)

- Laboratory and test-beam measurements
  \( \rightarrow \) correlate performance with glue parameters (coupling strength, uniformity)

Centered alignment

\( \frac{1}{2} \) pixel offset

SEM picture CCPDv3-CLICpix assembly

- Study of glue parameters:
  - Viscosity
  - Bonding force
  - Alignment
  - Glue-layer uniformity

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Centered alignment

\( \frac{1}{2} \) pixel offset
CCPDv3-CLICpix calibration

- Dedicated test pixels: direct access to CCPDv3 output signal
- Used to calibrate CLICpix ToT response
- Simulation of CLICpix ToT response for different values of coupling capacitance → estimate coupling capacitance by comparison of measured and simulated response: ~10 fF

Measured CCPDv3+CLICpix response

Simulated CCPDv3+CLICpix response

work in progress
CCPDv3-CLICpix test-beam results

CERN SPS test beam with AIDA telescope:
- High detection efficiency, even without bias (diffusion)
- Measured mean charge (ToT) varies across matrix → non-uniformity of glue thickness, observed in early assemblies produced without control of planarity
- ~6 μm single-point resolution

Detection efficiency vs. bias

Detection efficiency vs. threshold

ToT uniformity

CLICdp-Pub-2015-003

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CCPDv3 TCAD simulation

- Implemented CCPDv3 pixel layout in TCAD
  - n-in-p sensor
  - thickness: 75 μm
  - resistivity: 10 Ωcm
  - bias voltage: -60 V
- 2-D transient simulation for MIPs at different positions within pixel
  - Fast rise of collected charge within ~ns (drift in depleted volume)
  - Significant increase over hundreds of ns (diffusion in bulk)
- Next steps:
  - validation with 3-D simulation
  - interface sensor response to CLICpix simulation
  → simulation of full chain

![Layout for 2-D simulation](image)

- Collected charge [e⁻]

  - MIP 1
  - MIP 2
  - MIP 3

  - Drift component
  - Diffusion component

  - Work in progress

September 29, 2015  Vertex + tracking R&D for CLIC
Summary

• Challenging requirements for vertexing and tracking at CLIC
• Developed detector concepts matching the requirements
• Recent progress in CLIC vertex detector R&D:
  • Ultra-thin planar sensors with Timepix readout
    → competing requirements: charge sharing vs. material budget
  • Fine-pitch planar sensors with CLICpix readout
    → bump bonding with 25 μm pitch on single-die level
  • Active HV-CMOS sensors with capacitive coupling
    → proof of principle achieved, calibration in progress

More information:
CLICdp WG vertex-detector technology: http://indico.cern.ch/category/2843/
CLICdp WG tracker technology: http://indico.cern.ch/category/6243/

Thanks to everyone who provided material for this talk!
CLIC detector & physics collaboration

CLICdp member institutes:
- Dept. of Physics, Aarhus University
- Laboratoire d’Annecy-le-Vieux de Physique des Particules (LAPP), Annecy
- Vinca Institute for Nuclear Sciences, Belgrade
- University of Bergen
- The School of Physics and Astronomy, University of Birmingham
- University of Bristol
- Institute of Space Science, Bucharest
- Dept. of Physics, University of Cambridge
- Dept. of Physics and Technology, AGH University of Science and Technology, Cracow
- Polish Academy of Sciences, Cracow
- CERN, Geneva
- University of Glasgow
- Argonne National Laboratory, Lemont
- Department of Physics, University of Liverpool
- Australian Collaboration for Accelerator Science (ACAS), Melbourne
- University of Michigan, Ann Arbor
- NC PHEP, Belarusian State University, Minsk
- MPI Munich
- Dept. of Physics, Oxford University
- Institute of Physics of the Academy of Sciences of the Czech Republic, Prague
- Pontificia Universidad Católica de Chile, Santiago de Chile
- Spanish Network for Future Linear Colliders
- Dept. of Physics, Tel Aviv University

• The CLICdp collaboration is addressing detector and physics issues for the future Compact Linear Collider (CLIC) [http://clicdp.web.cern.ch/]
• CERN acts as host laboratory
• Currently 26 institutes from 16 countries
• The CLIC accelerator R&D is being conducted in collaboration with ~48 institutes
**2013-18 Development Phase**
Develop a Project Plan for a staged implementation in agreement with LHC findings; further technical developments with industry, performance studies for accelerator parts and systems, as well as for detectors.

**4-5 year Preparation Phase**
Finalise implementation parameters, Drive Beam Facility and other system verifications, site authorisation and preparation for industrial procurement. Prepare detailed Technical Proposals for the detector-systems.

**Construction Phase**
Stage 1 construction of CLIC, in parallel with detector construction. Preparation for implementation of further stages.

**2018-19 Decisions**
On the basis of LHC data and Project Plans (for CLIC and other potential projects), take decisions about next project(s) at the Energy Frontier.

**2024-25 Construction Start**
Ready for full construction and main tunnel excavation.

**Commissioning**
Becoming ready for data-taking as the LHC programme reaches completion.
CLIC detector concept

• Low-mass **vertex detector** with ~25x25 μm² pixels

• **Silicon tracker**

• Fine-grained **PFA calorimetry**, 1+7.5 \( \Lambda_i \)

• 4-5 T solenoid

• **Return yoke** with muon ID

• Complex **forward region** with final beam focusing
• Precision measurements of SM processes (Higgs, top, electroweak)
• Precision measurements of new physics potentially discovered at 14 TeV LHC
• Search for new physics: unique sensitivity to particles with electroweak charge

• Flavor tagging essential:
  • Separation of b, c and light jets, e.g. measurement of H→bb,cc,gg
  • Accurate reconstruction of top quarks in the decay t→Wb, e.g. for ttH
  → need high-precision vertex detectors
**Flavor-tagging performance**

- Use b- and c-tagging performance as benchmark for detector designs
- Challenging full-simulation study (multivariate analysis)
- Implementations following engineering studies:
  - Geometry with **2x more material** in vertex layers
    \[ \rightarrow 5\% - 35\% \text{ degradation in performance} \]
  - **Spiral end-cap** geometry (air-flow cooling)
    \[ \rightarrow \text{few problematic regions with reduced coverage,} \]
    otherwise similar performance as for disk geometry
  - 3 double layers vs. 5 single layers
    \[ \rightarrow \text{small improvement for lower-energy jets (less material per layer)} \]

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**Material budget**

**Spiral end caps vs. disks**

**Double vs. single layers**

P. Roloff, N. Alipour Tehrani
Flavor tagging: impact on physics performance

- $e^+e^- \rightarrow H_{\nu\nu}$: dominating Higgs production process at $\sqrt{s}=3$ TeV
- $\sigma \times$ BR measurement for the decays to $bb$ and $cc$
- flavor tagging crucial for achievable precision

<table>
<thead>
<tr>
<th>channel</th>
<th>stat. unc. on $\sigma \times$BR</th>
<th>change for +/−20% fake r.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$H \rightarrow bb$</td>
<td>0.23%</td>
<td>0.24% / 0.21%</td>
</tr>
<tr>
<td>$H \rightarrow cc$</td>
<td>3.1%</td>
<td>3.6% / 2.6%</td>
</tr>
</tbody>
</table>

- consider $\pm 20\%$ change in fake rates
- sizeable effect, in particular for $H \rightarrow cc$: $30\%$ more integ. luminosity required for same precision when increasing fake rate by $20\%$ ($>1$ year of additional running!)

LCD-Note-2011-036, CLICdp Note-2014-002
Beam-induced backgrounds

small beam profiles at IP → very high E-fields
Beamstrahlung leads to:
• $e^+e^-$ pairs
• hadronic events
→ Reduces $E_{cm}$
→ Background particles

CLIC luminosity spectrum
$L=6\times10^{34}\text{ cm}^{-2}\text{s}^{-1}$
30% in “1% highest energy”

Main backgrounds in detector:
• **Incoherent $e^+e^-$ pairs**: 60 particles / BX
detector design issue (occupancies)
• $\gamma\gamma \rightarrow$ hadrons: 54 particles / BX
impacts physics
→ Need pile-up rejection
Backgrounds in inner tracking region

CLIC_ILD incoherent pairs + $\gamma\gamma \rightarrow$ hadrons: silicon hits, no safety factors

• Train occupancies up to 3% in vertex region (including clustering and safety factors)
• moderate radiation exposure, $\sim 10^4$ below LHC

<table>
<thead>
<tr>
<th>Region</th>
<th>Readout granularity</th>
<th>Max. occup.</th>
<th>NIEL [n_{eq}/cm^2/y]</th>
<th>TID [Rad/y]</th>
</tr>
</thead>
<tbody>
<tr>
<td>VXB</td>
<td>20 $\mu$m x 20 $\mu$m</td>
<td>1.9 %</td>
<td>4x10^{10}</td>
<td>20k</td>
</tr>
<tr>
<td>VXEC</td>
<td>20 $\mu$m x 20 $\mu$m</td>
<td>2.8 %</td>
<td>5x10^{10}</td>
<td>18k</td>
</tr>
<tr>
<td>FTD pixels</td>
<td>20 $\mu$m x 20 $\mu$m</td>
<td>0.6%</td>
<td>2.5x10^{10}</td>
<td>5k</td>
</tr>
<tr>
<td>FTD strips</td>
<td>10 cm x 50 $\mu$m</td>
<td>290 %</td>
<td>1x10^{10}</td>
<td>700</td>
</tr>
<tr>
<td>SIT</td>
<td>9 cm x 50 $\mu$m</td>
<td>170 %</td>
<td>2x10^{9}</td>
<td>200</td>
</tr>
</tbody>
</table>
## Medipix/Timepix hybrid r/o chip family

<table>
<thead>
<tr>
<th>Chip</th>
<th>Year</th>
<th>CMOS Process</th>
<th>Pitch [μm²]</th>
<th>Pixel operation modes</th>
<th>r/o mode</th>
<th>Main applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timepix</td>
<td>2006</td>
<td>250 nm</td>
<td>55x55</td>
<td>∫ToT or ToA or γ counting</td>
<td>Sequential (full frame)</td>
<td>HEP (TPC)</td>
</tr>
<tr>
<td>Medipix3RX</td>
<td>2012</td>
<td>130 nm</td>
<td>55x55</td>
<td>γ counting</td>
<td>Sequential (full frame)</td>
<td>Medical</td>
</tr>
<tr>
<td>CLICpix demonstrator</td>
<td>2013</td>
<td>65 nm</td>
<td>25x25</td>
<td>ToT + ToA</td>
<td>Data driven</td>
<td>Test chip with 64x64 pixel matrix</td>
</tr>
<tr>
<td>Timepix3</td>
<td>2013</td>
<td>130 nm</td>
<td>55x55</td>
<td>ToT + ToA, γ counting + ∫TOT</td>
<td>Data driven</td>
<td>HEP, Medical</td>
</tr>
<tr>
<td>Velopix</td>
<td>2015</td>
<td>130 nm</td>
<td>55x55</td>
<td>ToT + ToA, γ counting + ∫TOT</td>
<td>Data driven</td>
<td>LHCb (10x Timepix3 rate)</td>
</tr>
<tr>
<td>Smallpix/Timepix4</td>
<td>2016</td>
<td>65 nm (t.b.c.)</td>
<td>~35x35</td>
<td>ToT + ToA, γ counting + ∫TOT</td>
<td>Data driven</td>
<td>HEP, Medical</td>
</tr>
<tr>
<td>CLICpix</td>
<td>tbd</td>
<td>65 nm</td>
<td>25x25</td>
<td>ToT + ToA</td>
<td>Sequential (data comp.)</td>
<td>CLIC vertex detector</td>
</tr>
</tbody>
</table>

- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

ToT: Time-over-Threshold  
→ Energy
ToA: Time-of-Arrival  
→ Time

September 29, 2015  
Vertex + tracking R&D for CLIC
Timepix3 high-rate hybrid pixel readout ASIC:

- 256x256 pixels, 55 μm pitch
- implemented in 130 nm CMOS technology
- simultaneous ToT (10 bit) and ToA (18 bit), event counting, integr. ToT
- fast time stamping (1.6 ns precision)
- data-driven readout up to 40 Mhits/cm²/s
- power-pulsing functionality

- assemblies with Advacam 300 μm sensors produced
- test-beam campaign in CERN-PS (August 2014) with AIDA/EUDET telescope
  → first results in talk by M. Benoit on Tuesday
- later this year: thin-sensor assemblies
• The analog front-end shapes photocurrent pulses and compares them to a fixed (configurable) threshold
• Selectable polarity (positive / negative signals)
• Digital circuits simultaneously measure Time-over-Threshold and Time-of-Arrival of events and allow for zero-compressed readout
CLICpix analog frontend

Krummenacher network

CSA preamplifier

Calibration DAC

Discriminator

Digital part
CLICpix: time and energy measurement

- Energy measurement: Time Over Threshold (TOT)
- Time measurement: Time of Arrival (TOA)

Baseline

Threshold

Particle

0 1 2 3 4

V

time

Configuration data:
Th.Adj, TpulseEnable, CountingMode, Mask

Threshold

Polarity

Feedback network

Input

CSA

4-bit Th.Adj DAC

Polarity

V_{test\_pulse}

4-bit TOT counter

4-bit TOA counter

Clk divider

HF

Bottom pixel

Top pixel

shutter close
CLICpix: energy measurement

- Measure charge released in each pixel
  → Improve position resolution through interpolation

- Time-Over-Threshold (TOT) measurement (4-bit precision)

- Calibration measurement using external test pulser:

![Graph showing energy measurement for various preamp. settings](image-url)
Calibrated spread across the whole matrix is 0.89 mV RMS (~22 e⁻)
For comparison: MIP signal in 50 μm silicon ~3700 e⁻

S. Kulis, P. Valerio
CLICpix: uniformity of gain and noise

- Uniform gain across the matrix
- Gain variation ~4.2% r.m.s.
  (for nominal feedback current)

- Uniform ENC across the matrix
- Mean ENC: 55 e^-, SD: 5.7 e^-
  (without sensor)
CLICpix: radiation qualification

- Moderate radiation-tolerance requirements at CLIC: <100 kRad TID
- However: building blocks can be re-used for RD53 (~1 GRad required)
- Results of radiation testing useful for gaining deeper understanding of the chip
  → performed radiation test up to 1 GRad (up to 150 kRad/minute) in calibrated X-ray setup

- No significant changes observed in sub-MRad range relevant for CLIC
- For >250 MRad: PMOS switches in current mirror fail
  → Break-down of analog power (note: band gap foreseen for final chip, instead of current mirror)
- digital components kept working normally

S. Kulis, P. Valerio
First ideas for new version of CLICpix:

- larger pixel matrix (**256x256**)
- analog front-end re-design:
  - sharing between adjacent pixels, to save space
  - allows for increased counter depth:
    - 5 bit TOA (instead of 4)
    - 7 bit TOT (instead of 4)
- share TOA between adjacent pixels (to be discussed)
  - would make space for **10 bit TOT**
- on-board LDO
- PLL, band-gap blocks (RD53)
- features for daisy-chain
- bug fixes

- Launched sensor production for 256 x 256 CLICpix
  - (in anticipation of new chip version)
CLICpix power-pulsing + delivery requirements

Small duty cycle of CLIC machine allows for power reduction of readout electronics: turn off front end in gaps between bunch trains

Challenging requirements:
- Power budget $<50 \text{ mW/cm}^2$ average (air-flow cooling limit)
- High peak current $>40 \text{A/ladder}$
- Different timing analog/digital electronics
- High magnetic field 4-5 T
- Material budget $<0.1\% X_0$ for services+supports
- Regulation $<5\% \ (60 \text{ mV})$ for analog part

Figure 3: Analog and digital power consumption per ladder ($N=24 \text{ ASICs}$).

Assuming $t_{on}=15 \mu s$, $t_{r}=t_{f}=1 \mu s$ and $T=20 \text{ms}$, the average power consumption of the analog and digital electronics per cm$^2$ corresponds to 1.6 mW and 22.5 mW, respectively. This way of providing high power during small intervals and low power during the longest part of every period is referred as "power pulsing", and represent an efficient way to reduce the average power consumption down to the allowed level.

4. Regulation

The analog voltage required at the ladder is 1.2V, while the digital voltage could be lowered to reduce power consumption. To obtain higher efficiency and lower noise coupling, both will be supplied separately.

Powering the analog electronics is more challenging than the digital, as it has a higher consumption, a bigger current transient and it requires a better voltage regulation. As a CLICPix design specification, the voltage ripple for analog electronics should be within 50 mV in order to insure a stable Time-Over-Threshold (TOT) measurement [ref]. Along this paper we will propose a scheme for powering the analog electronics, while the digital implementation will be addressed in a future work.

Figure 4 shows the analog current shape for a whole ladder, which changes from no load to full load ($I_{max}=40 \text{A}$) in one microsecond.

The desired regulation is normally achieved by means of Power Distribution Network (PDN) theory [1]. Knowing the allowed voltage ripple and the maximum current, a target impedance is calculated using Ohm's law. The goal is to keep the impedance that the chips see looking into the PDN below this target impedance value over a wide frequency range, mainly defined by the bandwidth of the powered signal. The PDN is mainly formed of a voltage regulator module (VRM) that provides low impedance from DC up to few KHz regime, bulk capacitors (electrolytic, tantalum) at the frequency region up to 100KHz and multilayer ceramic decoupling capacitors up to the 100MHz range. Above this frequency, the impedance the chip sees is mainly inductive caused by the package and the only way to decrease it is using on-die capacitors.
CLICpix power-pulsing + delivery concept

Small duty cycle of CLIC machine → turn off front end in gaps between bunch trains, to reduce avg. power

- **Power pulsing** with local energy storage in **Si capacitors** and voltage regulation with **Low-Dropout Regulators (LDO)**
- **FPGA-controlled current source** provides small continuous current
- **Low-mass Al-Kapton** cables

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**Figure 3:** Analog and digital power consumption per ladder (N=24 ASICs).

- Analog: All ON
- Digital: All ON (N - 1) idle + 1 read out

- **Power-delivery + power-pulsing** design for **low mass**

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**Vertex-detector power consumption**

- **P[W]**
- **Bunch trains**
- **T = 20[ms]**

- **Digital**
  - All ON
  - (N - 1) idle + 1 read out
  - 2.4[W]
  - 0.54[W]

- **Analog**
  - All ON
  - All OFF
  - 48[W]
  - 0[W]

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C. Fuentes

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**September 29, 2015**

**Vertex + tracking R&D for CLIC**
CLICpix power-pulsing + delivery results

- Measurements on prototypes for digital and analog powering of ladders:
  - $I_{\text{ladder}} < 300 \text{ mA}$; $P < 45 \text{ mW/cm}^2$
  - Voltage stability: $\Delta V \sim 16 \text{ mV} \text{ (analog)}, \sim 70 \text{ mV} \text{ (digital)}$
  - $\sim 0.1\% X_0$ material contribution, dominated by Si capacitors
  - Can be reduced to $\sim 0.04\% X_0$ with evolving Si capacitor technology: $25 \mu\text{F/cm}^2 \rightarrow 100 \mu\text{F/cm}^2$

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Flex-Kapton + dummy-load setup:

analog power

\[ V_{\text{load}} = 1.2 \text{ V} \]
\[ V_{\text{Cap}} = 5.3 \text{ V} \]
\[ \Delta V = 16 \text{ mV} \]

Particular case $t_{\text{on}} = 20 \mu\text{s}$

\[ P_{\text{avg}} < 10 \text{ mW/cm}^2 \]

digital power

\[ V_{\text{load}} = 1.0 \text{ V} \]
\[ I_{\text{BE}} = 100 \text{ mA} \]
\[ I_{\text{load for 1 ASIC}} = 8 \text{ mA} \]
\[ 360 \text{ mA} \rightarrow 180 \text{ mA} \]

\[ V_{\text{Cap}} = 20 \text{ ms} \]
\[ V_{\text{Cap}} = 1.8 \text{ V} \]
Through-Silicon Vias (TSV)

Through Silicon Via (TSV): vertical electrical connection
→ eliminates need for wirebonds
→ 4-side buttable chips
→ increased reliability, reduced material budget

TSV project (ALICE, CLIC, ACEOLE, AIDA) with CEA-Leti
• 130 nm Medipix(RX) wafers, via-last process
• first phase: demonstrated feasibility
• on-going second phase: demonstrate good yield
• launched third phase: TSV with Timepix3 50 μm thickness

CEA-Leti via-last process flow

1. UBM deposition
2. Temporary bonding, thinning to 120 μm
3. via etching + isolation
4. Cu deposition + patterning
5. backside passiv. + UBM deposition
6. debonding + attachment to dicing tape

• 60 μm TSV diameter
• wafers thinned to 120 μm
• 5 μm copper layer for TSV

First Medipix3 image with TSV assembly (fish head):

Medipix3 redistribution layer

Cooling studies for CLIC vertex detector

• ~500 W power dissipation in CLIC vertex area
• spiral disks allow air flow through detector
• ANSYS Computational Fluid Dynamic (CFD) finite element simulation

→ air cooling seems feasible
• 5-10 m/s flow velocity, 20 g/s mass flow

Air flow through spiral endcaps

Temperature profile (FE simulations)

- Mass Flow: 20.1 g/s
- Average velocity:
  @ inlet: 11.0 m/s
  @ z=0: 5.2 m/s
  @ outlet: 6.3 m/s
Cooling: experimental verification

• built mock-up to verify simulations (temperature, vibrations)
• measurements on single stave equipped with resistive heat loads:
  • air flow
  • temperature
  • vibrations (laser sensor)
• comparison with simulation

Temperature increase: measurement + CFD simulation

F. Nuiry, C. Bault, F. Duarte Ramos, M.-A. Villarejo Bermudez, W. Klempt
Low-mass supports

- Aim for only ~0.1% X0 per layer for powering + supports
  → ~0.05% X0 for supports
- Evaluating various designs and materials based on:
  • Carbon-Fiber-Reinforced Polymers (CFRP)
  • Silicon-Carbide (SiC) foams
- Bending stiffness validated with calculations, finite-element simulations and measurements
Mechanical integration

- Detector integration: low-mass supports, services, assembly
- Taking into account constraints from powering and cooling
- Detailed material-budget calculations, comparison with simulation models

vertex-detector services

assembly scenario

material-budget calculation

F. Duarte Ramos, M.-A. Villarejo Bermudez