Mimoroma2 on the EUDET telescope @ CERN test beam

JRA1 meeting, 21 May 2008 DPNC Geneve

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1. **The Mimoroma2 chip**
   - **Brief description of chip and architecture**
2. **The testing tools**
   - **Mimoroma2 laboratory test set up**
   - **Sensor box**
   - **DAQ VME boards**
   - **Mechanical solution**
3. **Conclusions**

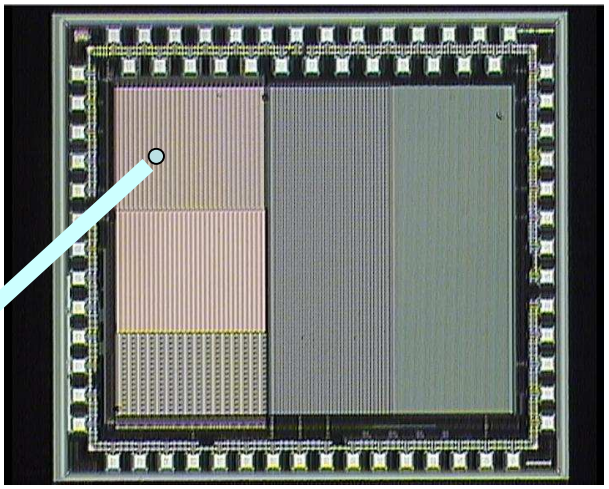
Mimoroma2 chip: main goals and constrains

More details on:
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=4&sessionId=5&confId=2564
http://www.roma3.infn.it/rictec/mimosa

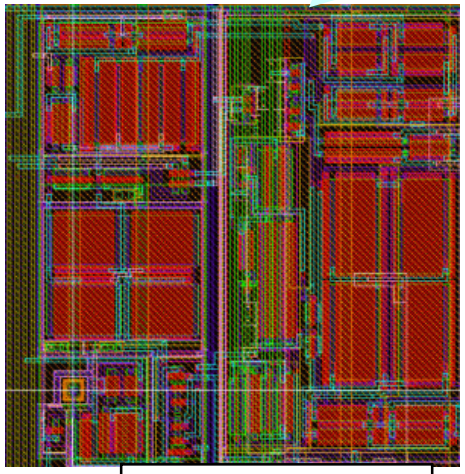
- Characterization of the signal (epitaxial thickness and quality) level provided by the STM 0.13 μm technology
- Implementation of an on-pixel sparsification architecture with **digital and analog output**

1. **Only NMOS transistors: no competing n-wells**
2. **Small available area (pitch 20-25 μm)**
3. **Common threshold for all pixels in a chip**
4. **Threshold voltage and curren mismatch in submicron CMOS**
5. **Noise:**
   - ❑ **Temporal noise**
   - ❑ **White and 1/f noise**
   - ❑ **Charge injection**
   - ❑ **Digital to analog cross-talk**

Chip mimoroma2 (STMicroelectronics 130nm technology)



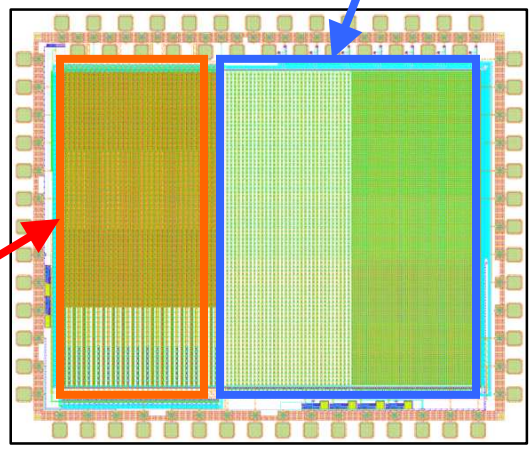
2 mm x 3 mm



25 μm x 25 μm

Non sparsified side

Sparsified side



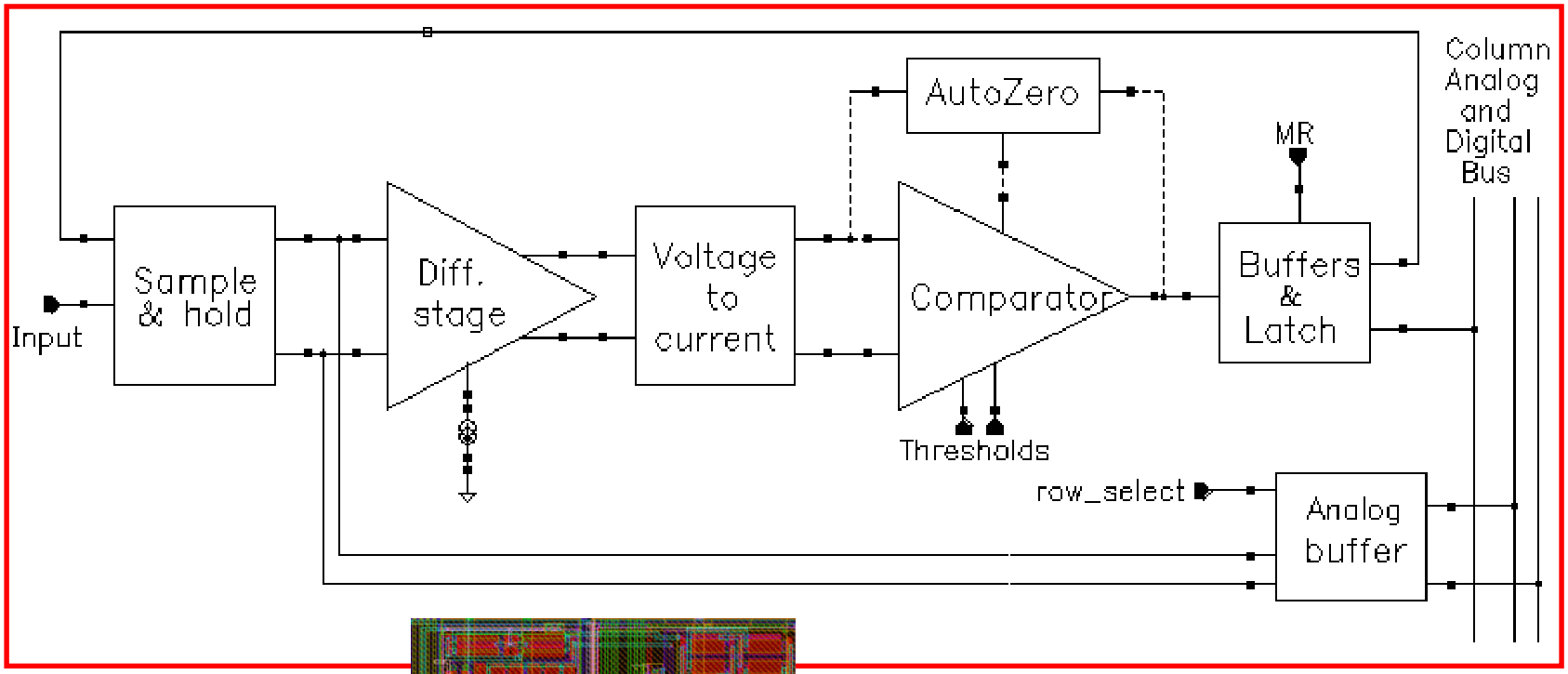
Technology characterization from the signal collection point of view
Different parameters for the non sparsified part of the chip

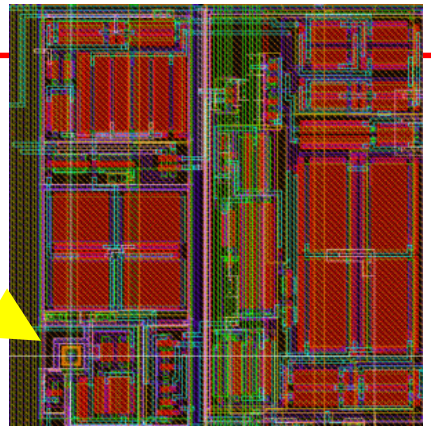
Ten different matrix implemented

- ✓ **Five 32x16 pixels arrays with 20x20 μm size**
- ✓ **Five 64x32 pixels arrays with 10x10 μm size**

Parameter	Value 1	Value 2
Pixel structure	3T	SB
Pitch	20 μm	10 μm
Diode dimension	1 μm x 1 μm	1.5 μm x 1.5 μm
SF transistor size	Small gain	Large gain
Power supply	2.5 V	1.2 V

Pixel architecture





Sensing diode

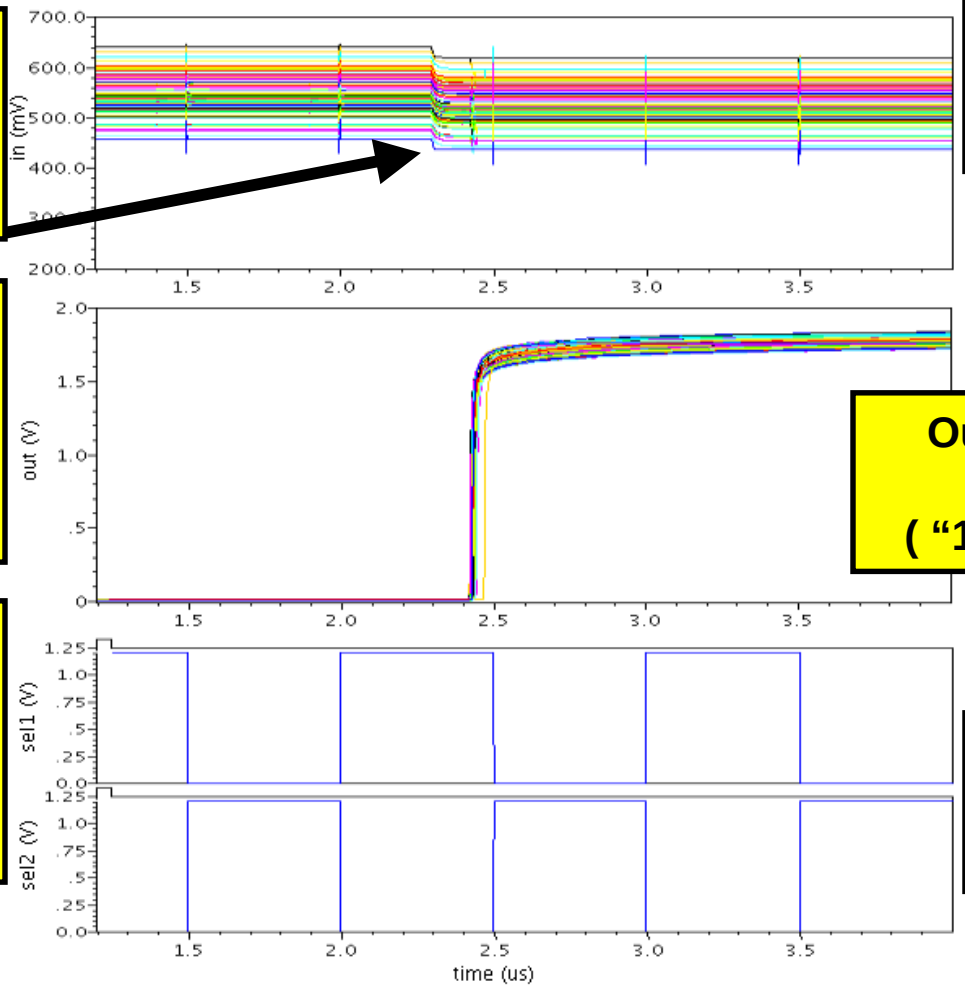
Size 25 μm x 25 μm
~ 70 transistors

Sparsification logic Montecarlo simulation (100 runs)

Input signal injected on sensing diode ~22 mV (~ 350 e)

~ 350 electron is a rough estimation of seed pixel charge in STM 0.13 μm

Treshold at the minimum value needed to have zero false trigger (“100% purity”)

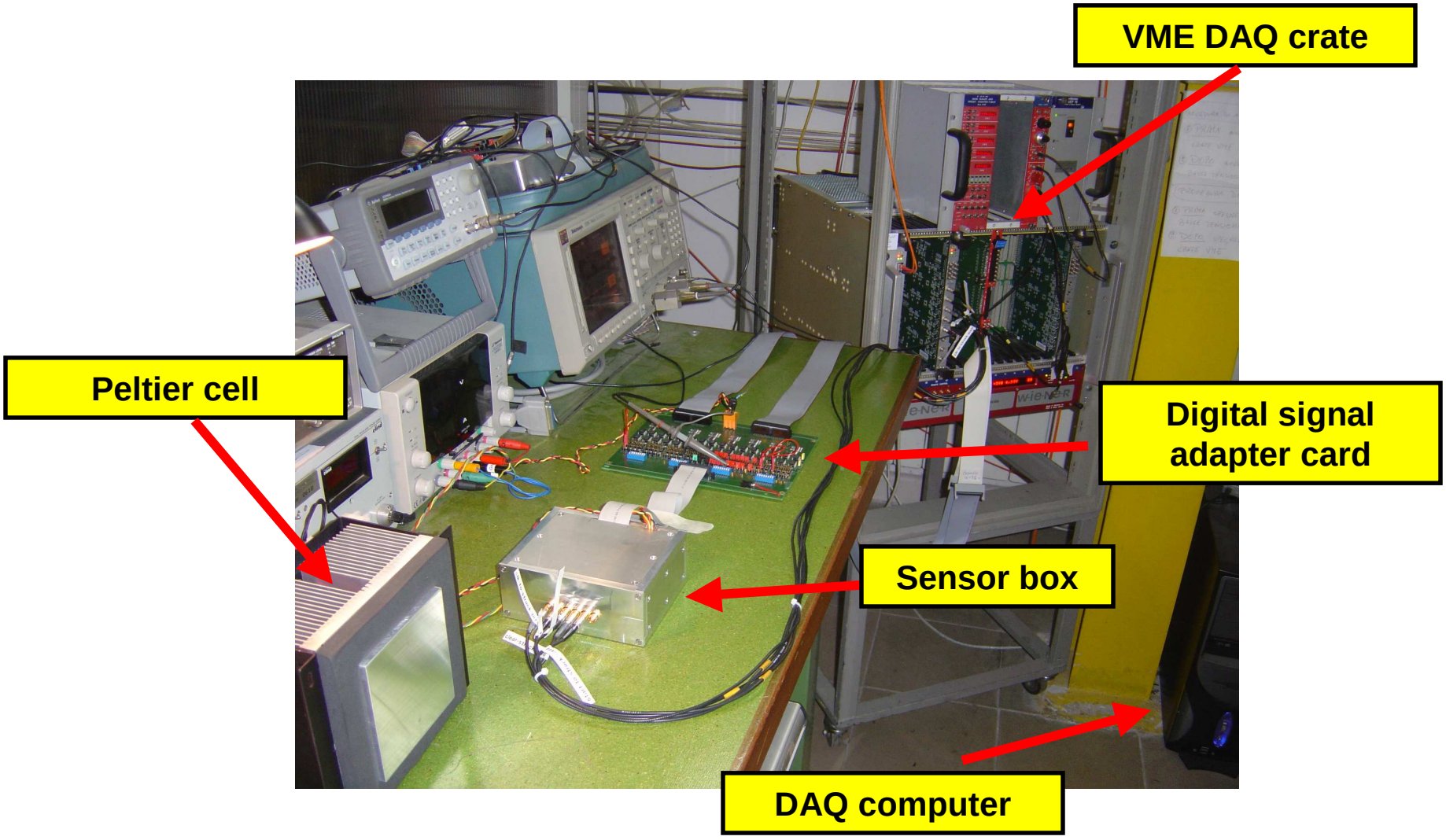


Mismatch spread on sensing diode ~182mV (~ 2900 e)

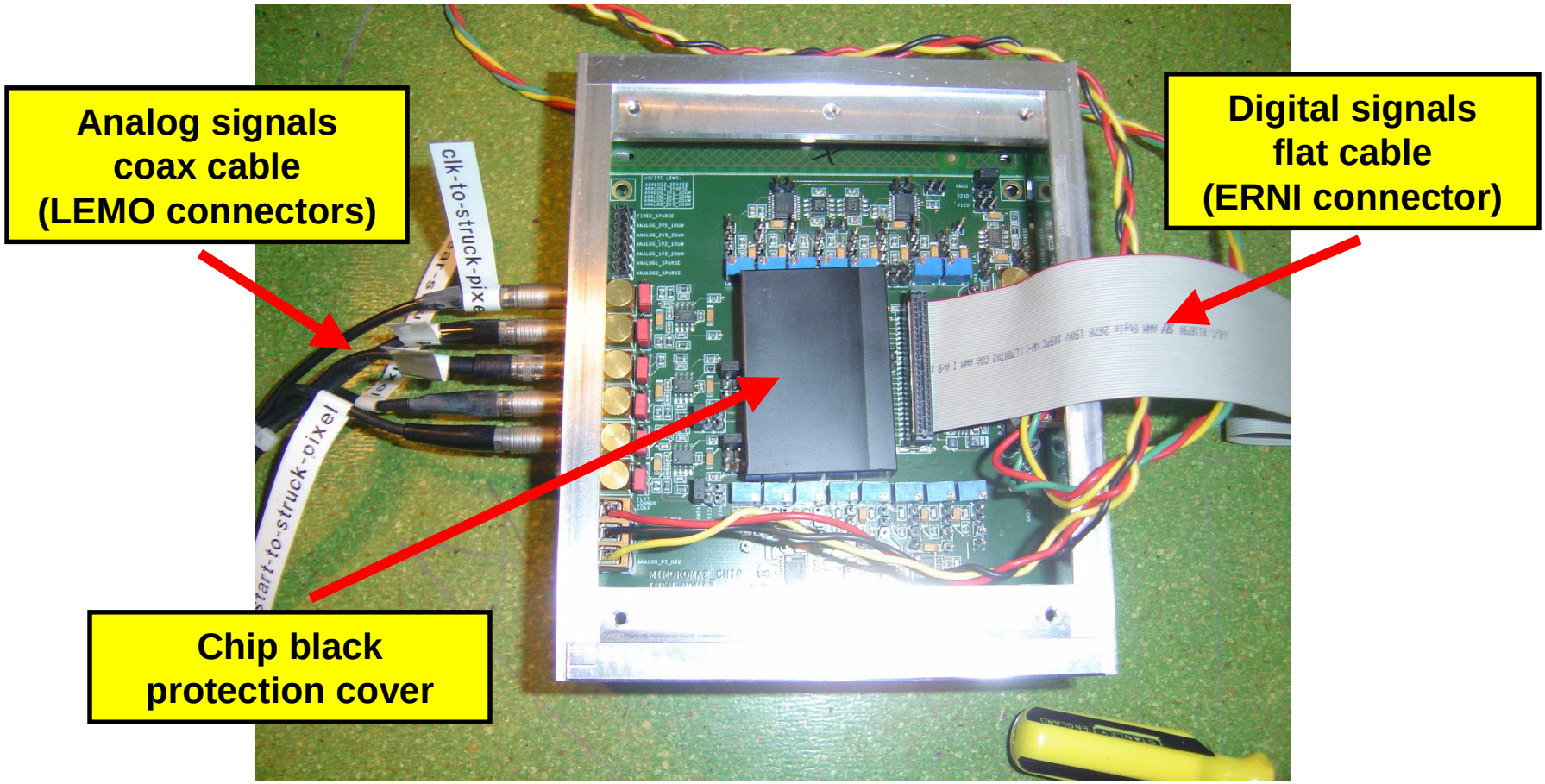
Output signal after discrimination (“100 % efficiency”)

Sample and hold timing (integration time)

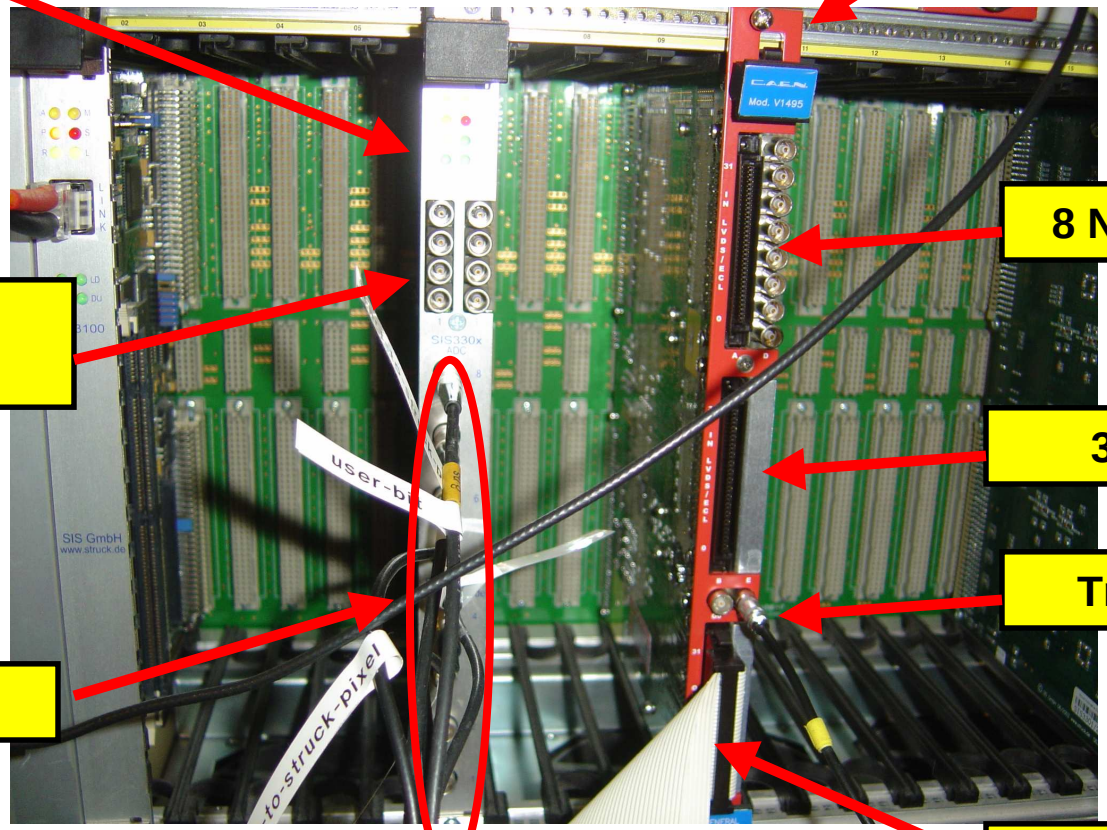
Mimoroma2 laboratory test set-up



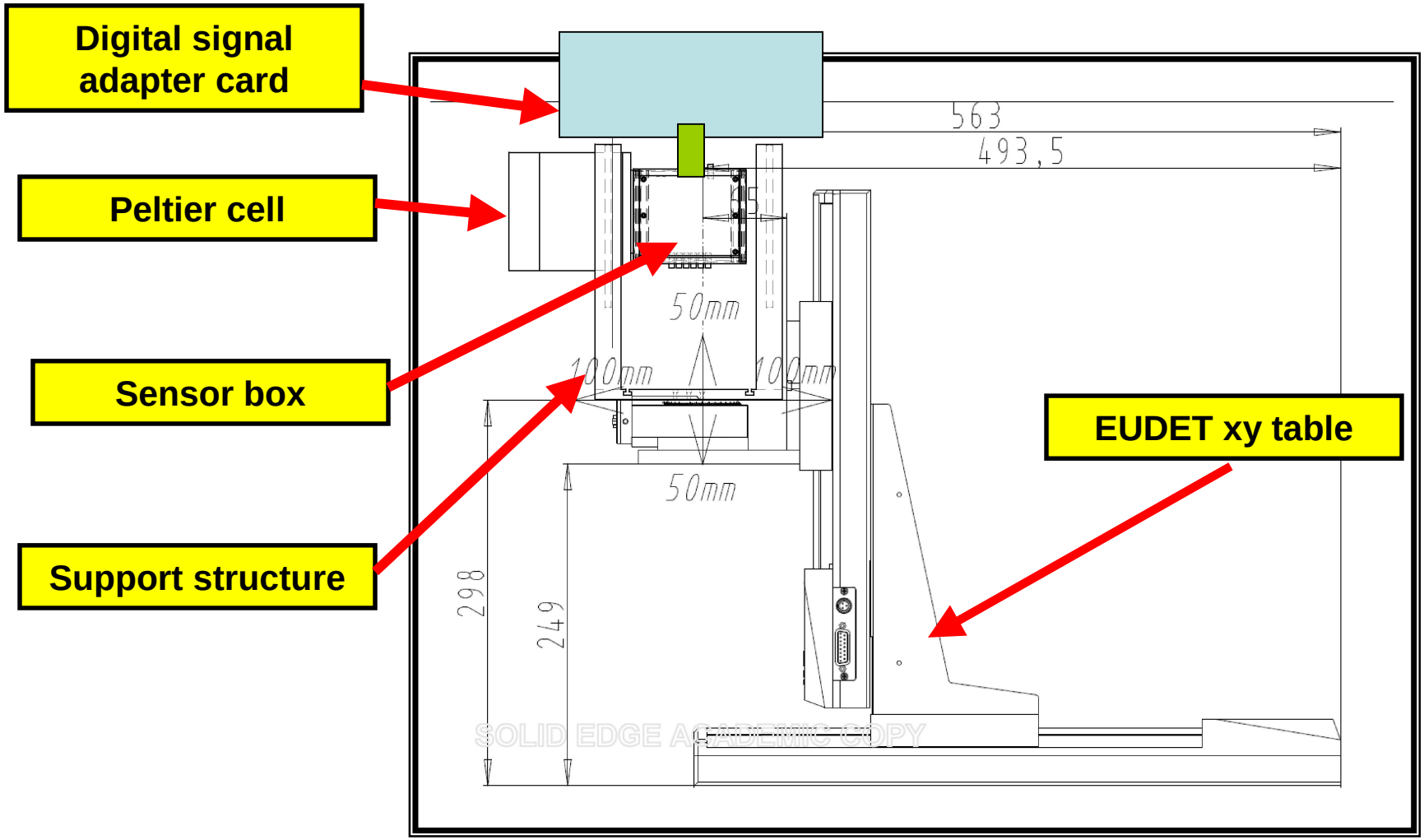
Sensor box


Analog signals
coax cable
(LEMO connectors)
Digital signals
flat cable
(ERNI connector)
Chip black
protection cover
clk-to-struck-pixel
start-to-struck-pixel

DAC VME boards



Mechanical solution



Conclusions

1. Lab chip testing just started (?)
2. Time schedule for August CERN test beam is tight
3. MIP data for STM 130nm next summer would be a must