The ATLAS Tile Calorimeter and its upgrades for the high luminosity LHC

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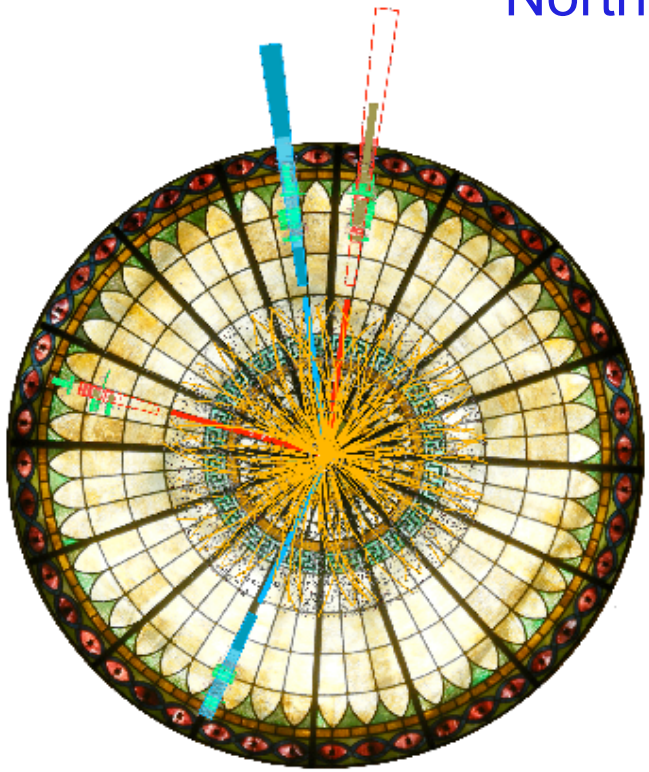

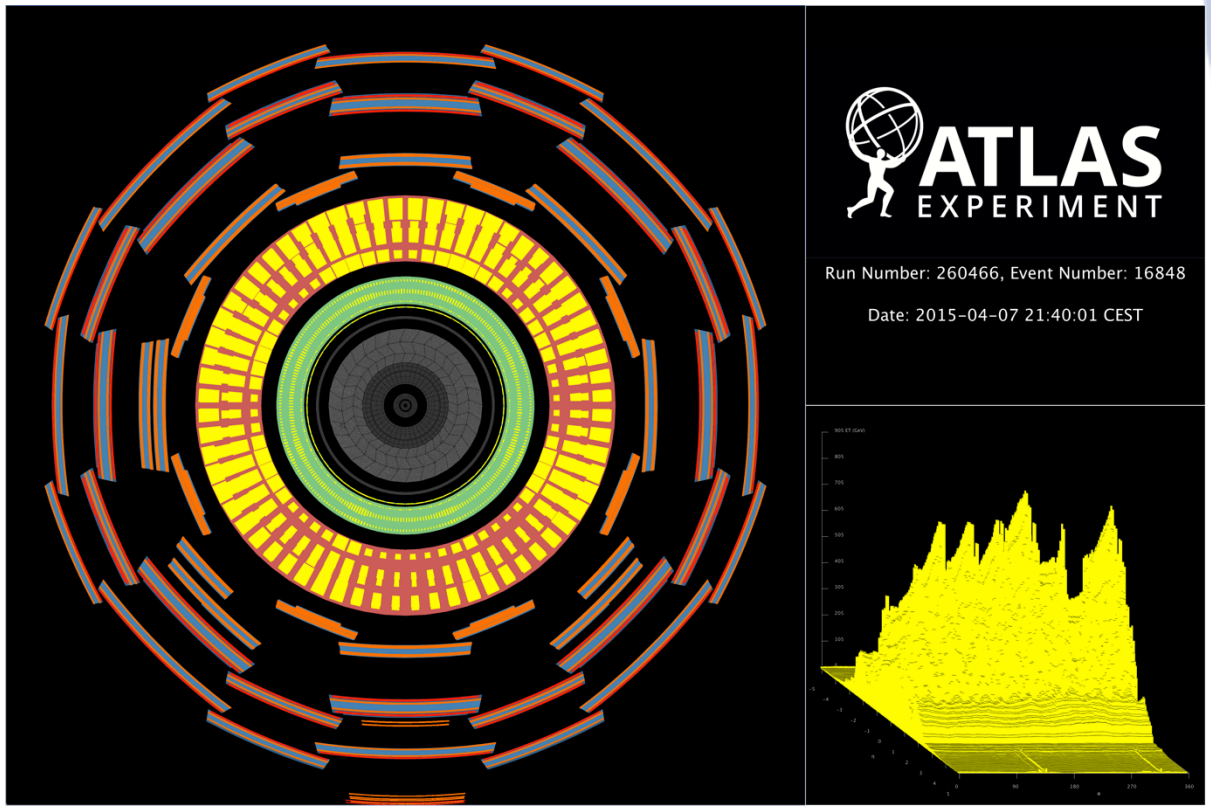

DIS 2015
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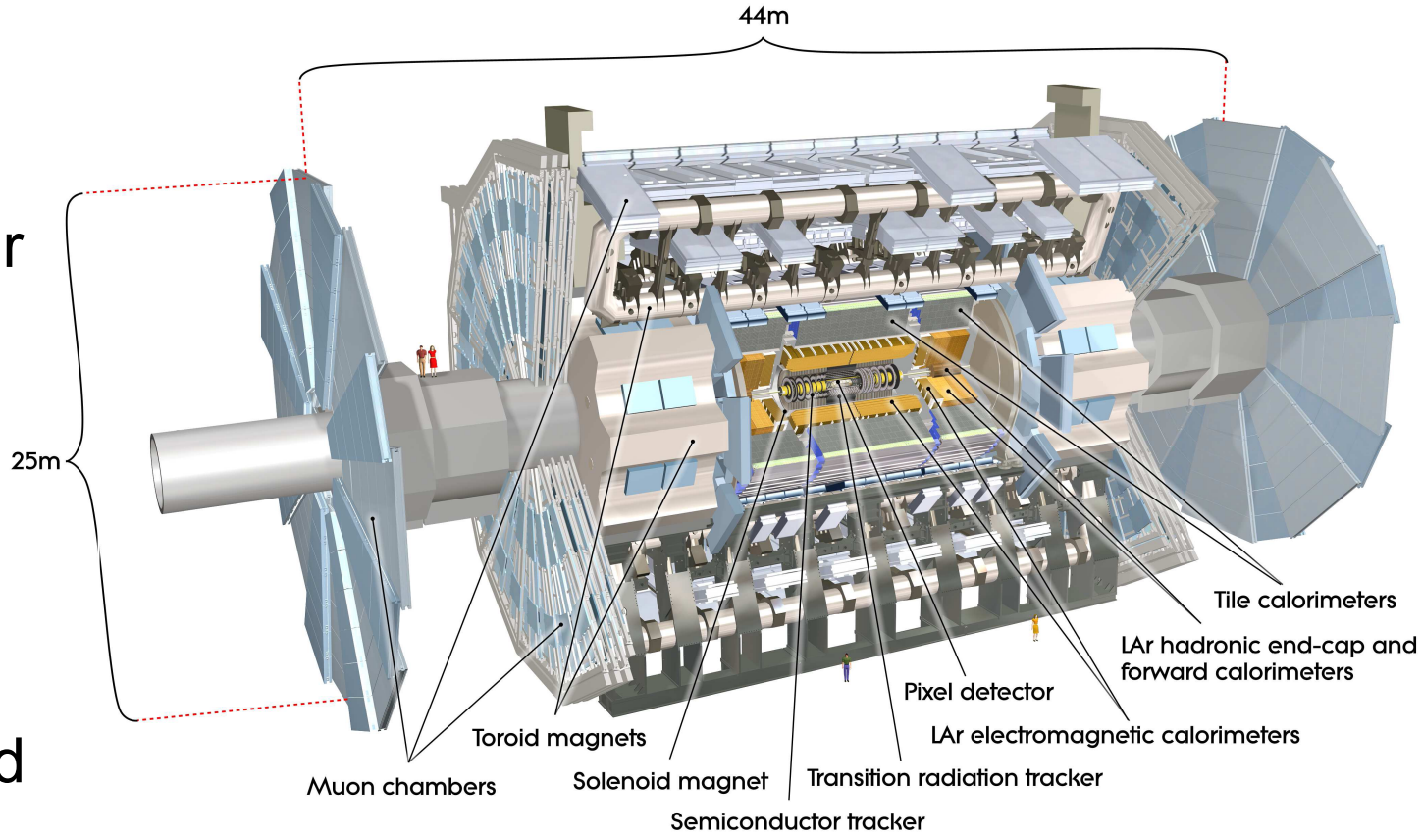
OUTLINE

- Introduction
- Tile calorimeter in ATLAS
- Performance during Run 1
- Pile-up, noise performance
- Electronics and upgrades
- Summary



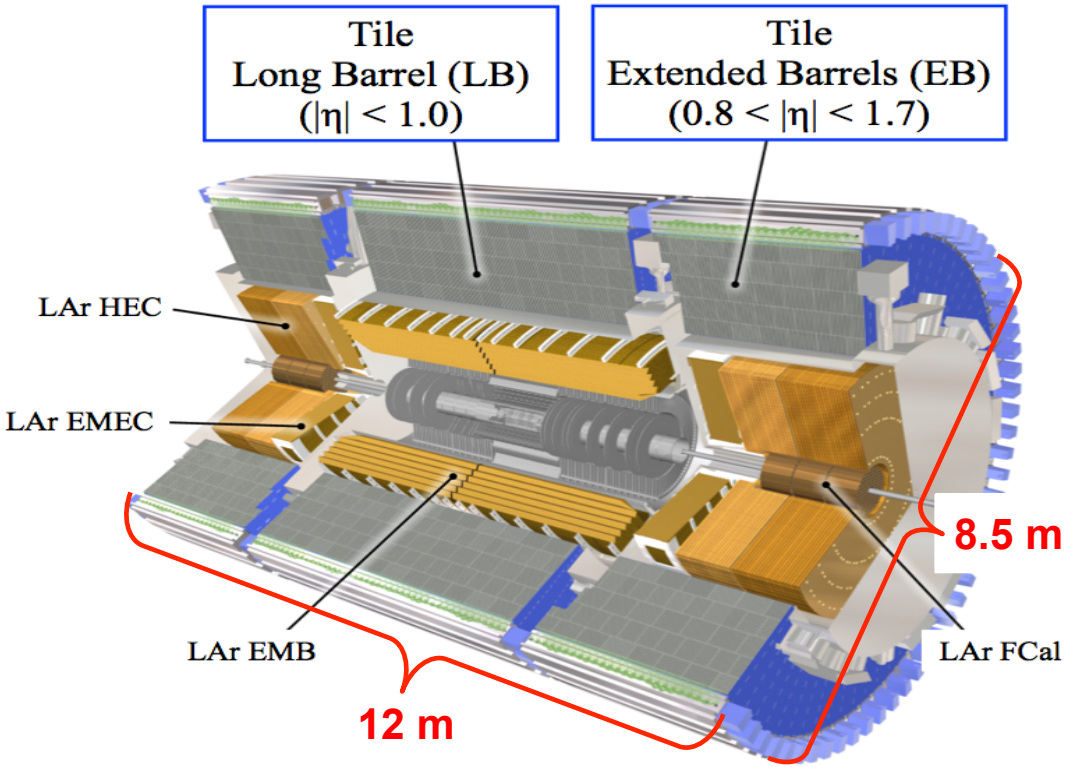
ATLAS Collaboration

Over 4000 collaborators
174 universities and labs
38 countries

Detector

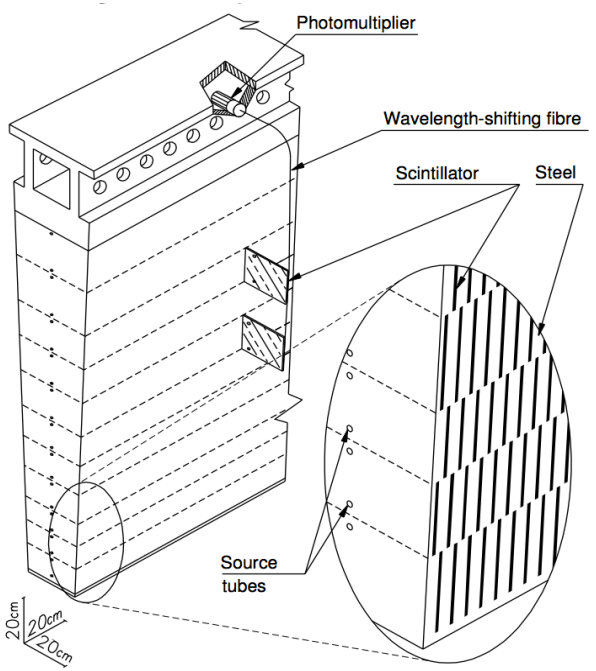
100 million channels
Weight: 7000 t
3000 km cables

The ATLAS Tile Calorimeter



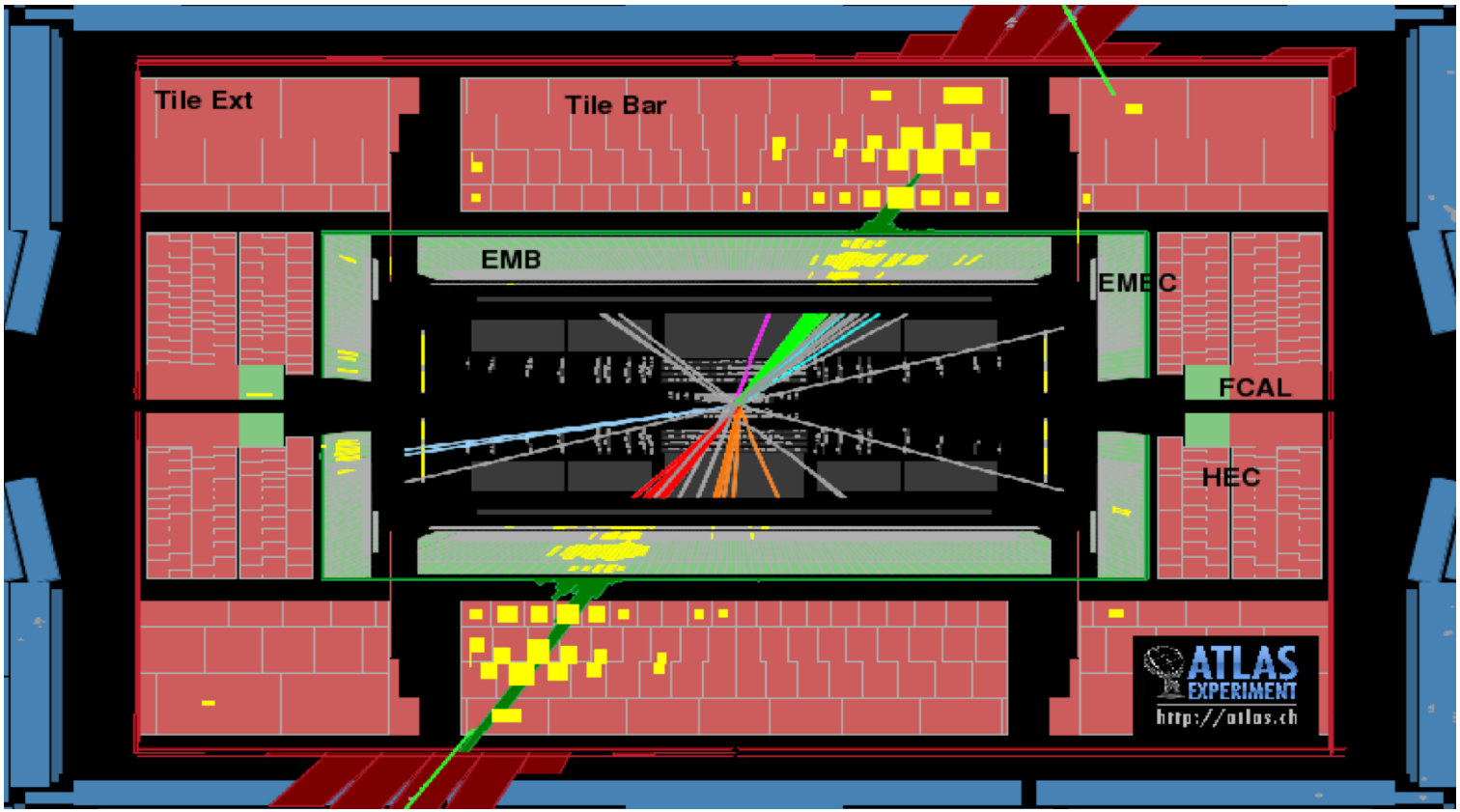
- Weight: 2900 t
- 256 modules, 9852 PMTs, 5198 cells
- 3 longitudinal layers : A, BC, D
- Thickness: 1.5, 4.1, 1.8 λ_{int} at η=0
- Additional layer E covers a gap between LB and EB
- 4 partitions EBA,LBA,LBC,EBC segmented in 64 wedge-shaped modules

- Steel absorber plates and rectangular **tiles** of plastic scintillator (cells)
- Front-end electronics located in the "super-drawer" - the outermost region of each module
- Wavelength shifting (WLS) fibers transmit the light produced in scintillators to the photomultiplier tubes (PMTs)
- Each cell is read out by 2 PMTs to reduce light attenuation dependence and achieve uniform response. Cell energy is the sum of energies measured in 2 channels

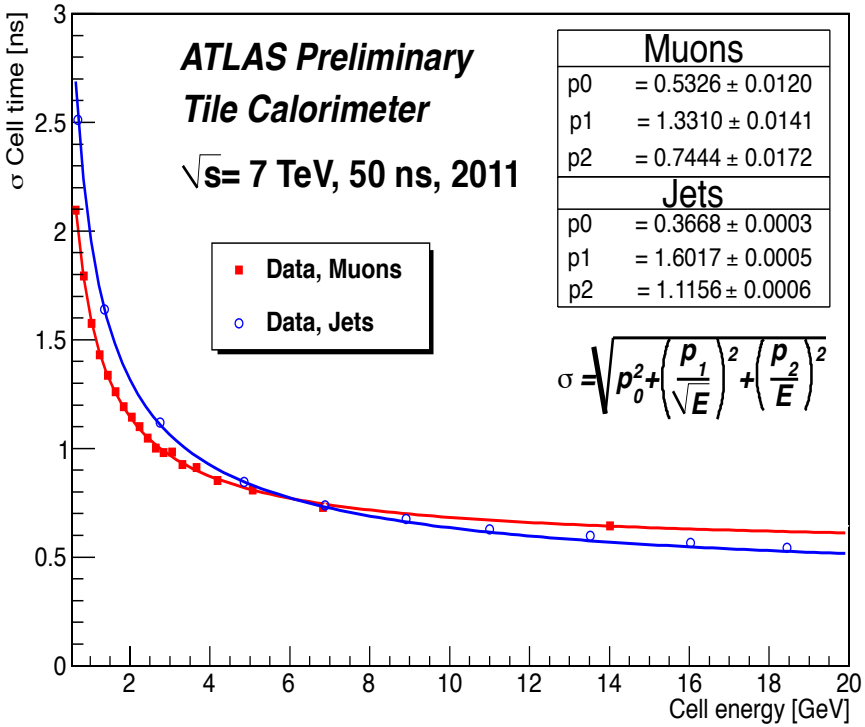


Capabilities of the Tile calorimeter

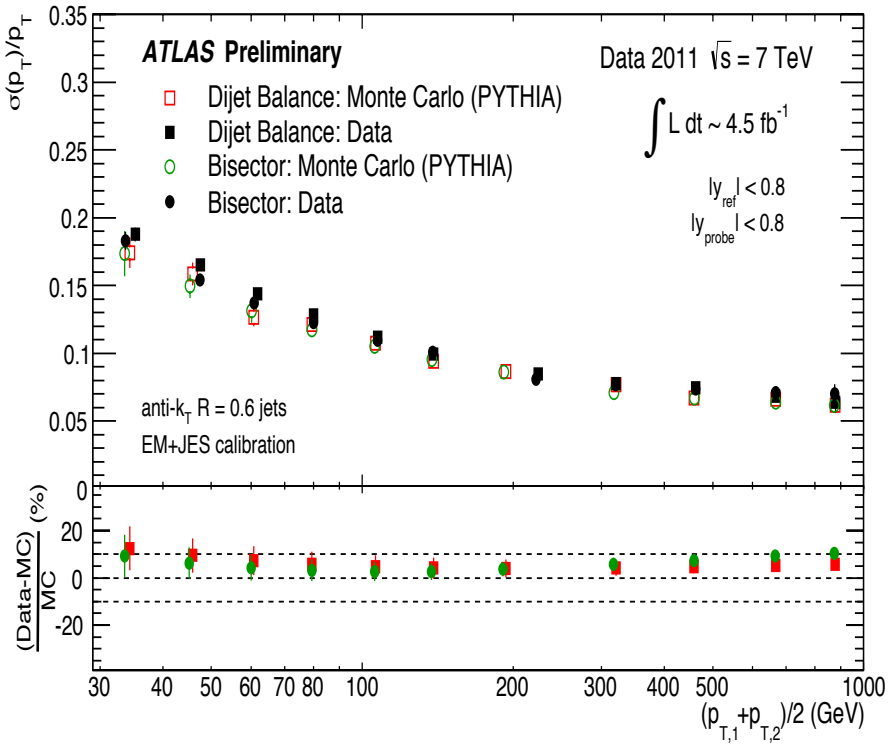
- Detection and measurements of hadrons, jets, leptons and missing transverse momentum
- Energy resolution for jets: $\sigma/E = 50\%/\sqrt{E} \oplus 3\%$
  - Linear within 2% (up to 4 TeV jets)



Energy and time resolution: jets

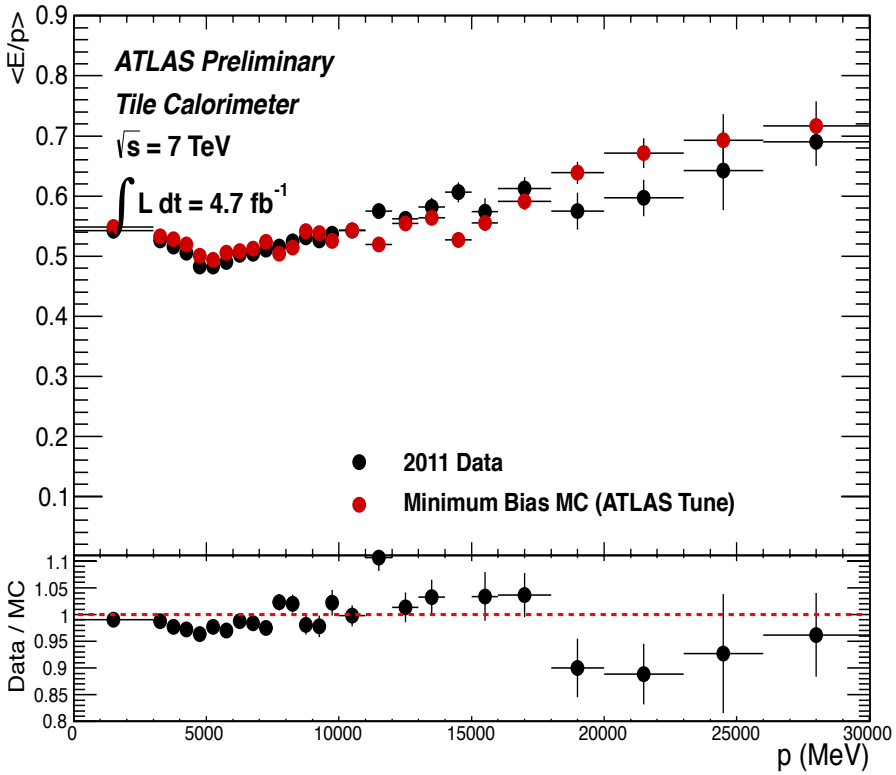


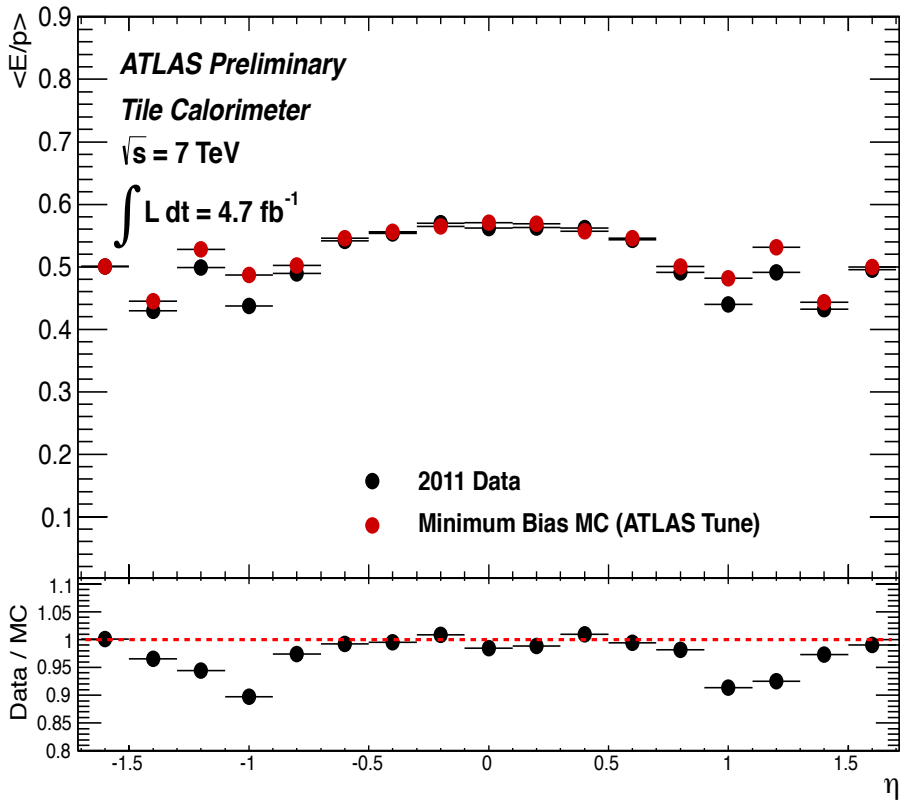
- Cell time resolution is measured as a function of cell energy in the 2011 collision data at √s = 7 TeV and 50 ns bunch spacing
- Muons : 0.75 ns for E ~10 GeV
- Jets : 0.55 ns at ~20 GeV



- Jet energy resolution as a function of the average jet transverse momenta measured with the di-jet balance and bisector in-situ techniques.
- The relative difference between data and MC is within ~10%

Performance with isolated hadrons

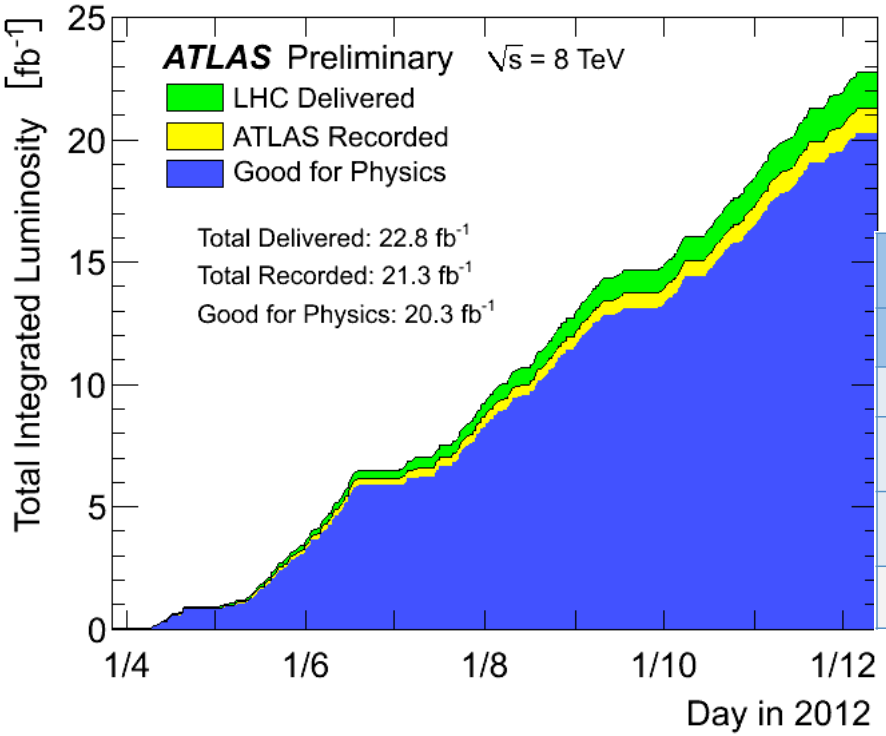




E/*p* v. *p* for hadronic tracks, √s = 7 TeV, 2011 data + MC

E/*p* v. η for hadronic tracks, √s = 7 TeV, 2011 data + MC

TileCal Run 1 data quality



ATLAS p-p run: April-December 2012

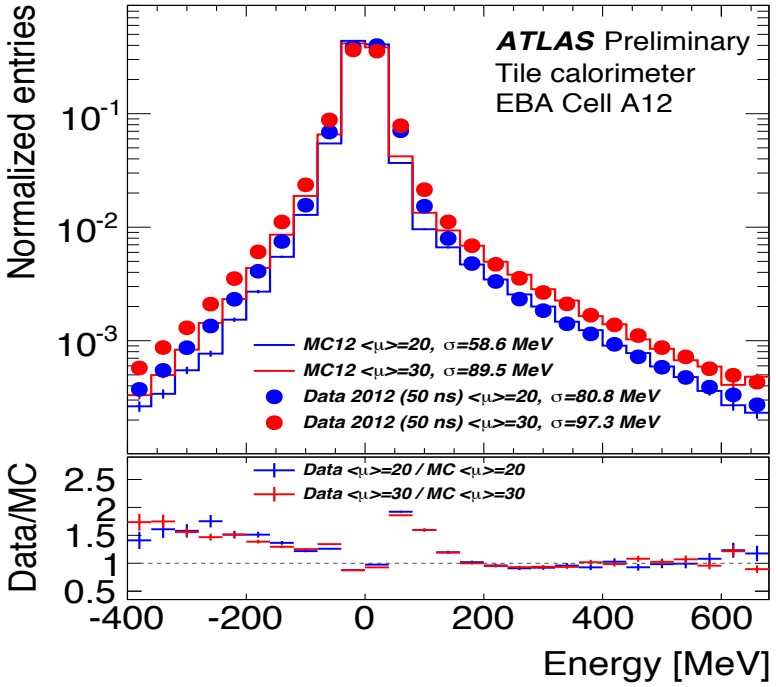
Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
99.9	99.1	99.8	99.1	99.6	99.6	99.8	100.	99.6	99.8	99.5

All good for physics: 95.5%

Luminosity weighted relative detector uptime and good quality data delivery during 2012 stable beams in pp collisions at √s=8 TeV between April 4th and December 6th (in %) – corresponding to 21.3 fb-1 of recorded data.

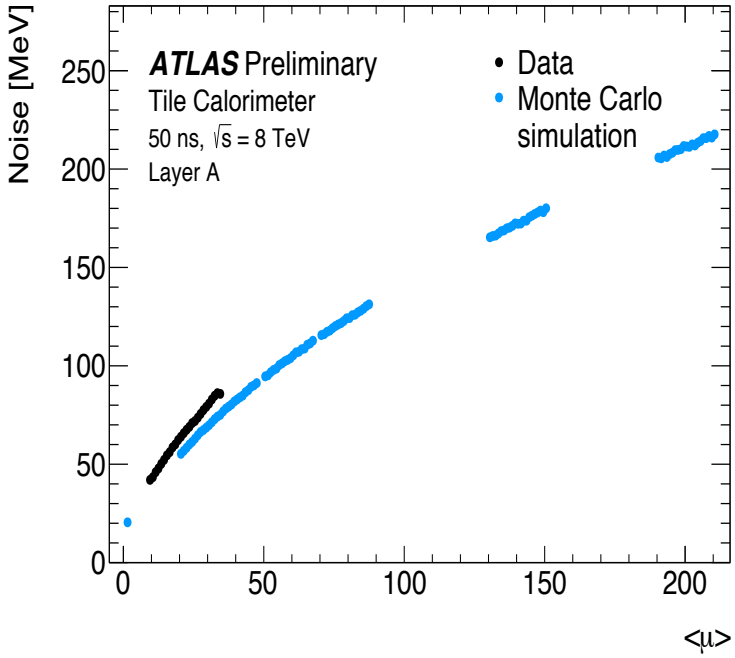
Tile data quality efficiency for *p-p* collisions in 2012 was 99.6% (2011: 99.2%, 2010: 100%)

Pile-up noise performance, Run1

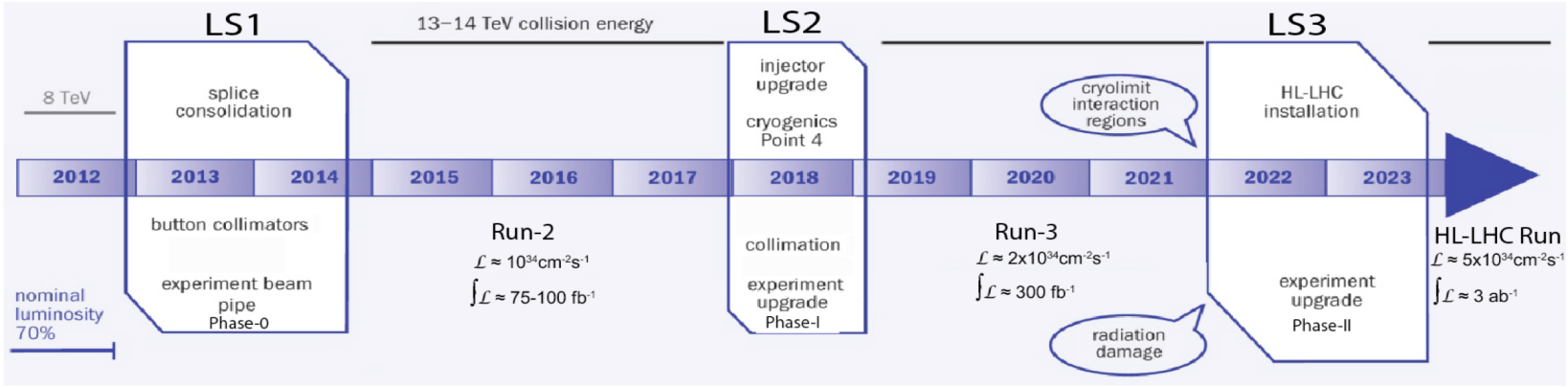


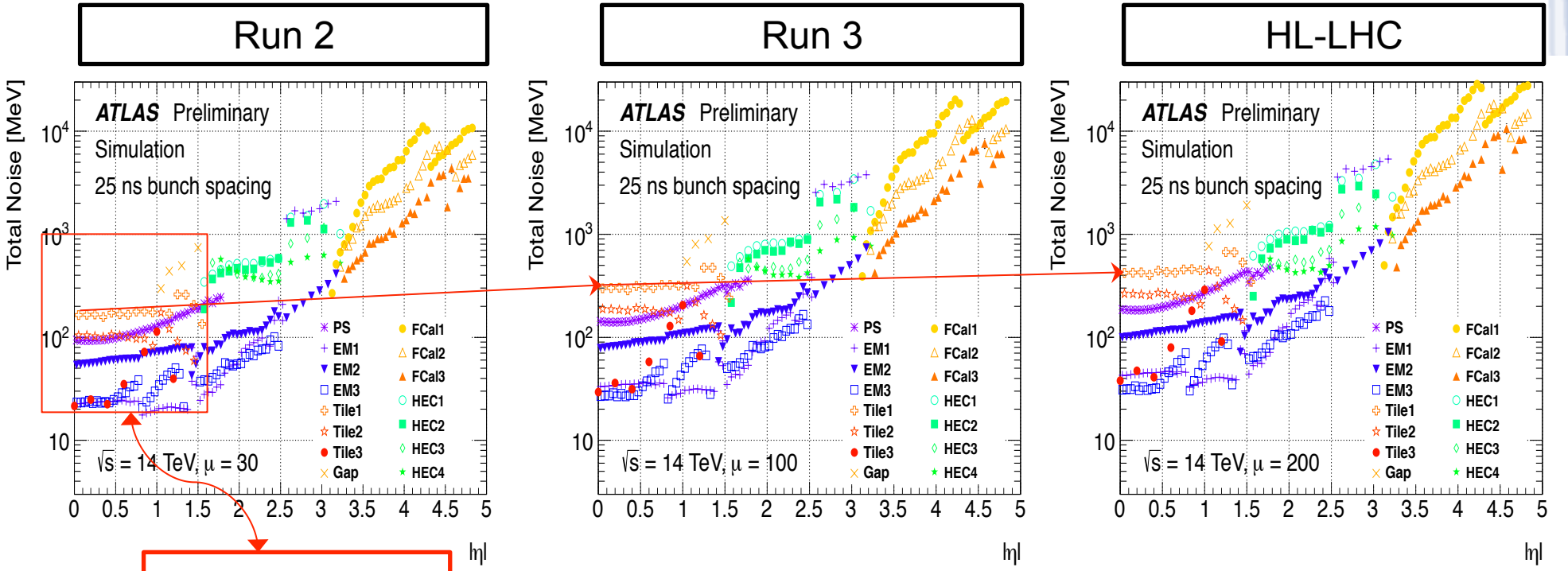
- Energy distribution for 50 ns data and simulation at √s = 8 TeV for the layer A cell with 1.1<η<1.2
- 2 different pile-up conditions with <μ>=20 (blue) and <μ>=30 (red).
- A reasonable agreement between data and MC above 200 MeV

- In the region where data and Monte Carlo simulation overlap a good agreement can be seen, with the largest difference at ~15 MeV.
- Noise comparison as a function of the mean number of interactions per crossing in the layer A at 8 TeV, 50 ns.

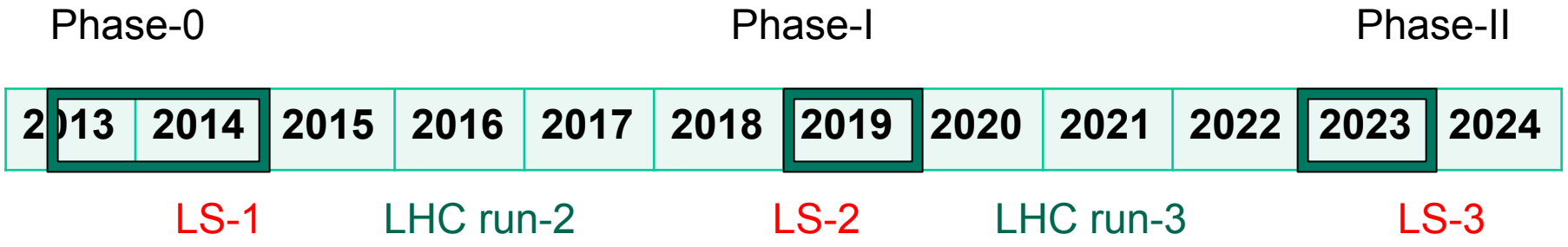


Expected noise performance





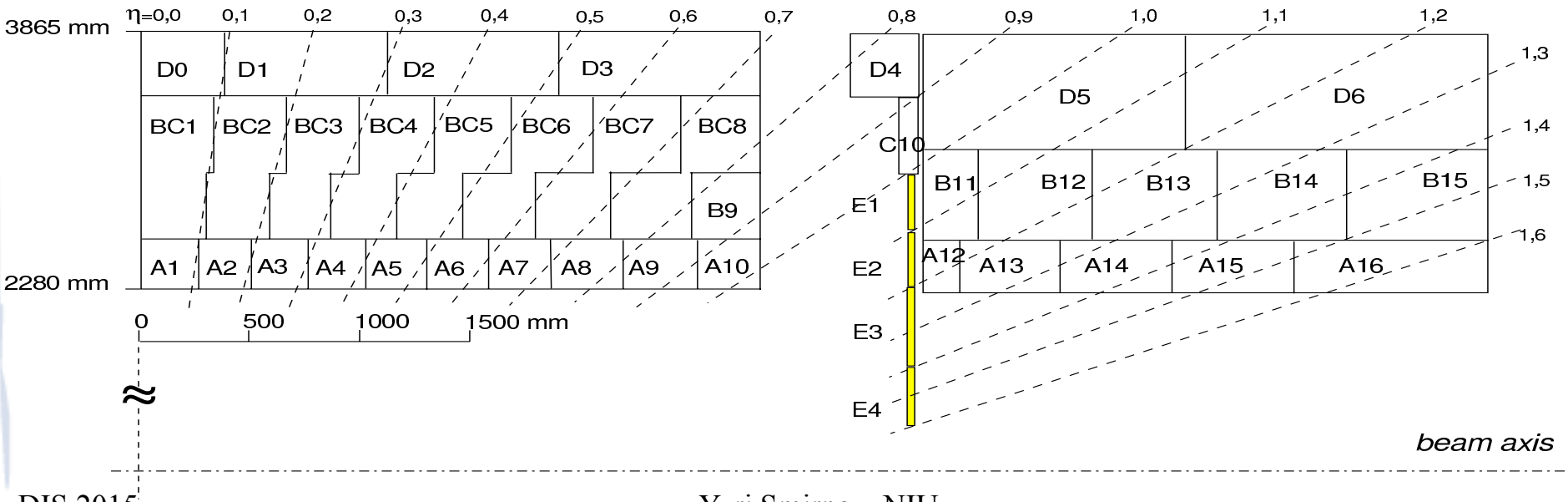
Tile Calorimeter upgrade timeline



- Run-1 (2009-2012): redesign LVPS on test 40 units
- Phase-0 (2013-2014): install new LVPS, MBTS, maintenance of FE boards, Tile 3rd layer in the Muon Trigger logic for $1.3<|\eta|<1.5$
- Phase-I (2019): replacement of gap scintillators
- Phase-II (2023): complete upgrade of the FE and BE electronics for High Luminosity LHC (HL-LHC) – details presented on next slides

Tile upgrade activities during LS1

- Completed the replacement all Low Voltage Power Supplies by new versions
- Updated the Cesium system mechanical structure
- Updated the Laser system to improve the light mixing to avoid non-uniformities in light distribution, more precise constants
- Modified Front-end electronics for E1-E4 cells to improve calibration constants
- Installed previously missing 8 (of 64) E3 and 8 (of 64) E4 counters per EB absent in Run 1 (due to MBTS readout)
- Will use TileCal D-layer with muon trigger system coincidence to reduce muon trigger fake rate

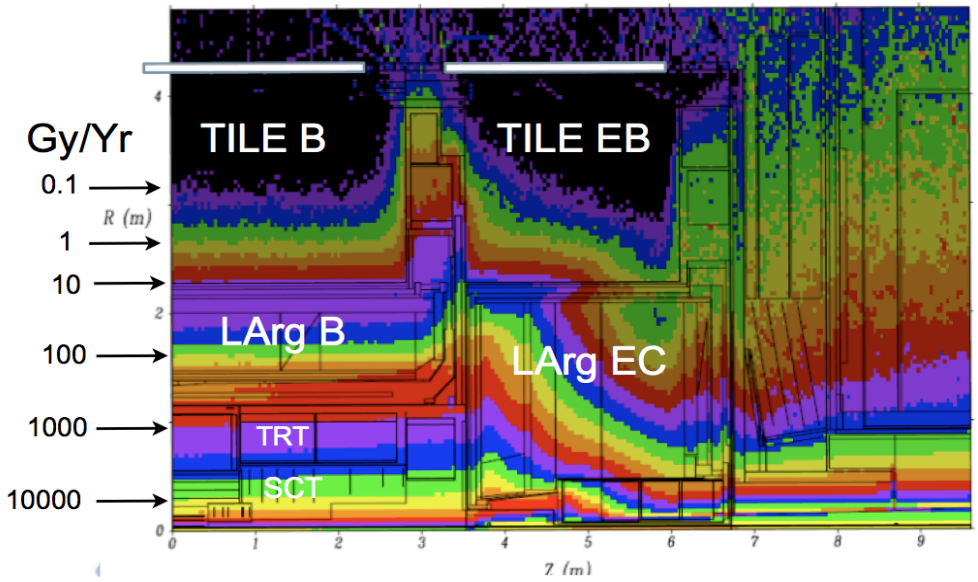


TileCal upgrade for HL-HLC: motivation

- LHC upgrade in 2023 aim:
  increasing the luminosity by factor of 10
  (5-7.5*10^{34} $cm^{-2}s^{-1}$ + luminosity leveling)
  - More events accepted with current criteria
  - More data generated ~500X
  - Better precision and granularity needed for triggering and event selection
- Ageing of components and need for faster output speed (100 kHz ➔ 40 MHz)
- Need better radiation tolerance
  - Single Event Effects
  - Non-Ionizing Energy Loss
  - Total Ionizing dose
- Simplify and reduce maintenance needs, improve the reliability

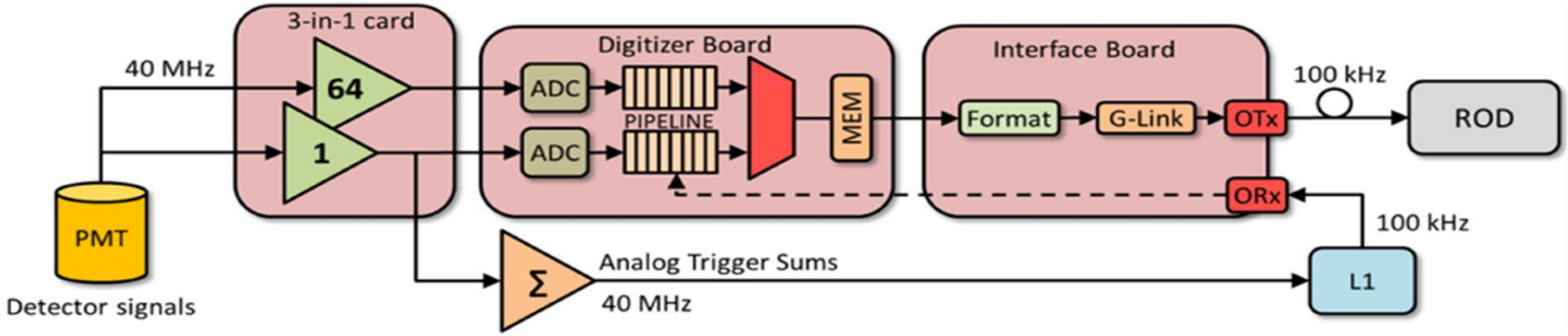
	Present	Phase-II
Total data rate	~165 Gb/s	~80 Tb/s
Fiber optic links	256	4096
BW per SuperDrawer	640 Mb/s	160 Gb/s

TID simulation (design Luminosity)

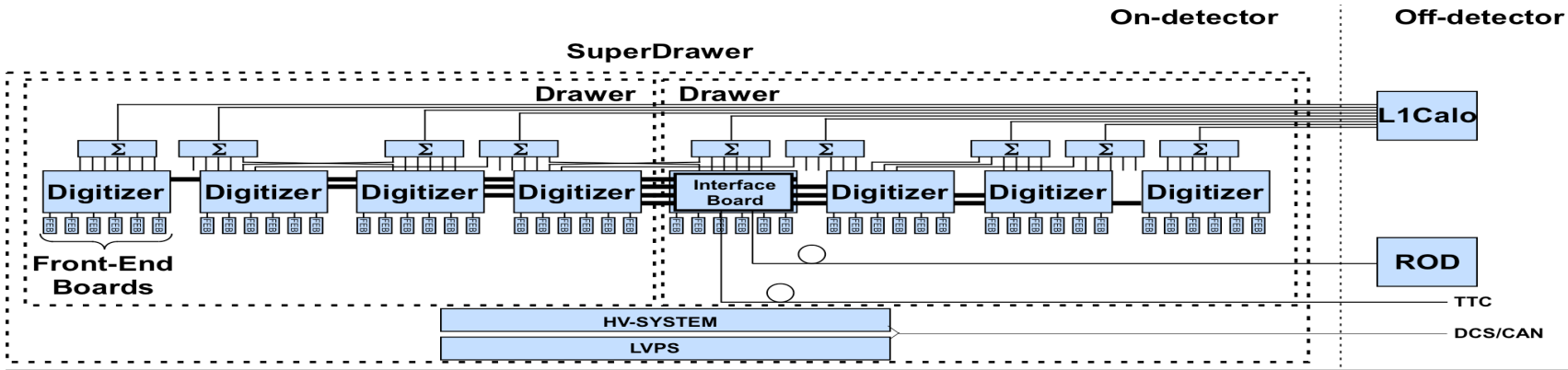


Phase 2 Radiation Tolerance Requirements (Estimate), TileCal HV Opto					
Type	Simulated Dose/Yr	Simulation Safety Factor	Low Dose Rate Safety Factor	Lot Variation Safety Factor	Total 10 Year Operation
TID	8.13E-01 Gy/yr	1.5	5	4	2.44E+02 Gy
NIEL	7.62E+10 n/cm²/yr	2	1	4	6.10E+12 n/cm²
SEE	1.85E+10 p/cm²/yr	2	1	4	1.47E+12 p/cm²

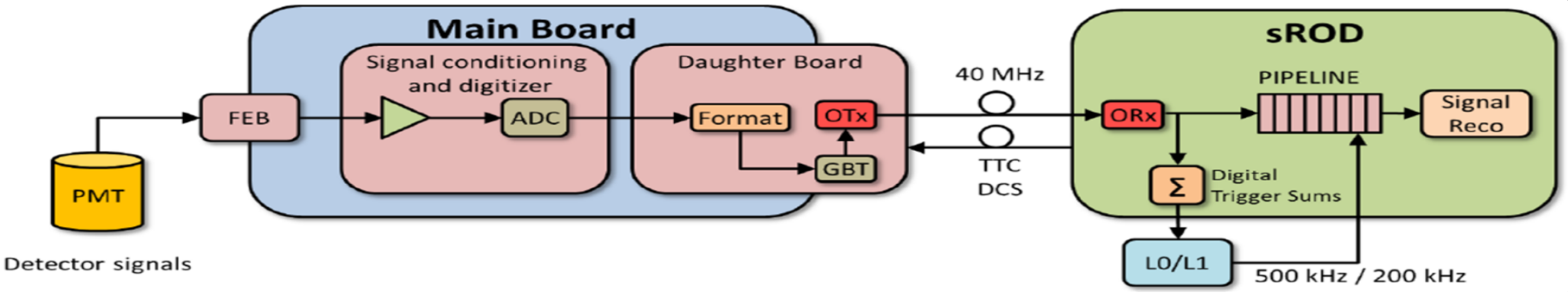
Read-out system: current architecture



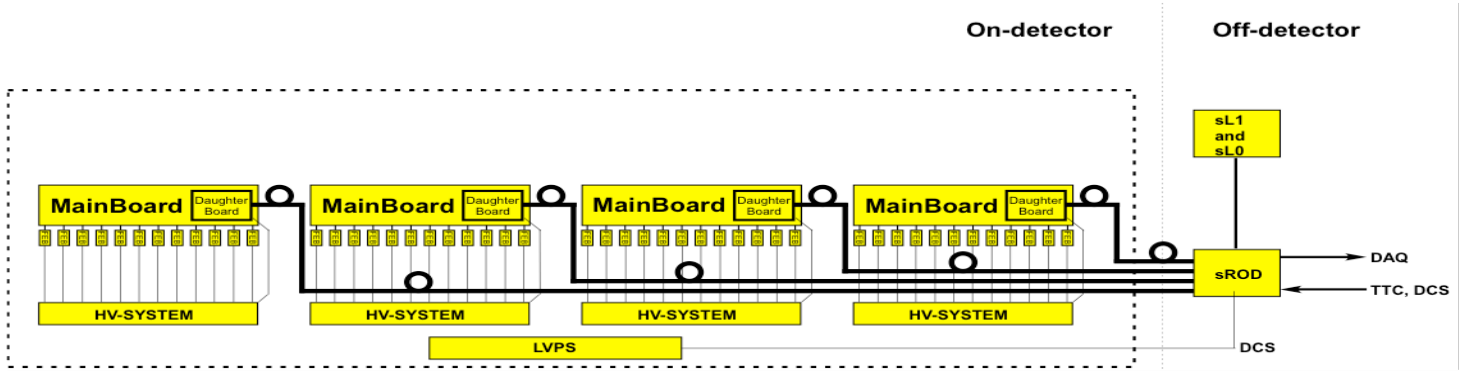
- 3-in1 FE board: shaping, amplification, integration. Trigger sums have 1 GeV energy precision
- Mother board: programming and powering of FE boards
- Digitizer cards: digitization, pipelines
- Interface card: OTx to the ROD at 100 kHz



Read-out system: Phase-II architecture

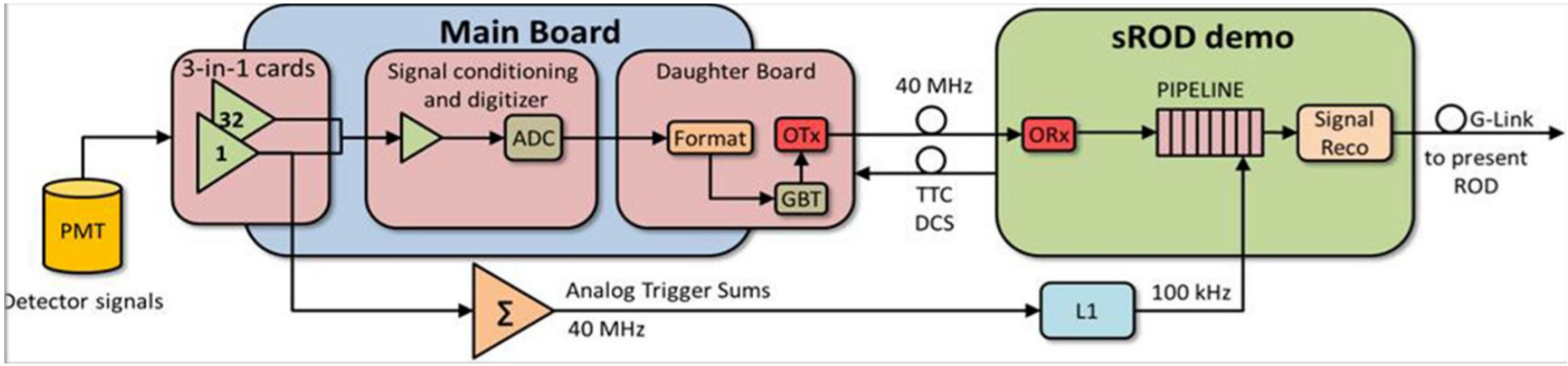


- Simplification: reduced number of boards and less inter-connections
- Front-end board: three options available
- Main board: conditioning and digitizer
- Daughter board: high speed optical communication for transmission of full data at 40 Mb/s to sROD
- sROD: pipelines and de-randomizers. Data information for the LVL0/LVL1 trigger system.
- Finer grain modularity: 1 SD splits in 4 independent mini-drawers with fully redundant data path, powering, internal cooling. Improves operation, maintenance and handling.



The demonstrator project

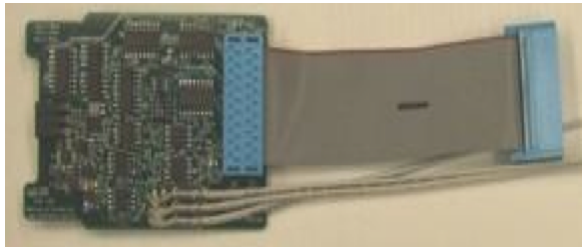
- Evaluation of the design and technology before the complete replacement of the associated electronics
- Similar as possible to Phase-II system while fully compatible with the present system
- Hybrid of the current and future architectures
- Provide both analog and digital trigger output
- The sROD system will interpret the Trigger Timing Control (TTC) and the Detector Control System (DCS) commands and translate new detector data into a form acceptable by the present ROD
- Planned insertion in Tile Calorimeter in 2015-2016



Front-end electronic board options

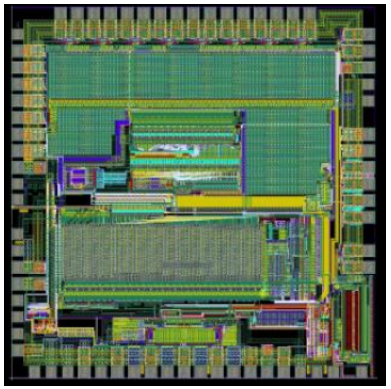
Modified 3-in-1

- Receive and shape
  - Provides analog output (2 gains)
  - Charge injection
  - Integrator
- Based on current 3-in-1 cards
  - Commercial off the shell
- 17-bit dynamic range
- Improved
  - Radiation tolerance
  - Noise performance
  - Linearity performance



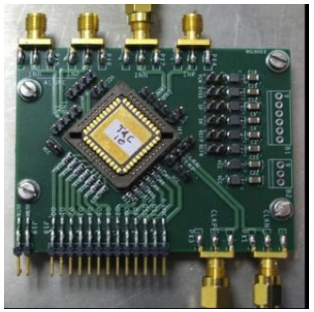
QIE ASIC

- Charge Integrator from Fermilab
- Different approach
  - Current splitter
  - Gated integrator
- Four different gains, but without shaping
  - No dead time
  - Useful for pile-up
- 17-bit dynamic range
- Clean measurement every 25 ns (40 MHz)



FATALIC

- Combines two ASIC solutions: FATALIC (Front-end for ATLAS TileCal Integrated Circuit) and TACTIC (Twelve bits AdC for atlas Tilecal Integrated Circuit)
- FATALIC
  - Shaping stage with 3 gain ranges (1, 8, 64)
  - 18-bit dynamic range
- TACTIC
  - 12-bit pipelined ADC
  - 40 MHz operations



Summary

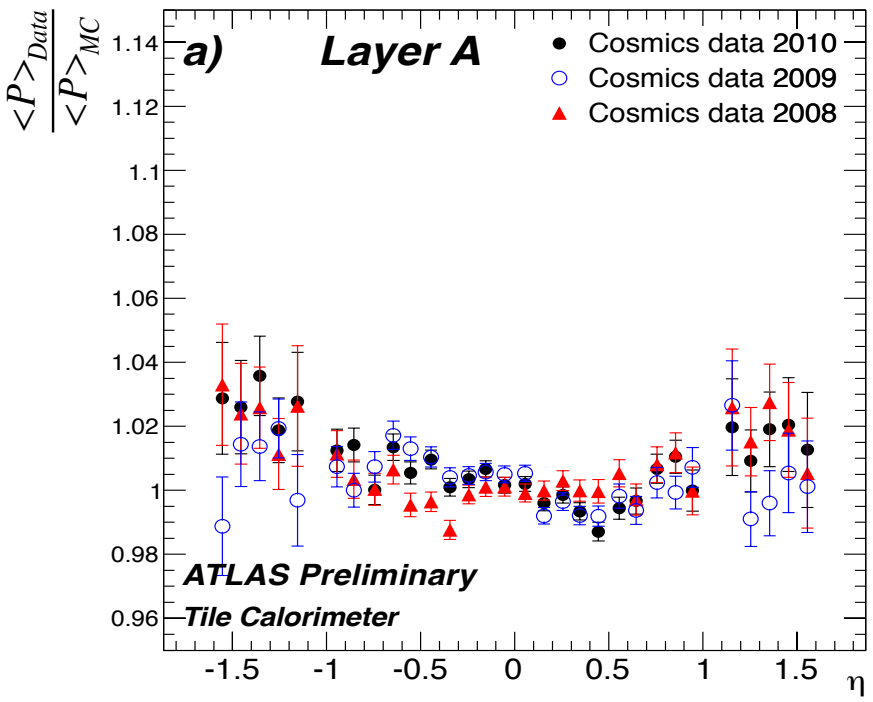
- The ATLAS Tile Calorimeter performed extremely well in LHC Run1 (data quality efficiency ~99.6%)
- This performance was crucial for SM measurements, new physics searches, and the discovery of the Higgs Boson
- Overall electromagnetic scale of Calorimeter known to within 3%, time resolution <1 ns, good agreement between data and MC for minimum bias data, single muons and hadrons
- Tile Calorimeter electronics upgrade is on schedule to maintain the strong performance under pile-up conditions of the HL-LHC

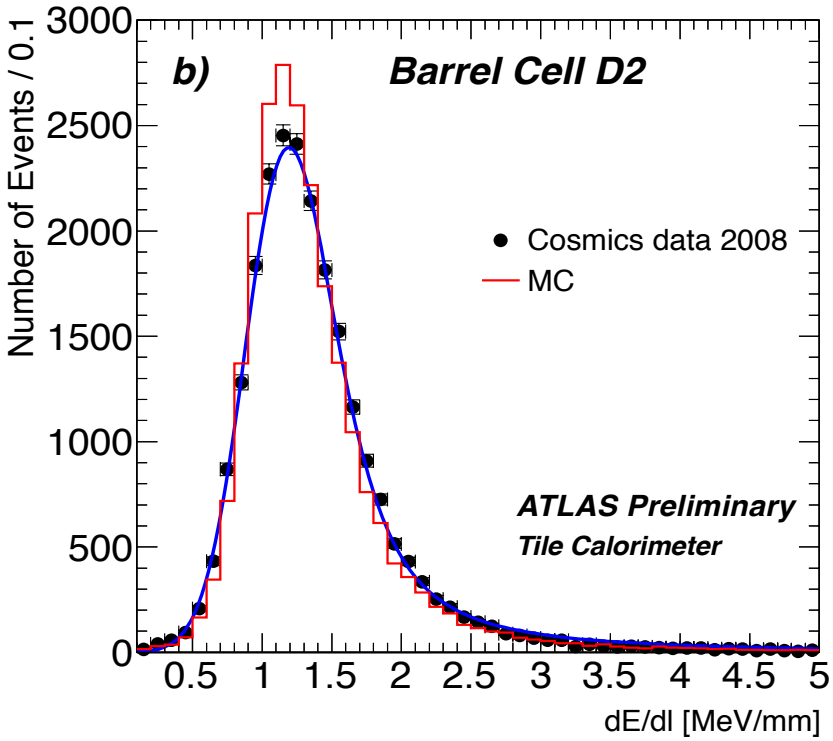
EXTRA SLIDES

Abbreviations and symbols

- ADC - Analog-to-Digital Converter
- ALARA - As Low As Reasonably Achievable
- ATCA - Advanced Telecommunications Computing Architecture
- DCS - Detector Control System
- EB - Extended Barrel
- FEB - Front End Board
- FMC - FPGA Mezzanine Card
- FPGA - Field Programmable Gate Array
- GBT - Giga Bit Transceiver
- HL-LHC - High Luminosity Large Hadron Collider
- LB - Long Barrel
- LVL0 - Level-0 trigger system
- LVL1 - Level-1 trigger system
- LVPS - Low Voltage Power Supply
- MBTS - Mini Bias Trigger Scintillator
- ORx - Optical Receiver
- OTx - Optical Transmitter
- ROD - Read Out Driver
- sROD - super Read Out Driver
- TTC - Trigger Timing Control
- μ - number of overlaying interactions (pile-up) per bunch crossing

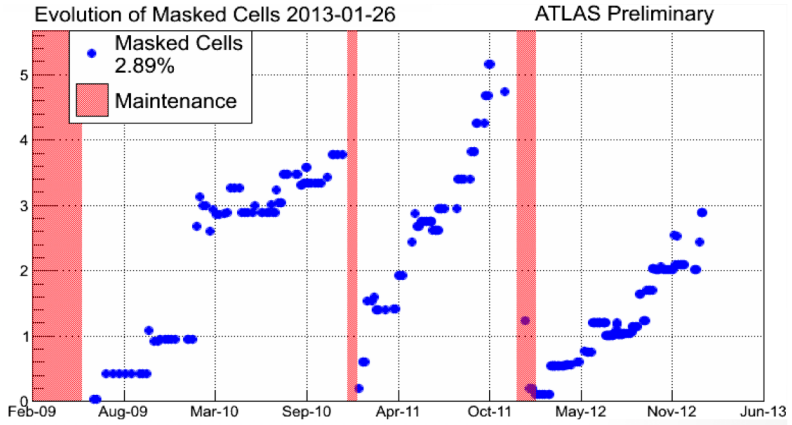
Performance with single muons

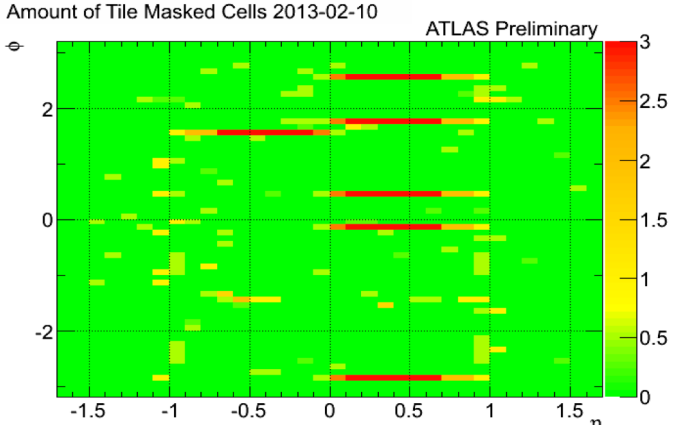


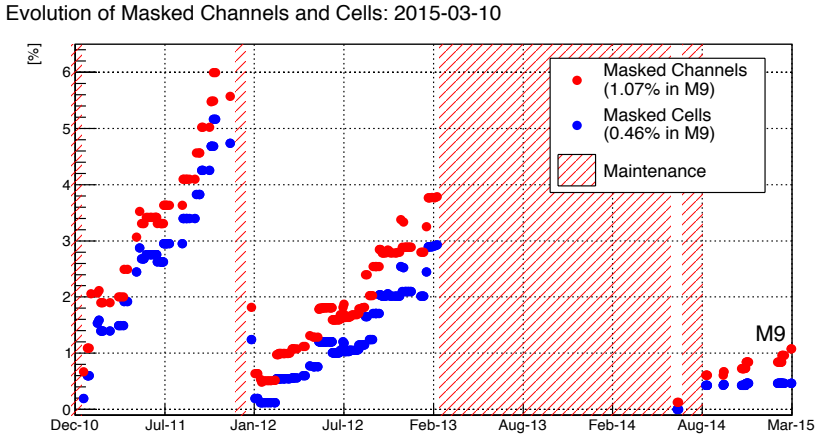


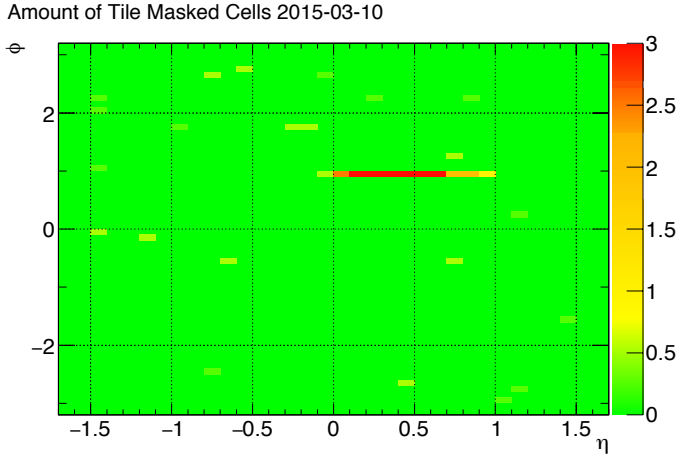
- Ratios of the cosmic rays average momenta p obtained using experimental and simulated data as a function of the pseudo rapidity η (left).
- Distributions of the energy deposited by cosmic rays per unit of path length dE/dl, in the cells LB-D2 obtained using 2008 experimental and simulated data (right).
- The average uncertainty is <1% in LB and <3% in EB.

TileCal : Faulty cells evolution



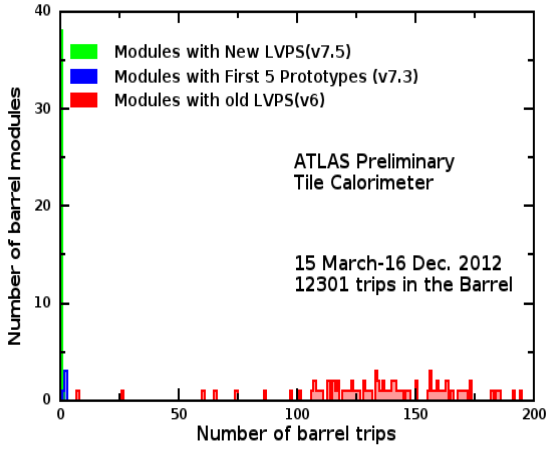


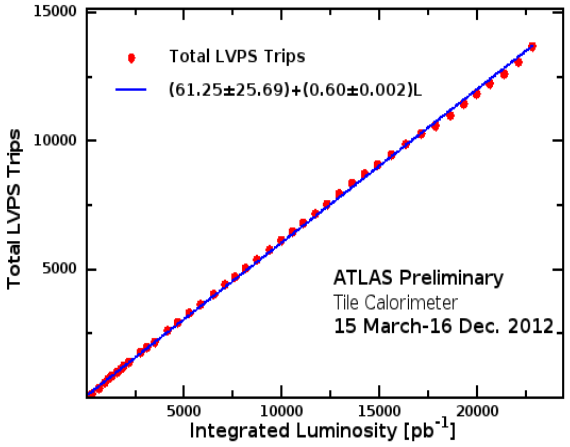


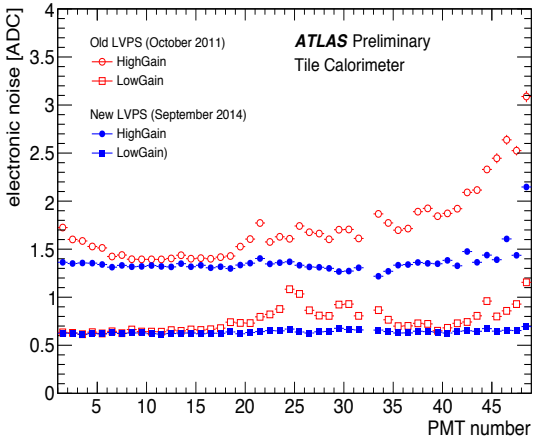


- Percentage of cells and channels masked in 2009-2012 (top) and 2010-2015 (bottom plots)
- The recent detector status corresponding to Milestone week 9 (M9) in March 2015 is noted.
- Most faulty modules due to failures of LVPS - low voltage power supplies.
- Bad LVPS were replaced with the new analogs in maintenance periods, faulty readout cells repaired.
- Significant reduction in the amount of faulty cells: ~2.9% (end of Run1) and ~0.46% (M9).

TileCal during Run1: LVPS trips







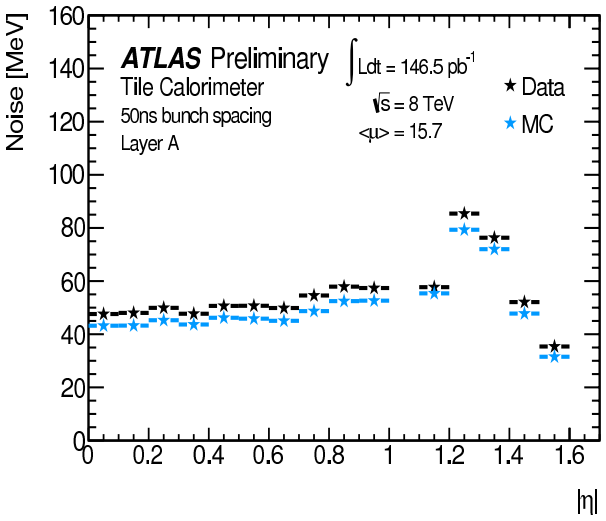
- Problematic Low Voltage Power Supplies (turning modules off):
  1. Number of LB modules that have tripped a specific number of times (left)
  2. The delivered luminosity versus the number of LVPS trips (middle)
  3. Electronic noise (defined as the RMS of the pedestal) in ADC counts as a function of PMT number (right)
- Frequent LVPS trips are correlated with the integrated luminosity.
- Automatic recovery implemented during physics runs
- During maintenance periods in 2011-2012 40 new LVPS installed
- Run1, 2012: ~14K LVPS trips in total, only 1 in the new LVPS version 7.5
- Long Shutdown 1 2013-2015: all LVPS has been replaced by new versions.
- Number of LVPS trips significantly reduced, so less corrupted data
- Improved noise with the newest LVPS: lower electronic noise and more Gaussian

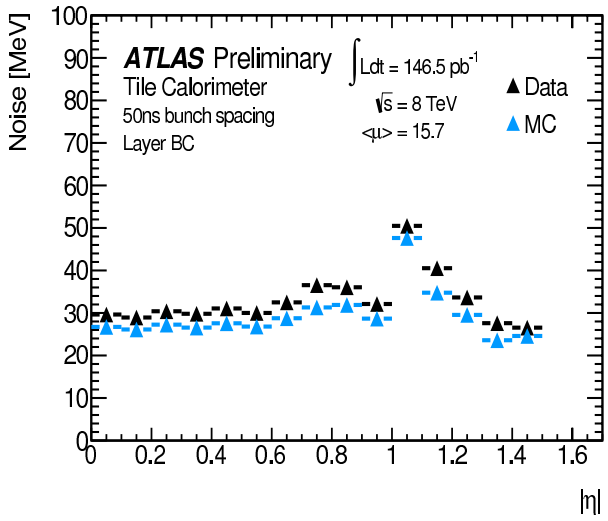
TileCal Run 1 data quality

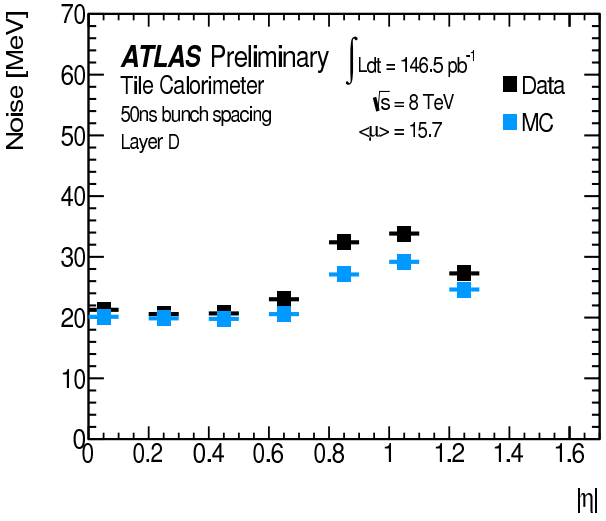
Some efficiency decreasing factors (when 4 or more consecutive modules off) :

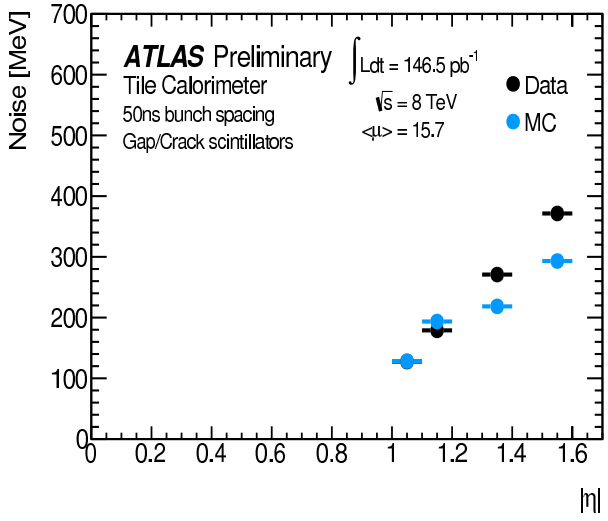
- Read-out link (ROL) not reading data from modules. Improved in June 2012 by implementing the automatic recovery
- Loss from channel times problems after restart. Corrected and recovered in data reprocessing
- Power trips, cuts affecting 200V PS

Performance in presence of pile-up





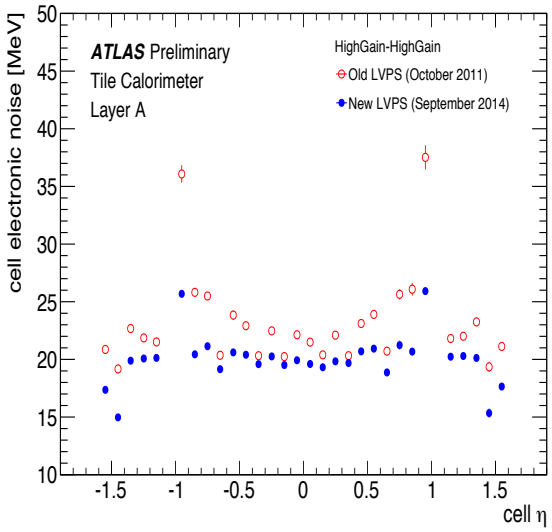


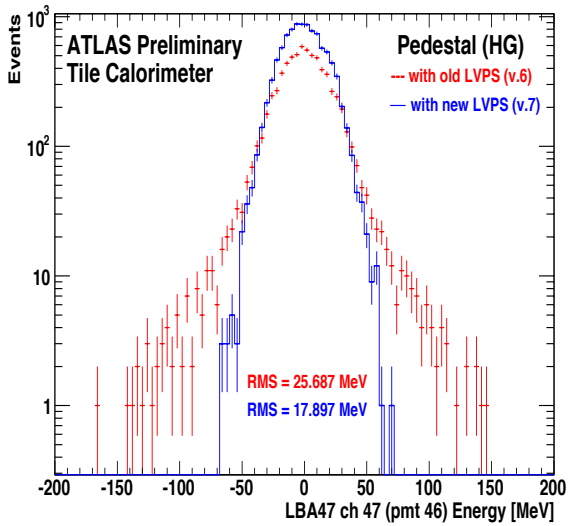


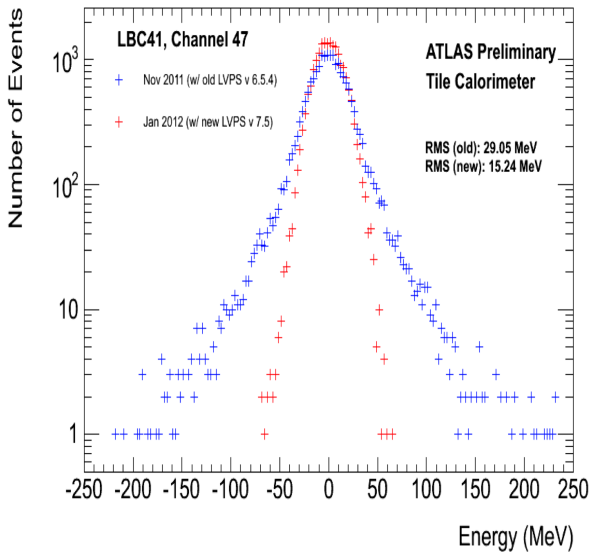
- Noise distribution in different TileCal cells and layers (8 TeV, 50 ns, <μ>=15.7)
- The noise was estimated as the standard deviation of the measured cell energy distribution.
- Total noise as sum of electronic and pile-up (additional *pp* collisions in same or neighboring bunch crossing)
- The highest pile-up observed in the layer A and the special E-cells (Gap/ Crack, bottom right)

Monte-Carlo simulation and Data agree well for the zero bias run 208781 of 2012.

TileCal: electronic noise

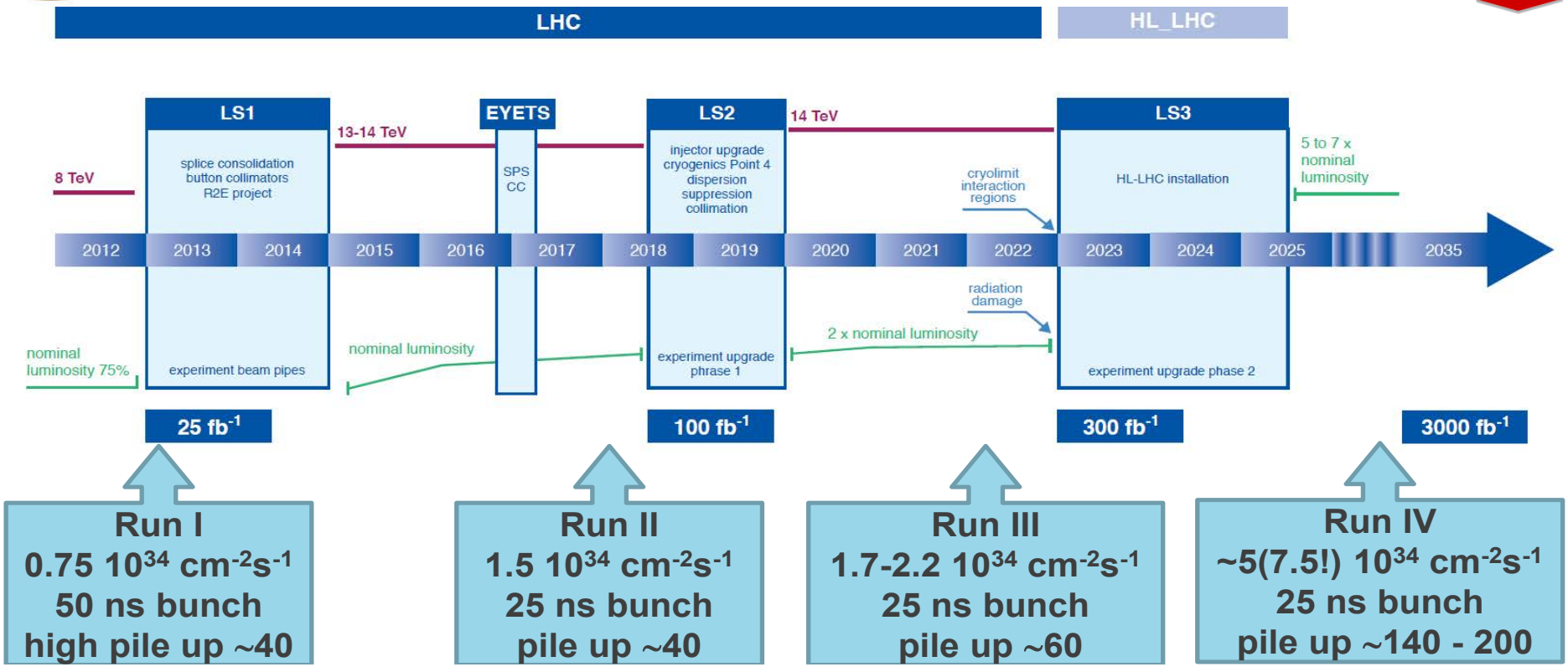






- Evaluation of the cell electronic noise using dedicated pedestal runs (both gains):
  1. Electronic noise (as the RMS of the pedestal) in MeV as a function of cell η (left)
  2. Reconstructed energy from channel 47 of the LBA47 module before and after (blue) the replacement of the LVPS (middle)
  3. A comparison between the reconstructed energy for 100k events in two high statistics pedestal runs, for module LBC41, channel 47 (right)
- Two Gaussian model was used to describe the cell noise in Run1
- Newly installed LVPS show lower noise and a Gaussian-shape distribution
- The RMS of the distribution goes down by almost a factor 2 after changing LVPS
- Total noise (sum of electronic and pileup noise) is well described by the simulation (next slide)

LHC Upgrades: Timeline towards HL-LHC

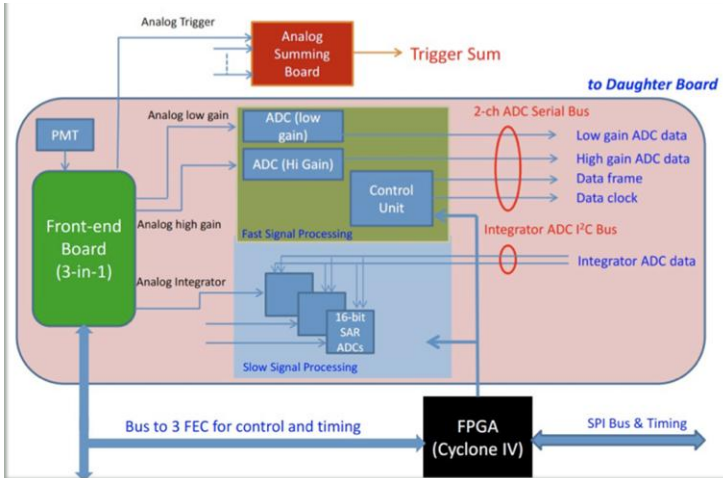


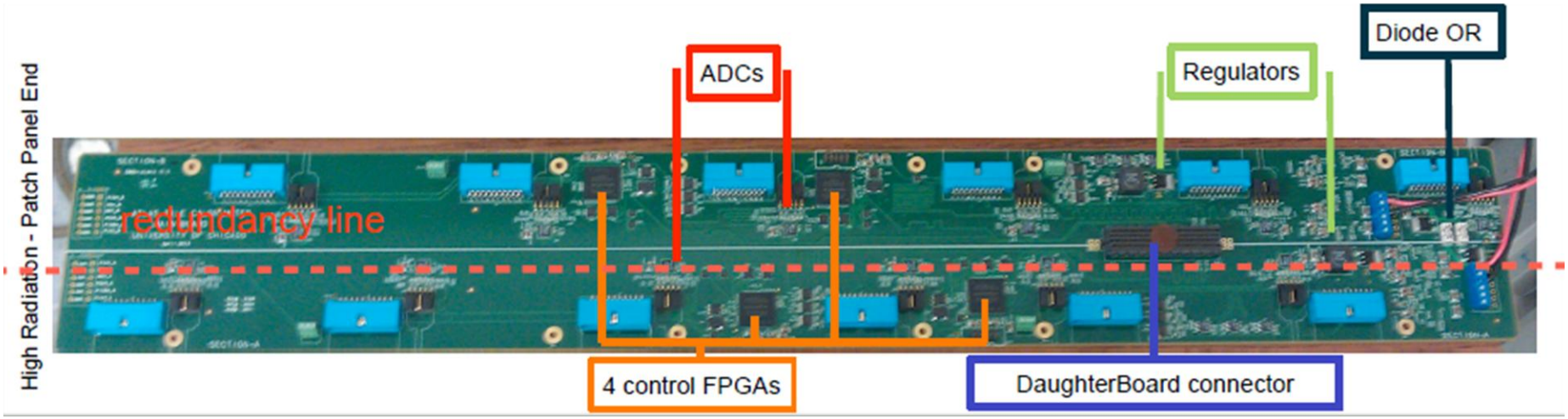
- High-Luminosity LHC upgrade planed for 2023 to extend discovery reach
- Increase luminosity by ten times LHC design value to explore new physics at TeV energies
- For the high luminosity era a major upgrade of the TileCal electronics is planned, with the developments for on- and off-detector systems, together with expected performance characteristics are ongoing

Main board

- MB-1 (Modified 3-in-1)
  - Digital control of 3-in-1 with 4 FPGAs
  - Digitization and transmission to Daughter Board via FMC connector
  - Redundant design (all levels)

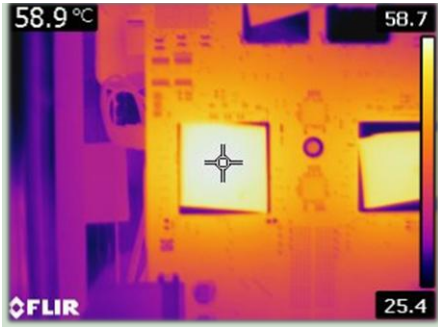
- MB-2 and MB3 (QIE and FATALIC)
  - Minor modification from MB-1
  - No ADCs needed



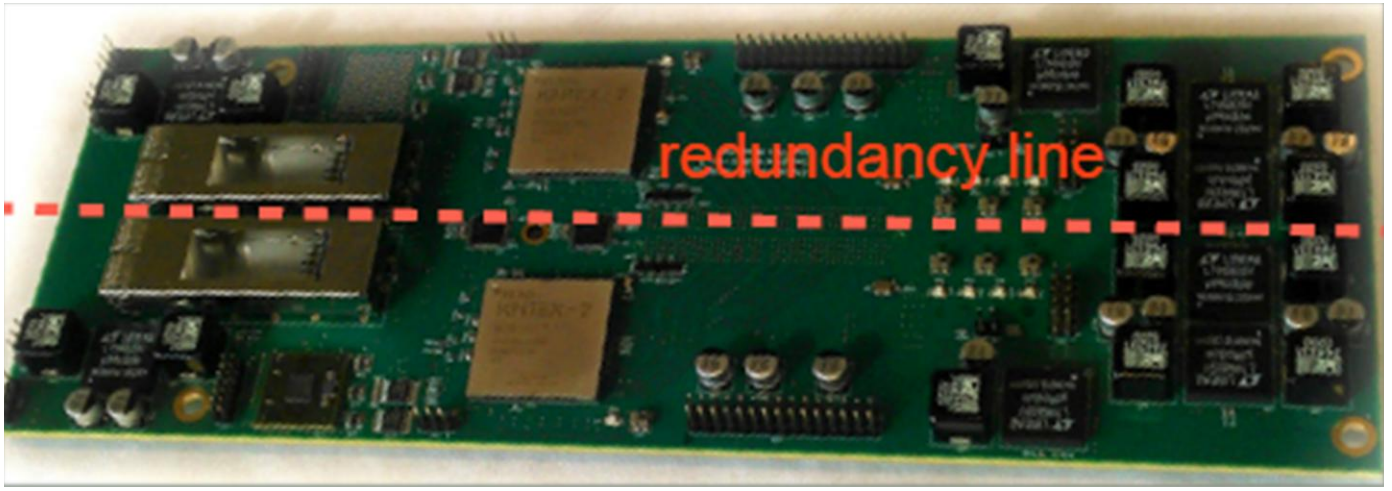


Daughter board

- High speed communication with back-end
  - Formats and transmits read out and Detector Control System (DCS) data
  - Receives configuration and control commands from DCS
  - Configurable via optical link

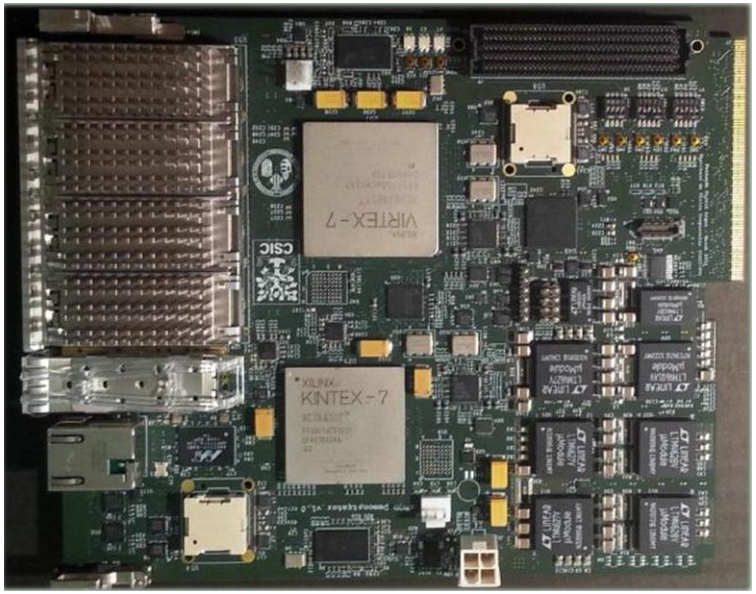


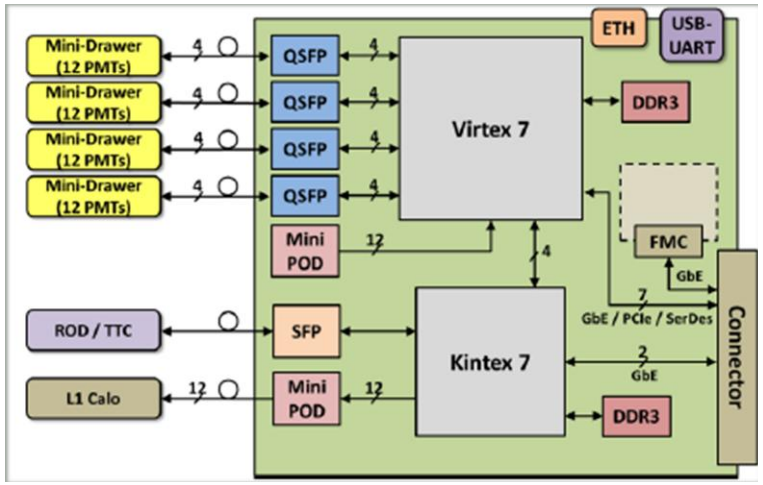
- Complete two fold redundancy
- Temperature tests done



SROD demonstrator

- Main interface for front-end to triggering system
  - Completely digital means better resolution
- Main functionality
  - Main data read out
  - Trigger and Timing Control distribution
  - DCS commands to front-end
- Reads out of 4 mini-drawers
- Designed for new back end infrastructure

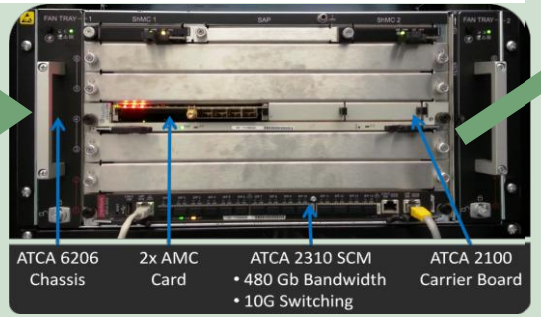




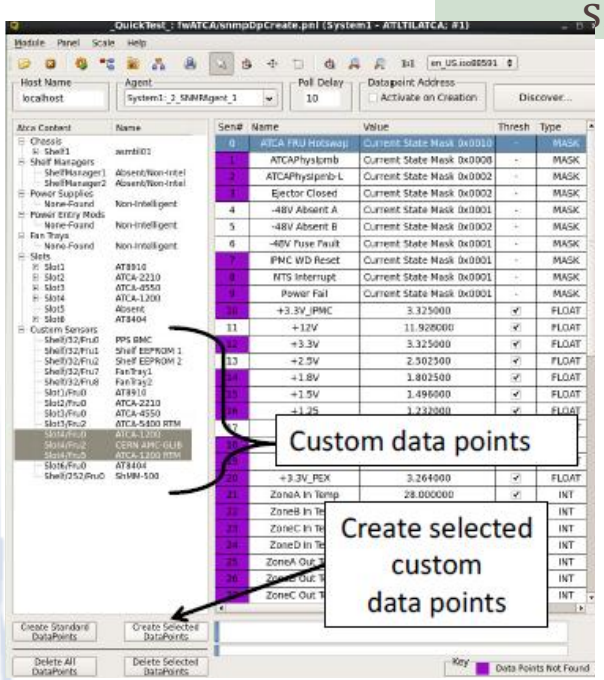
Back-end infrastructure

The ATCAs will house the back-end electronics

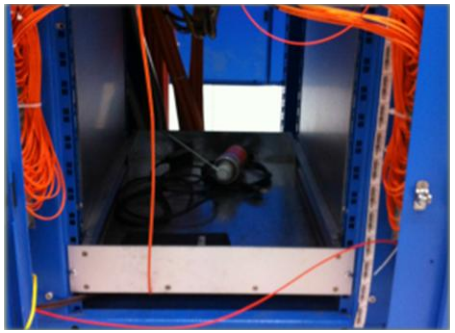
sROD



ATCA Chassis



- Integration of ATCAs into the ATLAS DCS with a new framework tool
- Control and monitor chassis and all components through Simple Network Management protocol



ATCA location for off detector electronics in the ATLAS cavern