A Large Ion Collider Experiment

ALICE Upgrade Progress

W. Riegler, LHCC, Sept. 23rd, 2014

ALICE Upgrade Strategy

High precision measurements of rare probes at low $p_{T,}$ which cannot be selected with a trigger, require a large sample of events recorded on tape

Target: Recorded Pb-Pb recorded luminosity $\geq 10\ nb^{-1}$ ➡ 8×10^{10} events

Gain a factor 100 in statistics over the Run1+Run2 programme and significant improvement of vertexing and tracking capabilities

I. Upgrade the ALICE readout systems and online systems to

- **read out all Pb-Pb interactions at a maximum rate of 50kHz (i.e. L = $6 \times 10^{27}\ cm^{-1}s^{-1}$), with a minimum bias trigger**
- **Perform online data reduction based on reconstruction of clusters and tracks (tracking used only to filter out clusters not associated to reconstructed tracks)**

II. Improve vertexing and tracking at low p_T ➔ New ITS

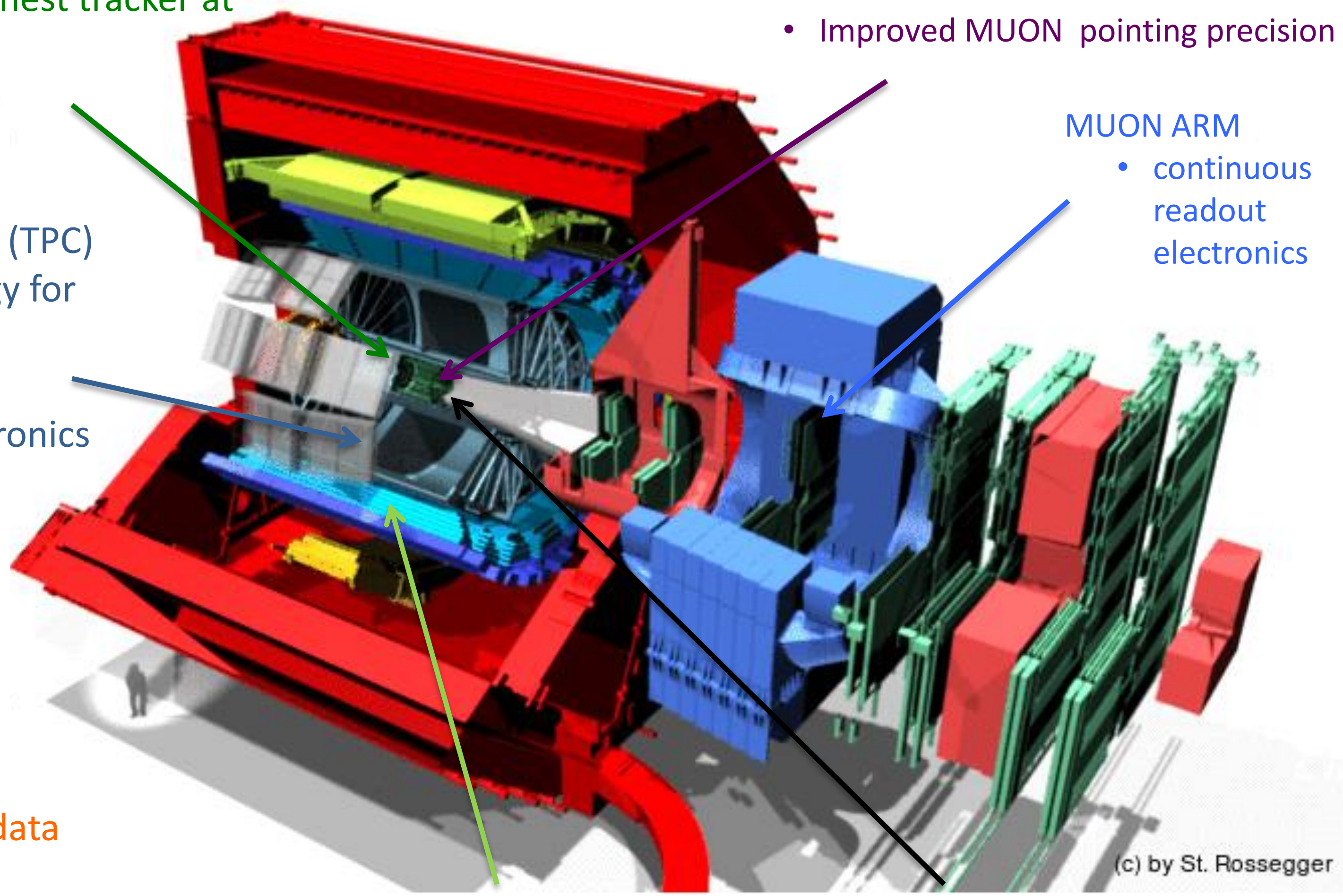
ALICE Upgrade

New Inner Tracking System (ITS)
- improved pointing precision
- less material -> thinnest tracker at the LHC

Muon Forward Tracker (MFT)
- new Si tracker
- Improved MUON pointing precision

MUON ARM
- continuous readout electronics

Time Projection Chamber (TPC)
- new GEM technology for readout chambers
- continuous readout
- faster readout electronics



Data Acquisition (DAQ)/
High Level Trigger (HLT)
- new architecture
- on line tracking & data compression
- 50kHz Pbb event rate

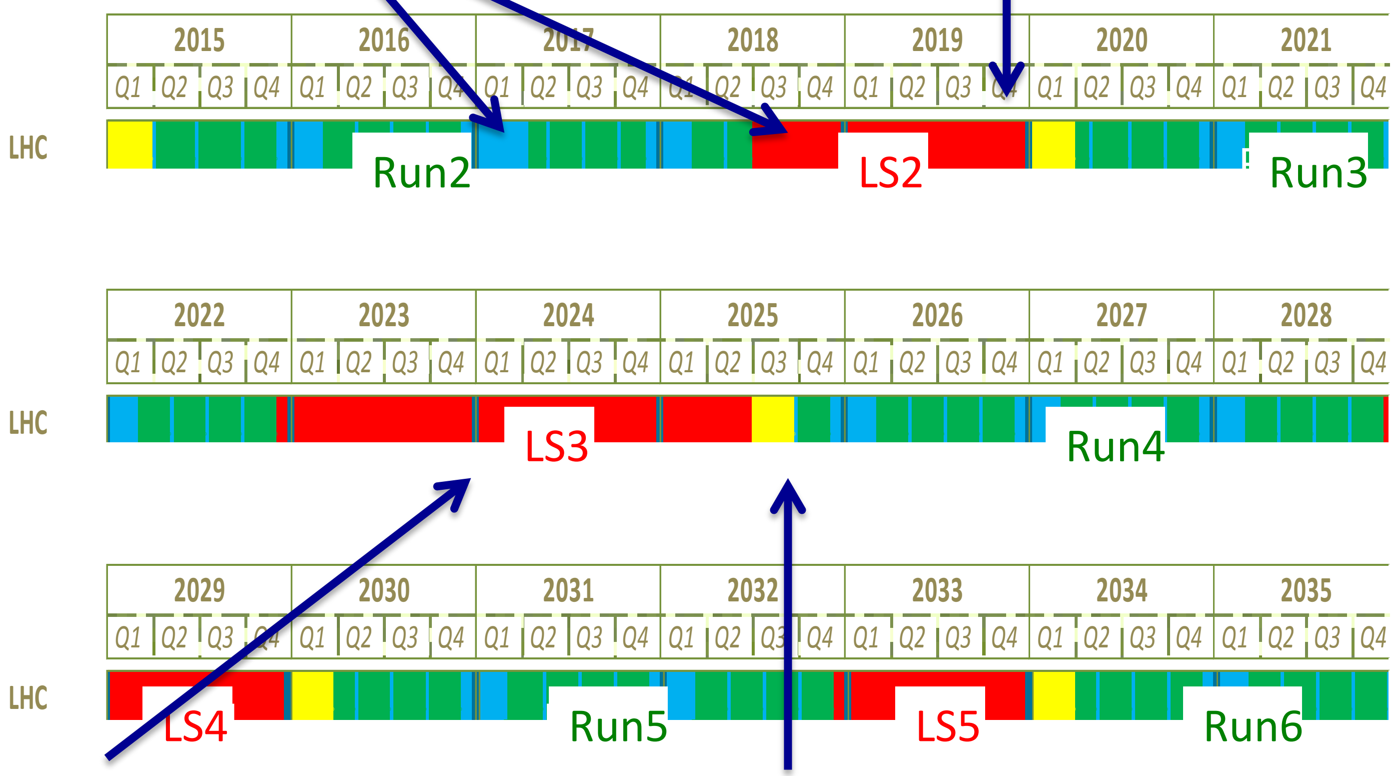
TOF, TRD
- Faster readout

New Trigger Detectors (FIT)

Long Term Schedule

PHASE I Upgrade
ALICE, LHCb major upgrade
ATLAS, CMS ‚minor‘ upgrade

Heavy Ion Luminosity from 10^{27} to 7×10^{27}



PHASE II Upgrade
ATLAS, CMS major upgrade

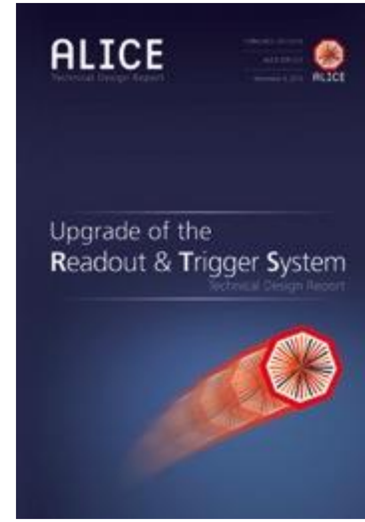
HL-LHC, pp luminosity from 10^{34} (peak) to 5×10^{34} (levelled)

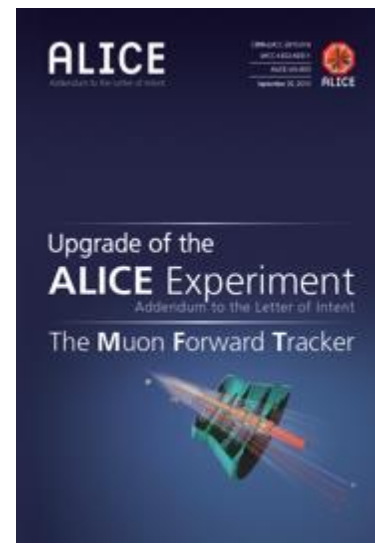
ALICE will operate beyond LS3 in the HL-LHC era

ALICE LS2 Scope

The approved LS2 upgrade is detailed in 5 Technical Design Reports

- **ITS**
- **Readout and Trigger System**
- **TPC (under review)**
- **MFT (Nov. 2014)**
- **Online Offline System (Jun. 2015)**





ALICE Upgrade

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- **improved pointing precision**
- **less material**

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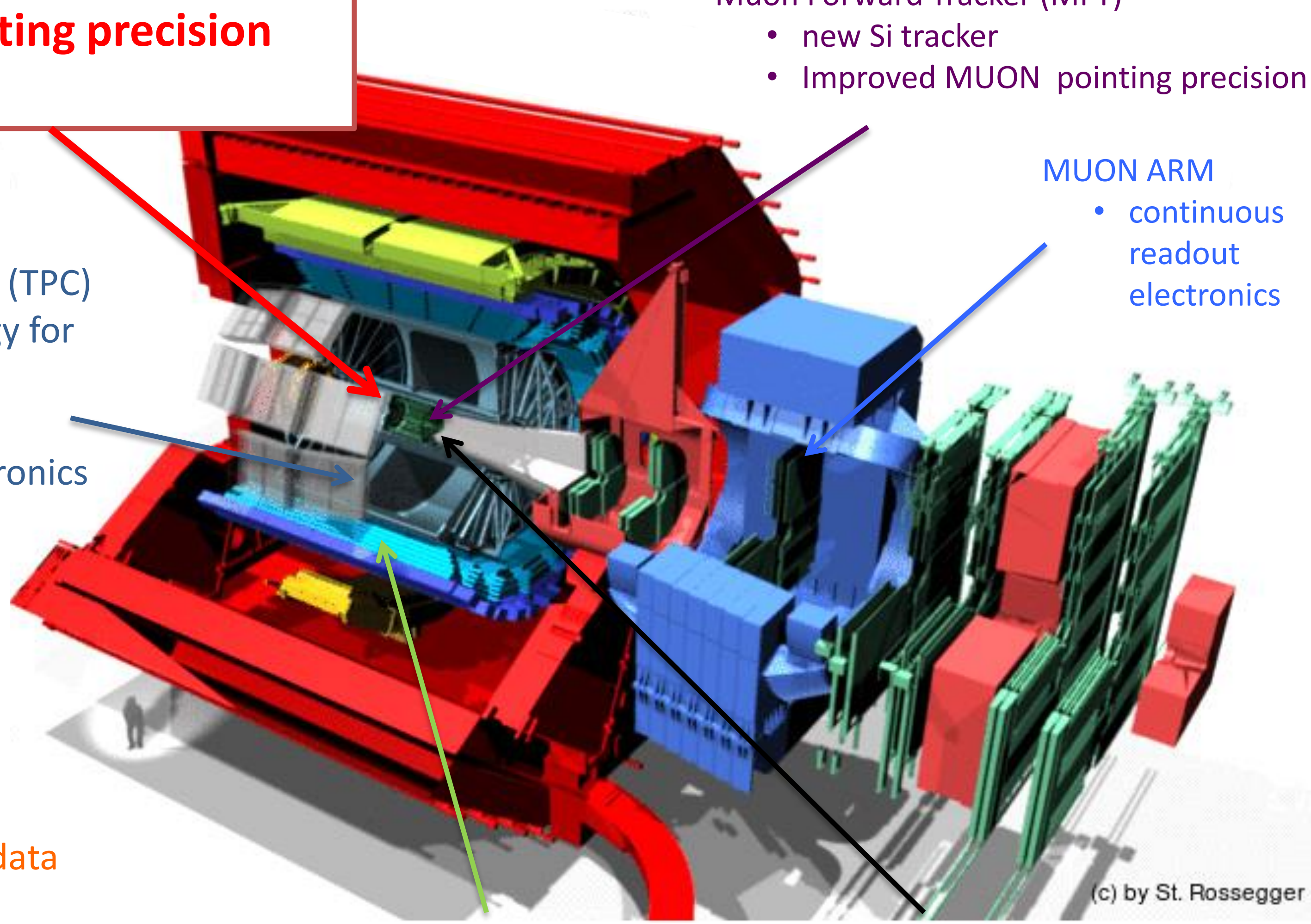

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Status of ITS CMOS Pixel Sensor

External layout

- dimensions and position of IO-pads defined
- Interface communication protocol defined

Internal Architecture (two options)

- ALPIDE
  - Specs comply with Inner Barrel and Outer Barrel
  - Pixel Size: 28μm x 28μm   Integration time: ~4μs
  - Power density: 40 mW/cm^2
- MISTRAL (more conservative approach)
  - Specs optimized for OB (L3-L6) but does not comply with Inner Barrel
  - Pixel Size: 36μm x 62μm   Integration time: ~20 μs
  - Power density: ~ 100 mW/cm^2

- Full scale prototype of ALPIDE and MISTRAL are currently being characterized in the laboratory and test beam
- Preliminary results (see following slides) very encouraging

pALPIDEfs – A full-scale prototype of ALPIDE

- Dimensions: 30mm x 15 mm
- About 0.5 M pixels 28μm x 28μm
- 40 nW front-end (4.7mW / cm^2)
- Allows reverse substrates bias to increases depletion volume
- 4 sectors with different pixels

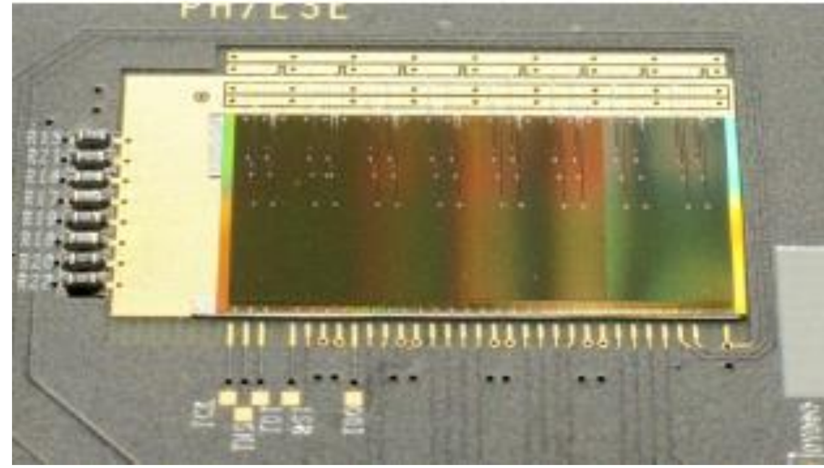
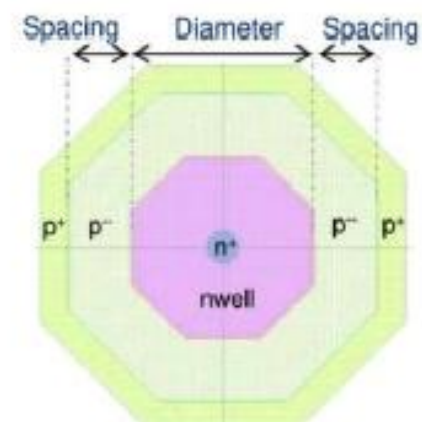


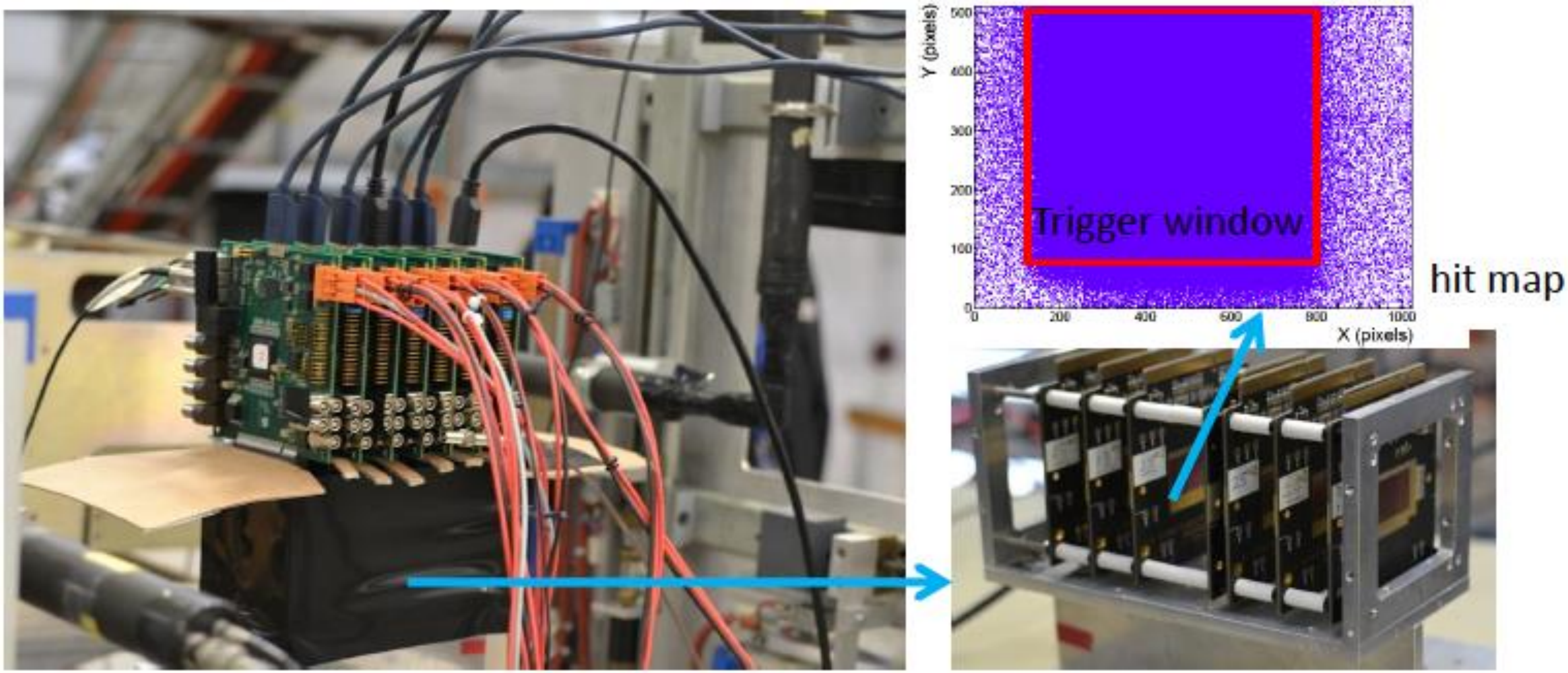
Figure: picture of pALPIDEfs

Sector	nwell diameter	Spacing	pwell opening	Reset
0	2 μm	1 μm	4 μm	PMOS
1	2 μm	2 μm	6 μm	PMOS
2	2 μm	2 μm	6 μm	Diode
3	2 μm	4 μm	10 μm	PMOS



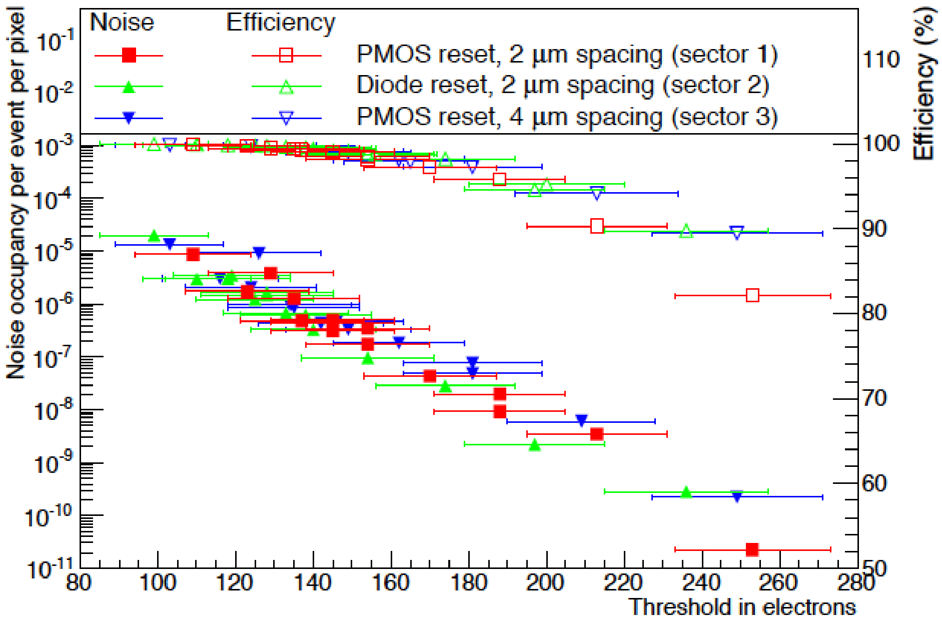
- In-matrix sparsification using priority-encoder logic
- No high-speed output link in this version

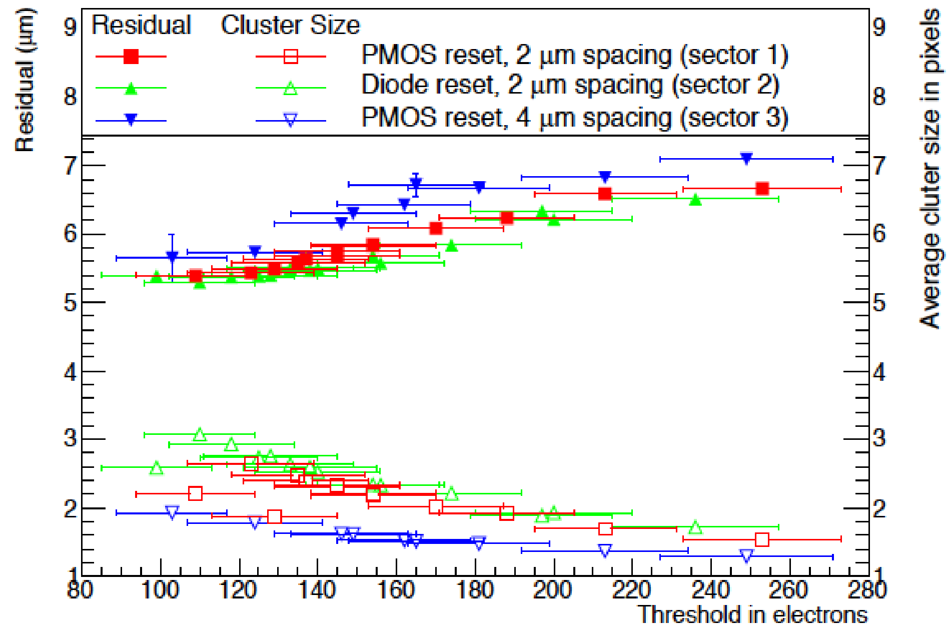
pALPIDEfs – measurements at PS test beam

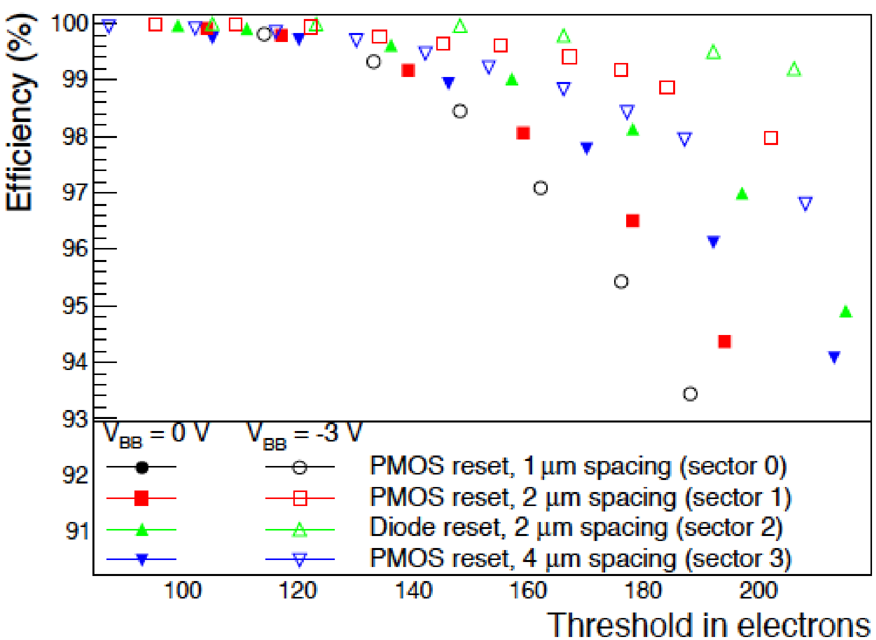


- Four weeks of test beam at the PS (5 – 7 GeV pions)
- Telescope based on a stack-up of 6 or 7 layers of pALPIDEfs
- Tested both thinned (50μm) and thick (450μm) chips
- 0V and 3V reverse substrate bias (measurem. at -6 V and after irradiation ongoing)
- Comprehensive characterization will continue at PS and in October at SPS

pALPIDEfs – measurements at PS test beam







- 99% efficiency at fake hit rate of 10^{-5} achievable (only 20 pixels masked) at 0V
- Reverse substrate bias (V_{BB}) provides additional margin
- Telescope based on a Stack-up of 6 or 7 layers of pALPIDEfs
- Spatial resolution (including tracking error of ~3μm): 5.5 μm

FSBB-M0 – Full Scale Building Block of MISTRAL

FSBB-M0 (Full Scale Building Block Mistral 0)

- About 1/3 of a complete sensor (approx. 9mm x 17mm)
- 416 x 416 pixels of 22μm x 33μm (final chip 36μm x 62μm)
- 40μs integration time
- Full chain working (front-end, discr., zero suppression)
- 25 sensors characterized showing similar noise perfor.
- Test beam measurements at SPS in October

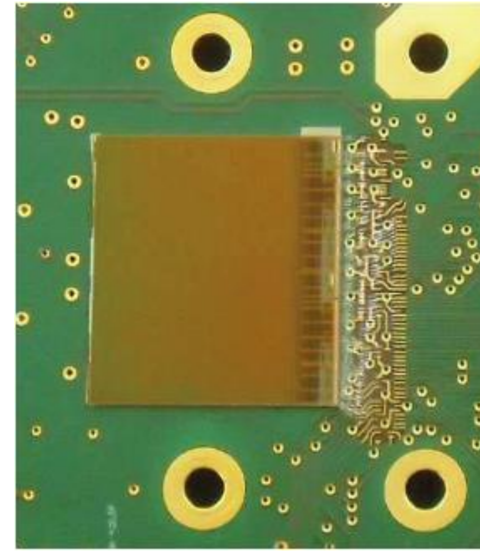
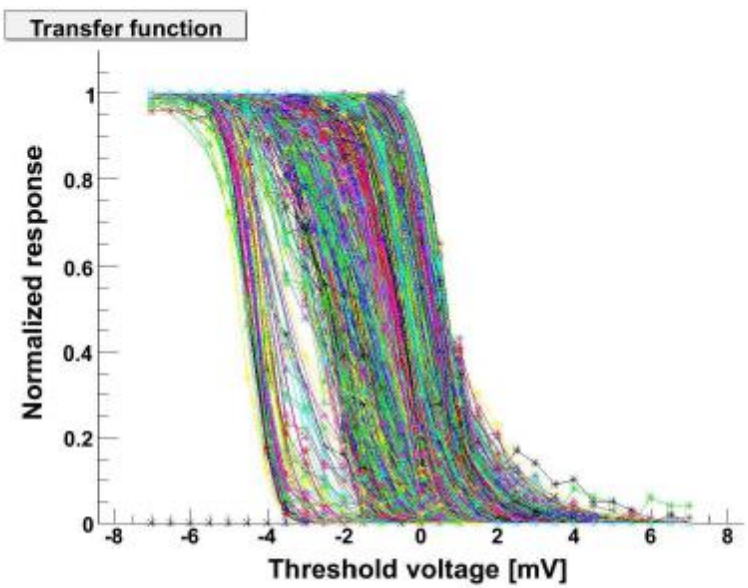
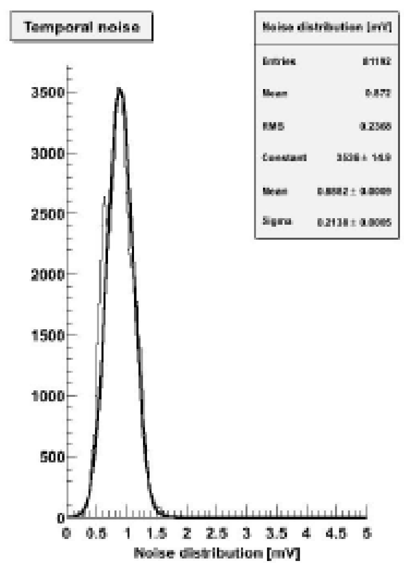


Figure: Two FSBB M0

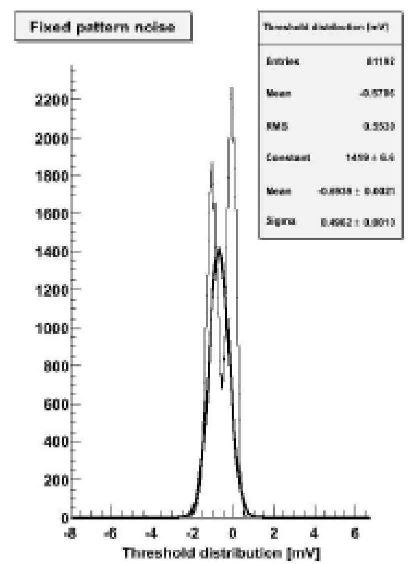


TN = 0.87mV



Temporal Noise

FPN = 0.55mV



Fixed Pattern Noise

ALICE Upgrade

Muon Forward Tracker (MFT)
- **new Si tracker**
- **Improved MUON pointing precision**

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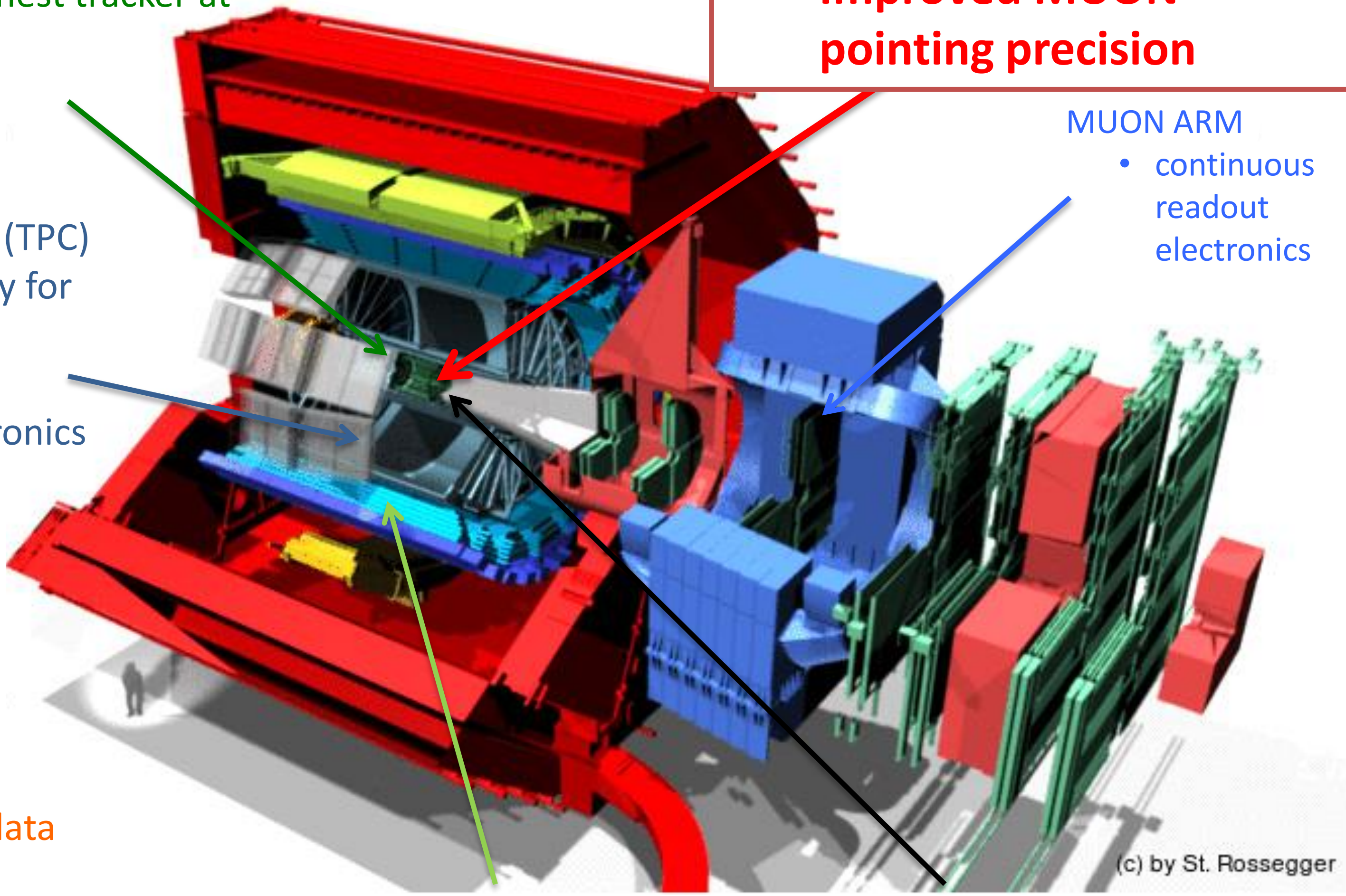

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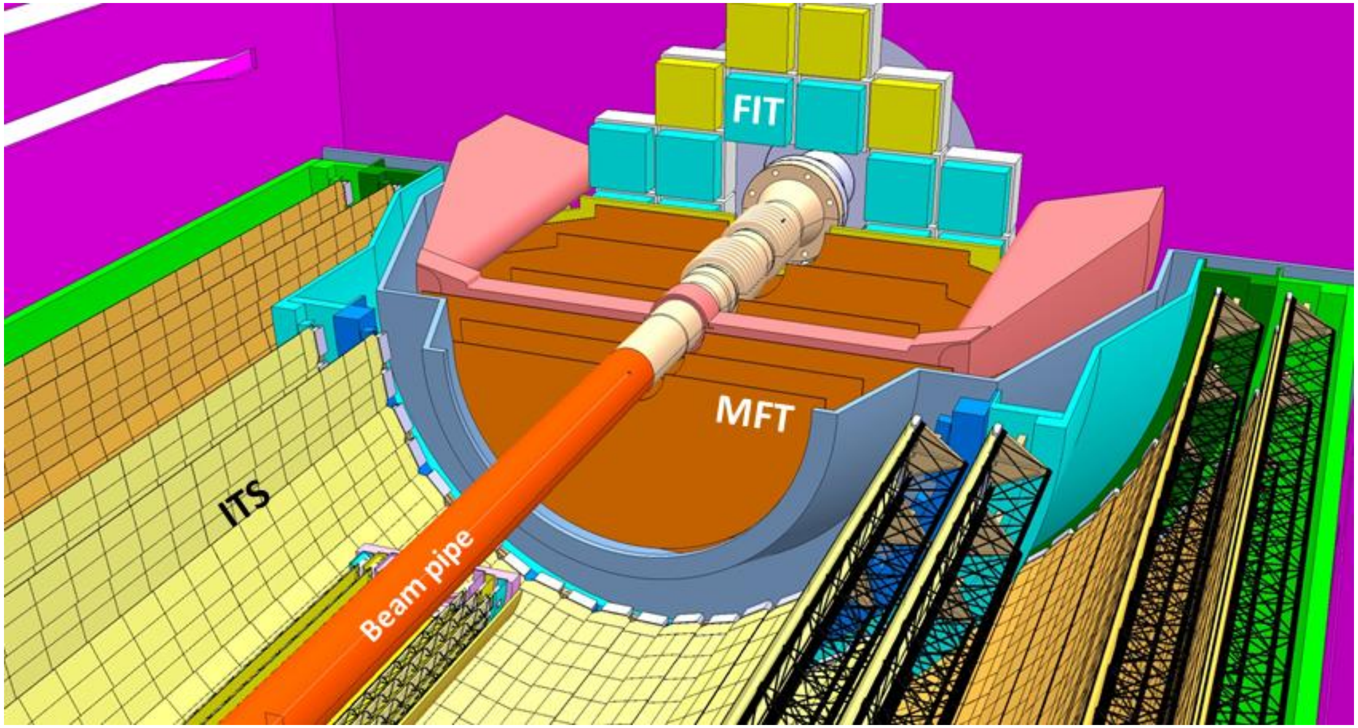
New Trigger Detectors (FIT)

Muon Forward Tracker (MFT)

The primary goal of the Muon Forward Tracker (MFT) is to measure muon tracks in the ALICE muon spectrometer acceptance with high precision vertexing in the interaction point area.

The MFT is a silicon pixel tracker complementing the acceptance of the ALICE upgraded Internal tracking system (ITS) and covering most of the acceptance of the muon spectrometer 2.5<η<3.6.

The MFT detector is placed inside the ITS outer barrel, between the ITS inner barrel and the frontal absorber and surrounding the ALICE vacuum beam-pipe.



Muon Forward Tracker (MFT)

Common Silicon Sensor with ITS (15 mm x 30 mm)

Polyimide Flex Printed Circuit with Al strips.

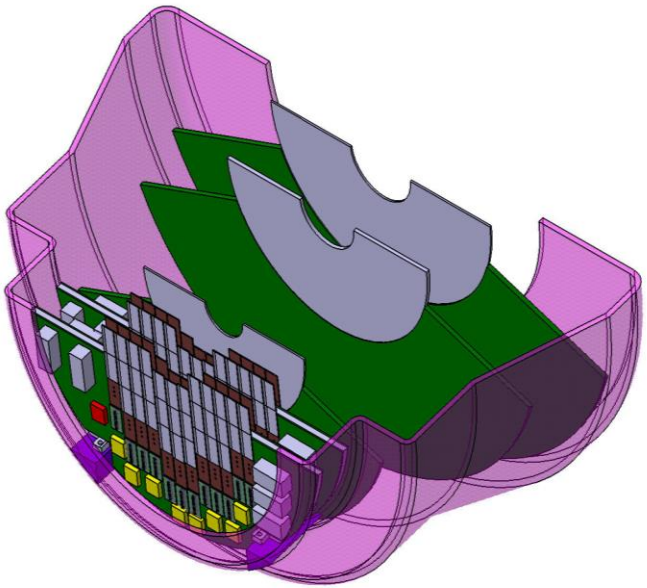
HIC consisting in 1-5 sensors bonded to the sensor via the Laser technology developed by the ITS group.

Each disk: Two detection planes, a disk spacer, a disk support and 2 PCB.

Each detection plane consisting ladders (MFT HIC glue two a stiffener).

Two option for sensor cooling begin considered:

- Air cooling
- Water cooling with polyimide cooling water pipes embedded in the disk spacer.



For a sensor consumption of 50 (30) mW/cm^2 the total power dissipated by the MFT sensors is 290 (180) W.

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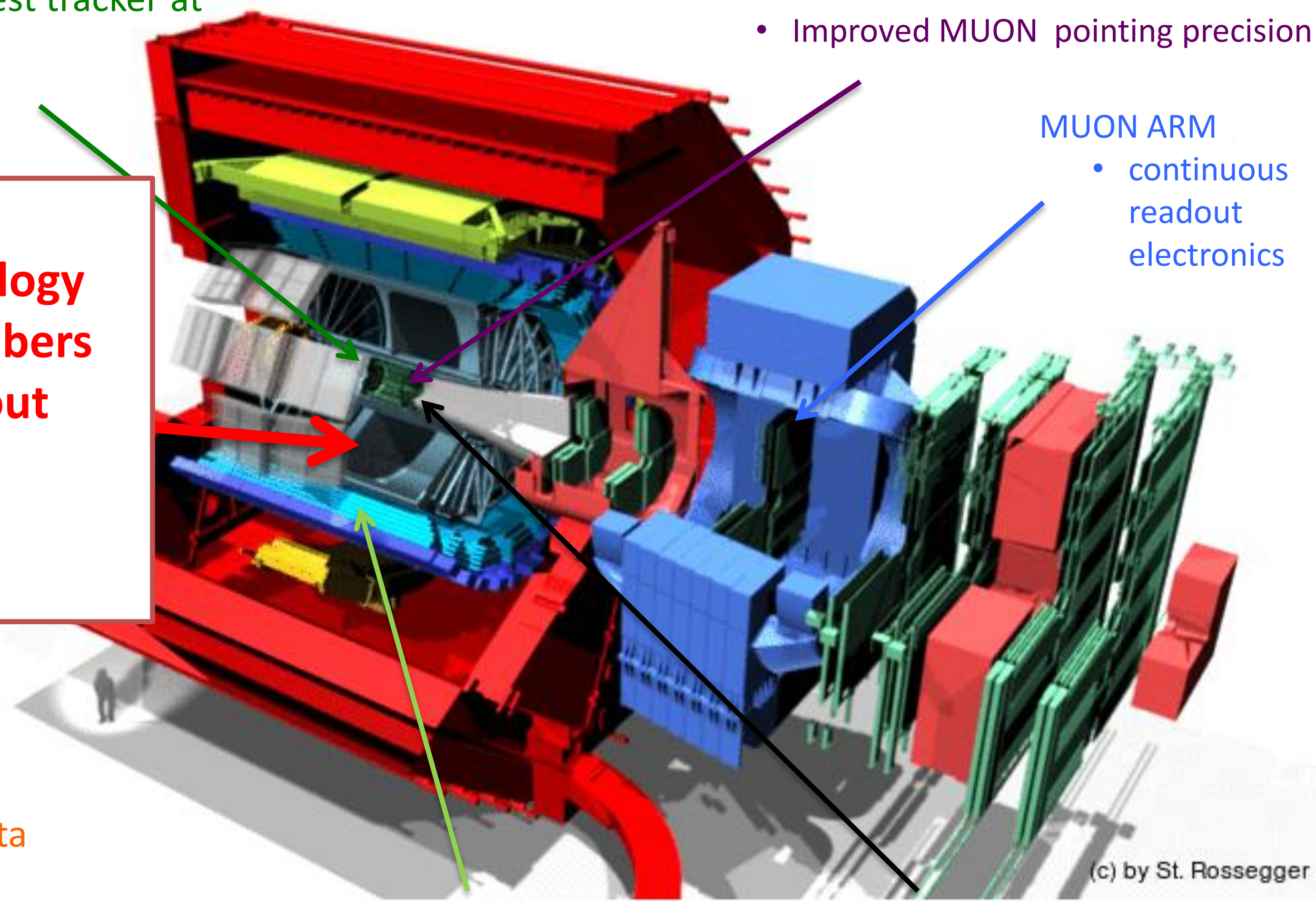

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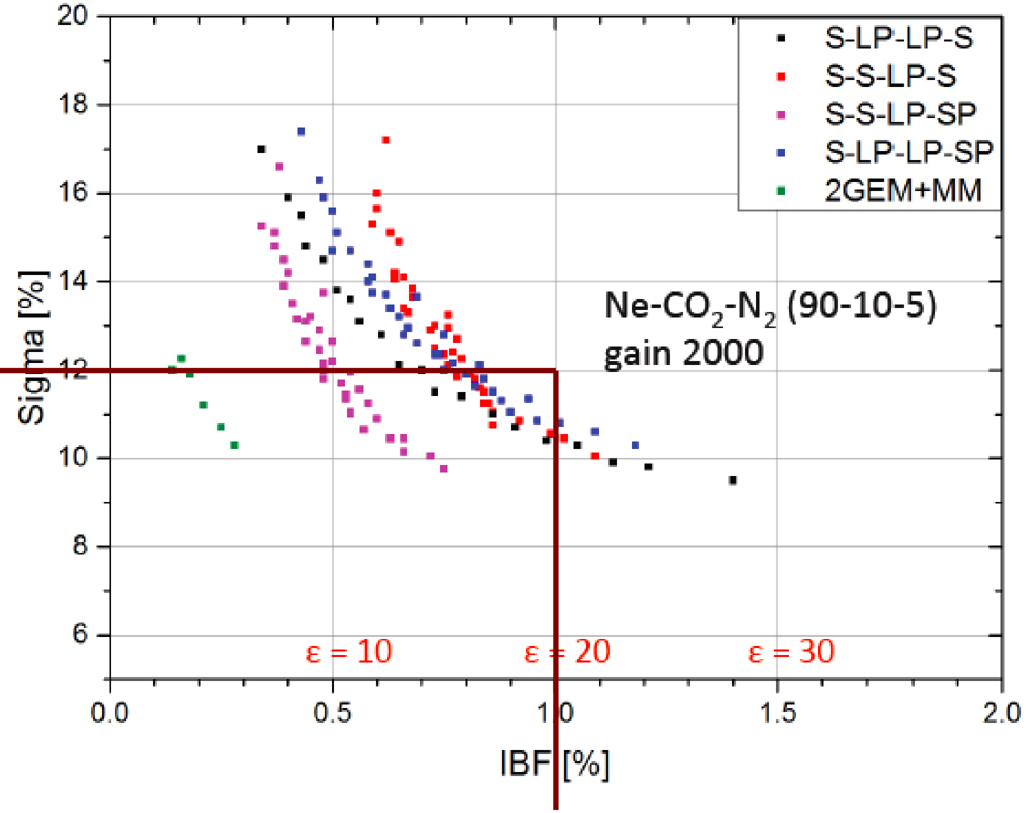
TPC Upgrade

ALICE

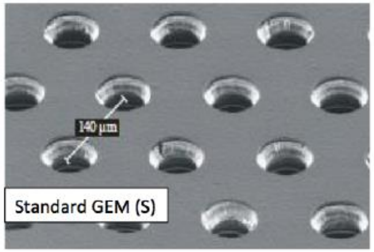
4GEM small prototypes

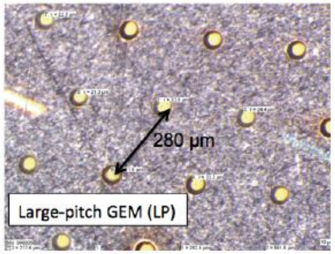
present status

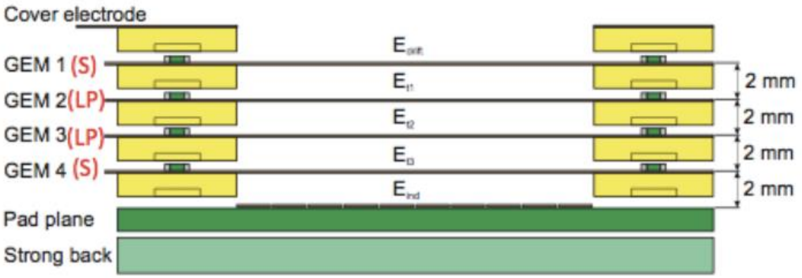


GEM holes:
Diam: 70um

Distance:
SP: 90um
S: 140um
LP: 280um

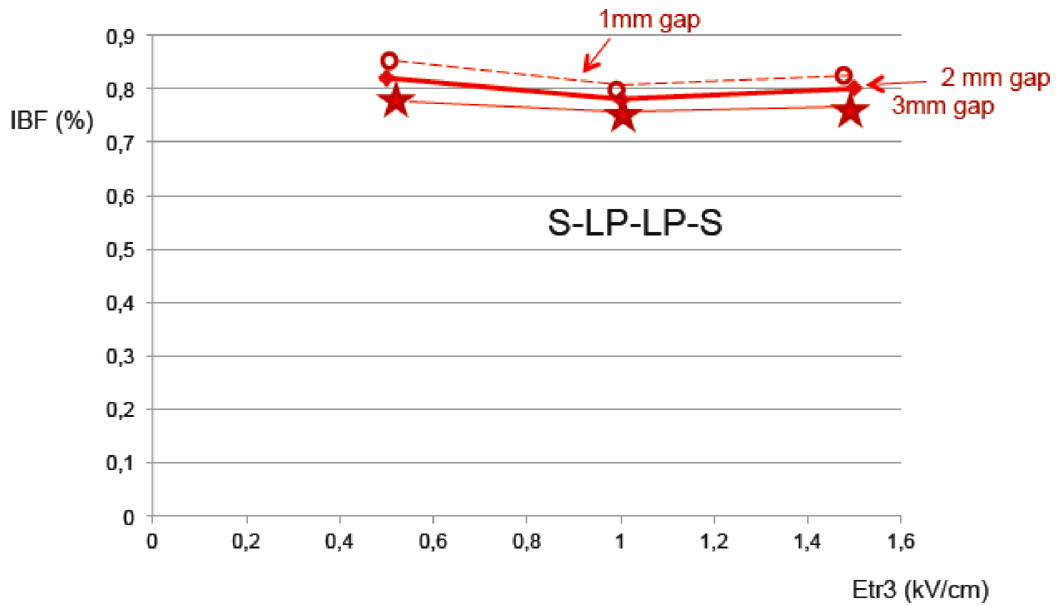




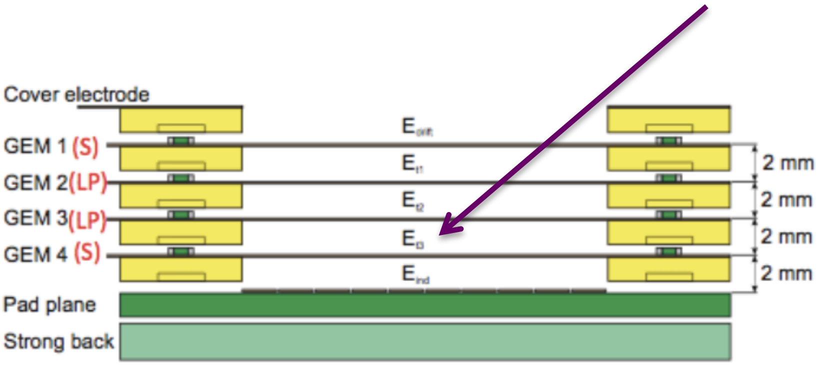


TPC Upgrade

4GEM small prototypes – ET3 gap dependence



no dependence on the ET3 gap



TPC Upgrade

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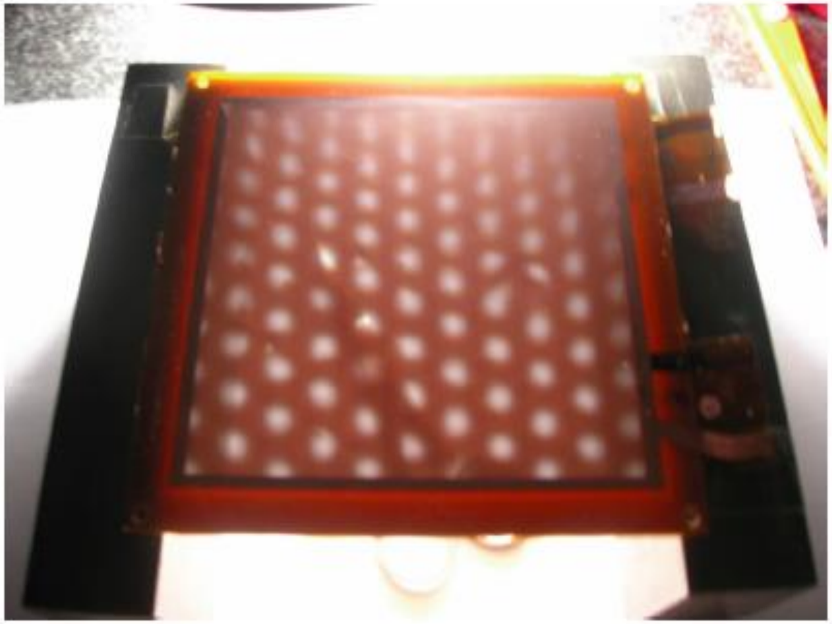
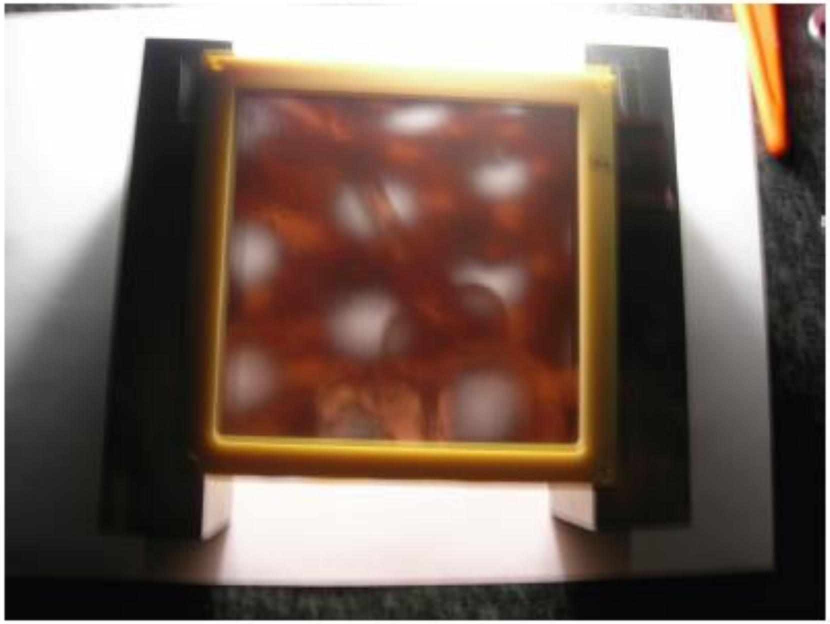
4GEM small prototypes – GEM alignemnt

- Optical transparency exhibits interference pattern in parallel GEM orientation





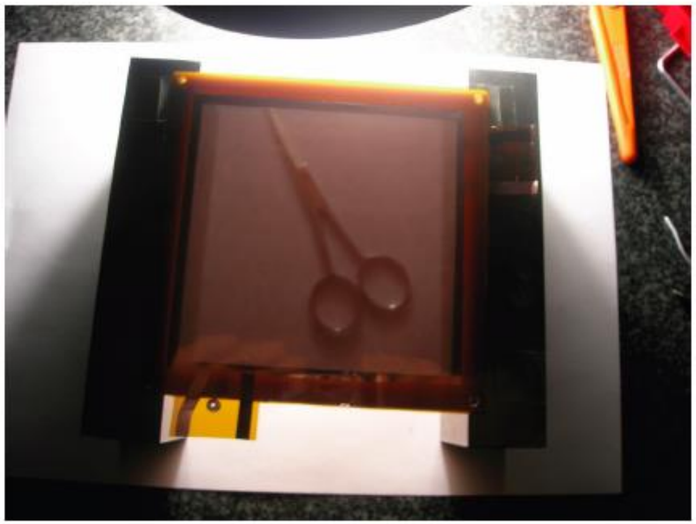
- two foils put on top here
- may lead to non-uniformities of GEM characteristics

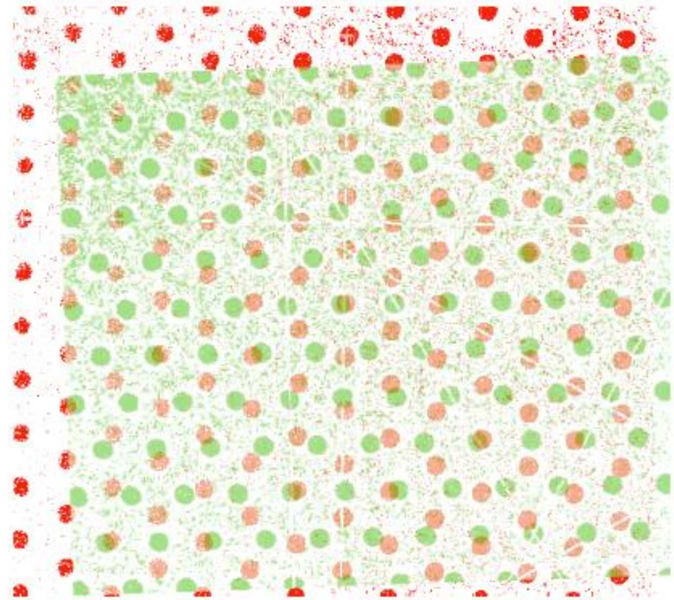
TPC Upgrade

A Large Ion Collider Experiment

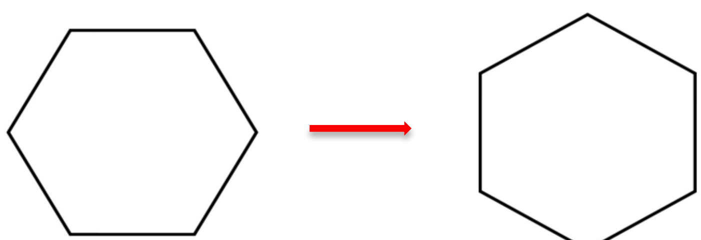
4GEM small prototypes – GEM alignemnt

- 90° orientation leads to random alignment





- Random alignment prefered in terms of uniform detector response
- quantitative studies ongoing

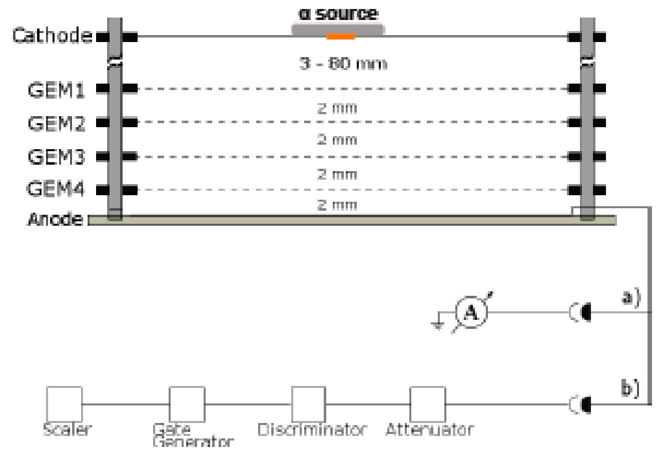


A Large Ion Collider Experiment

TPC Upgrade

ALICE

Discharge studies – update



Discharge probability is comparable (or possibly better) than the one for ‚standard' GEM settings.

Tests with MIPs in Nov./Dec. testbeam

SOURCE	S-LP-LP-S				
	IBF = 0.6 % σ_E/E = 12 % G = 1000	IBF = 0.6 % σ_E/E = 12 % G = 2000	IBF =0.6% σ_E/E=12% G =3300	IBF =0.6 % σ_E/E =12 % G =4000	IBF =0.6 % σ_E/E =12 % G =5000
^{241}Am *rate = 11 kHz* *drift gap = 80 mm*	$< 1.1\times10^{-8}$	$< 1.5\times10^{-10}$	$< 7.1\times10^{-10}$		
^{239}Pu + ^{241}Am + ^{244}Cm *rate = 600 Hz* *drift gap = 37 mm*		$< 3.1\times10^{-9}$		$\approx 5\times10^{-9}$	$(1.8 \pm 1.1)\times10^{-8}$

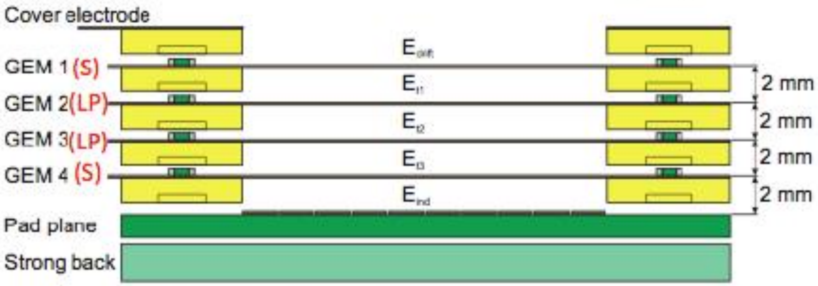
TPC Upgrade

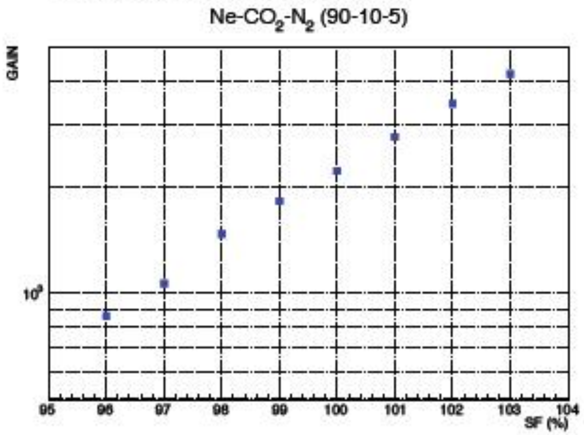
A Large Ion Collider Experiment

ALICE

4GEM IROC prototype

- 4 single-mask GEMs: S-LP-LP-S configuration
- Prototype ready in August 2014
- Commissioning with ^{55}Fe source
  - Baseline HV settings
  - Gain curve
  - Energy resolution ($\sigma_E/E \approx 12\%$ at G=2000 w/o corrections)
- To do:
  - Gain scan with multi-channel readout
  - Stability studies with ^{220}Rn source
  - Install FEE for test beam
  - Readout commissioning





Testbeam: PS Nov. 2014, SPS Dec. 2014

TPC Upgrade

A Large Ion Collider Experiment

ALICE

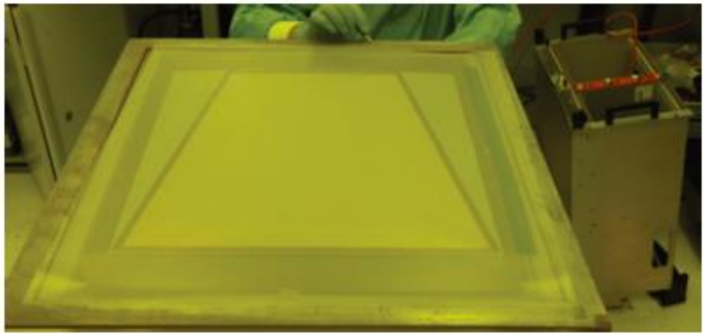
2GEM+MM IROC prototype

detector concept:

- pre-stretched Micromegas (400 LPI) with pillars and a spacer frame (128 μm) glued on top of a spare IROC alubody+padplane (same as for 4GEM IROC)
- 2 standard (pitch = 140 μm) IROC GEMs mounted (screwed/glued) on top

planned for the test-beam campaign for a direct comparison with 4GEM IROC

status:



alu-body + pad plane:

- wires and frames removed, feed-throughs drilled
- pad plane polished and cleaned

GEMs

- framed

mesh gluing

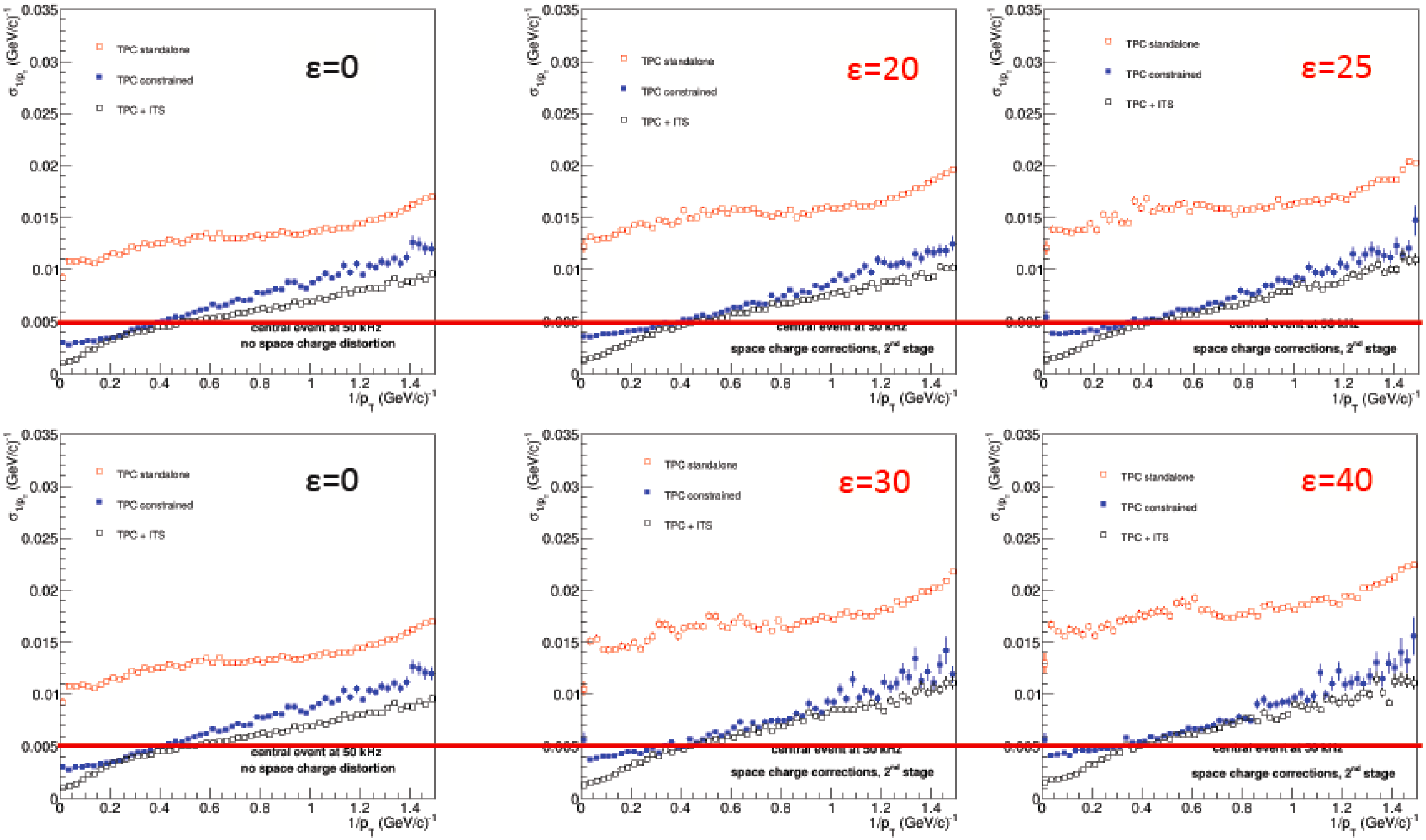
- 1st attempt in August: short developed after gluing → grounding area surrounding the pad plane has been removed
- 2nd attempt in September: second mesh has been produced and is now being installed in CERN lab

Testbeam: PS Nov. 2014, SPS Dec. 2014

A Large Ion Collider Experiment

TPC Momentum Resolution

Simulation



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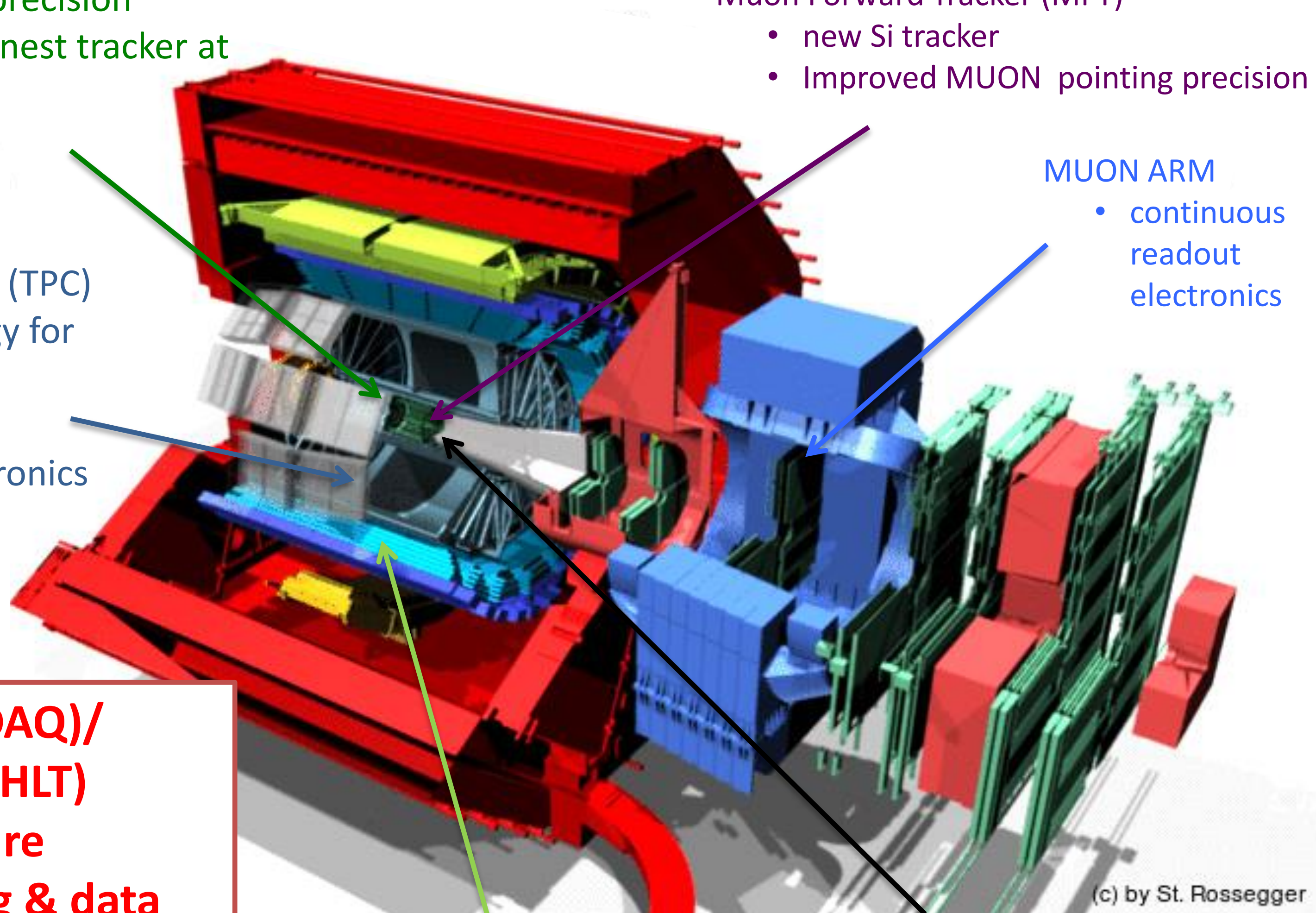

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TDR Schedule

- November ’13: Table of Contents, Editorial Committee (EC) membership
- December ‘13: List of contributions from the CWGs
- Feb ‘14 List of all plots, tables and text skeleton
- Apr ’14: Draft 0 of the text for review inside CWGs
- May ’14: Draft 1 for review inside EC
- 4th July ‘14: Draft 2 for review inside EC
- 1st Sep ‘14: Draft 3 for review inside EC (week 22 September)
- 24th -26th Sep ‘14: EC review
- Jan ‘14: Draft 4 for review inside O^2
- Feb ‘14: ALICE internal review
- Mar’ 15: early: Final version for editing
  mid : Circulate TDR to the ALICE collaboration
- Apr ’15: end: Submission TDR to LHCC 29 (1 month before)
- Jun ’15 : LHCC meeting

Key technical milestones

- Activities in progress
  - Overall architecture and design
  - Computing platform benchmarks
  - Computing system simulation
  - Software framework prototype (Alfa testbed)
    - Refines dataflow functionalities
    - Data distribution and load balancing studies
    - Implement the first version of Run3/4 raw data format and use it for the simulated data
    - Test existing HLT algorithms
    - Used to compare design options and technical solutions
  - TDR writing
- TBD
  - Decide on the options to be selected and those which will be left open in the TDR

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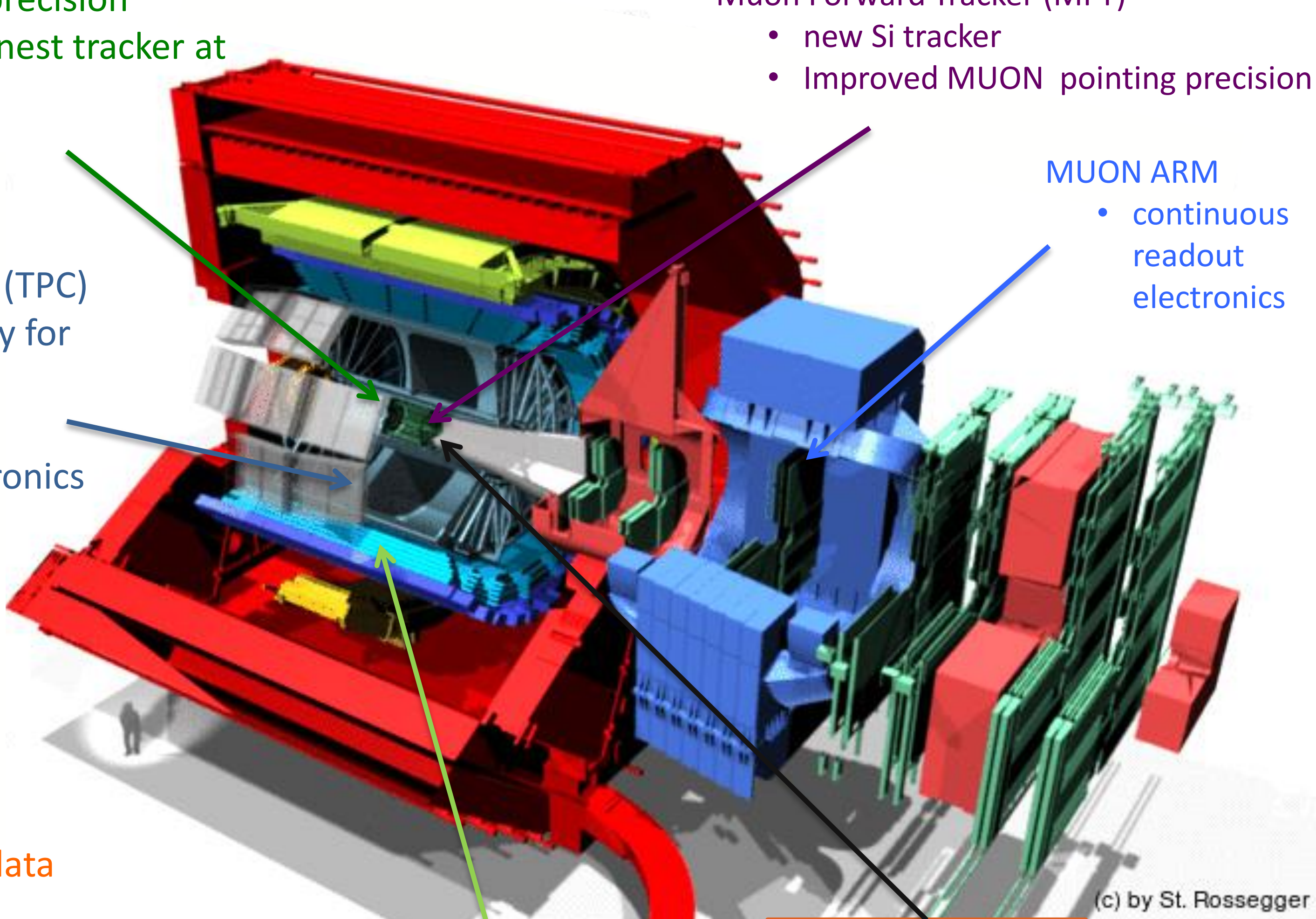

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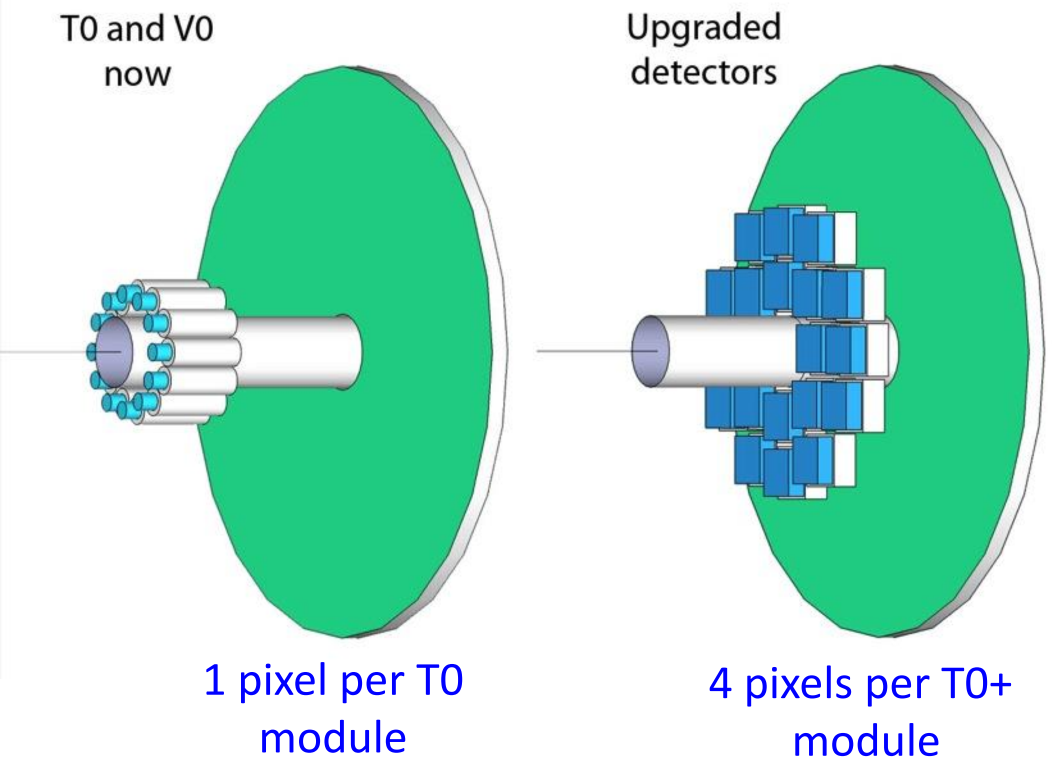
Fast Interaction Trigger (FIT)

Upgraded Quartz Cherenkov (T0+) and Plastic Scintillator (V0+)

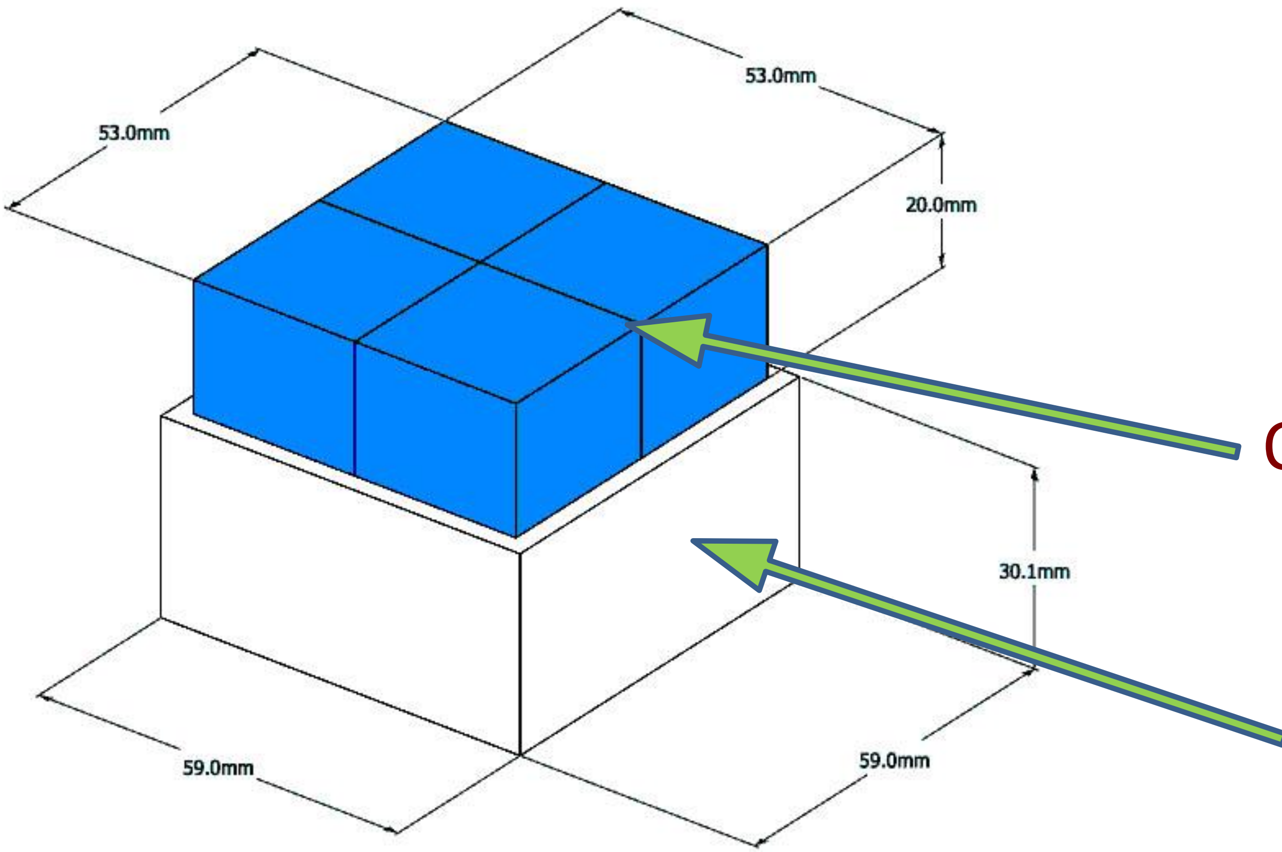


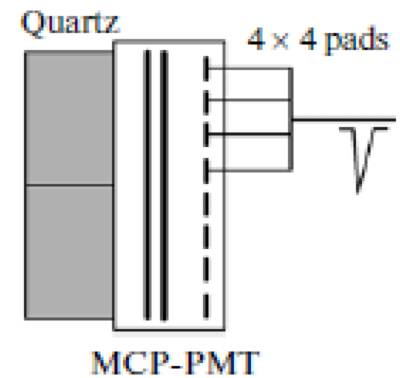
- **New** sensor: MCP-PMT
- **Larger** acceptance
- **More** channels

  T0 → 2 x 12 x 1 = **24**

  T0+→ 2 x 20 x 4 = **160**
- **Improved** readout

FIT: T0+



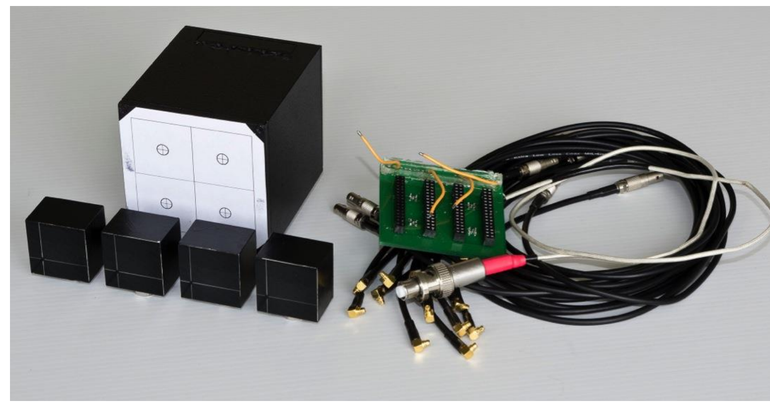


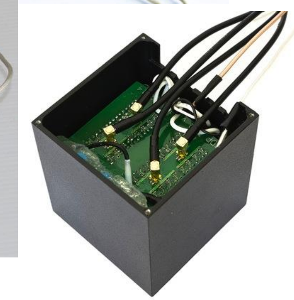
Quartz radiator
(segmented into 4)

MCP – PMT

FIT: T0+ Prototypes

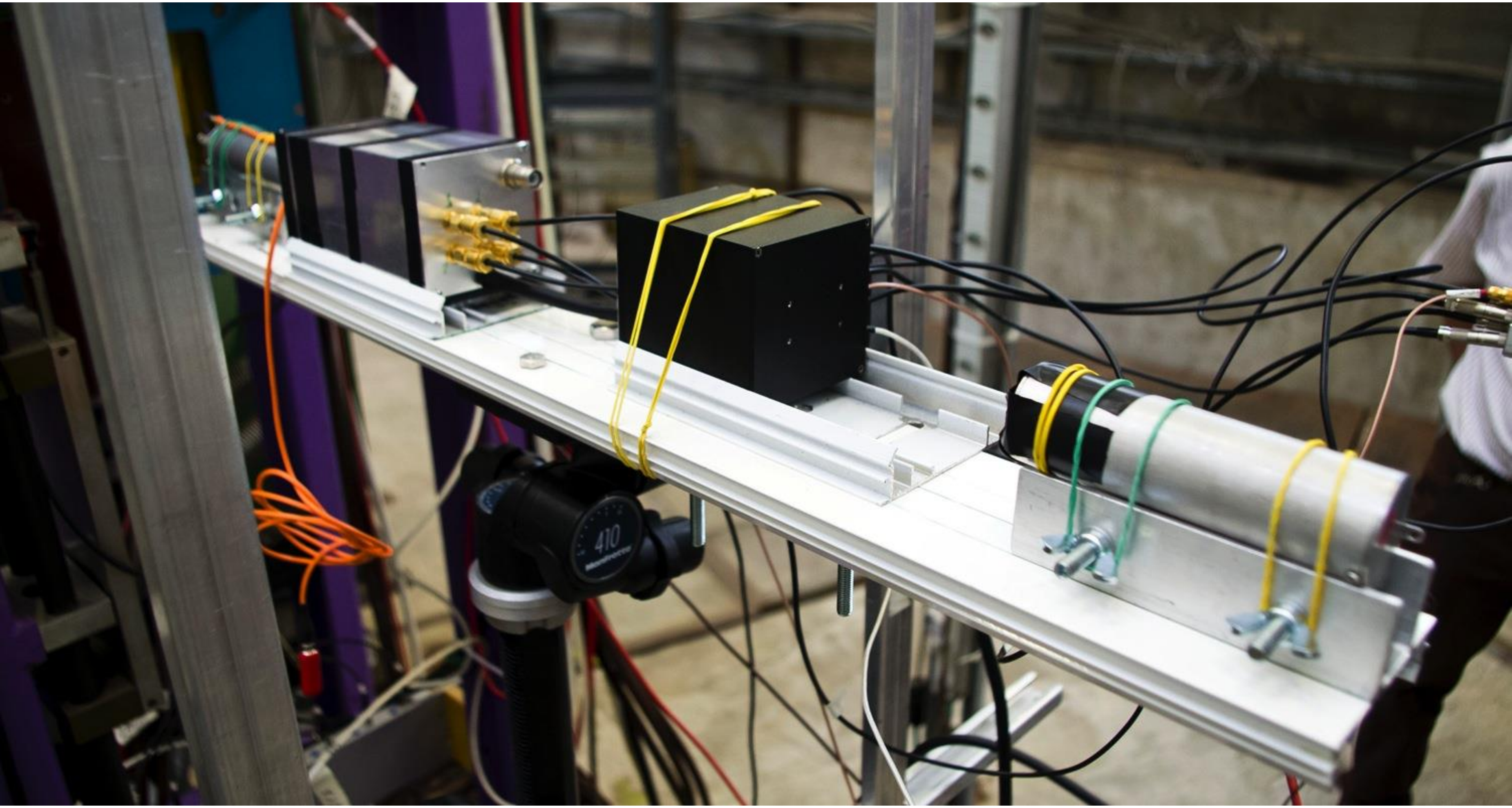
1st prototype with amplifier on the detector



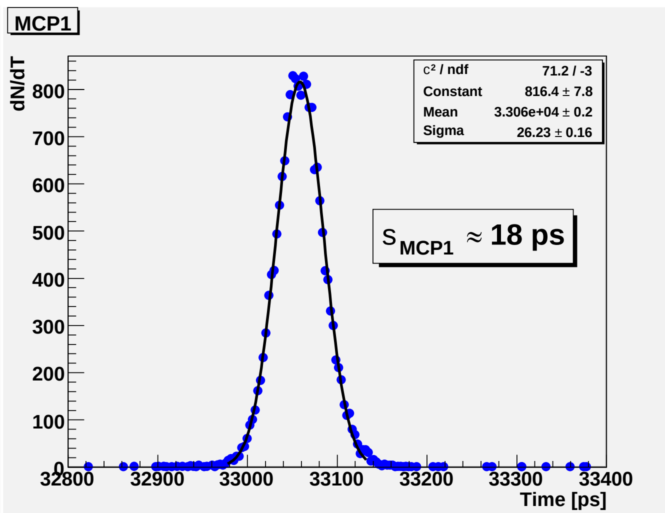


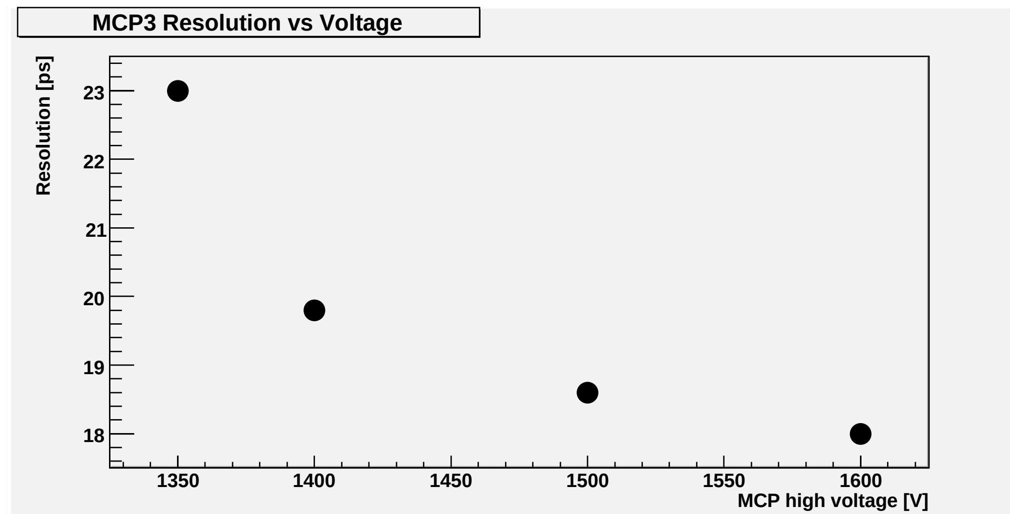
2nd prototype with amplifier after 8m of cable.

FIT: T0+ Prototypes Teastbeam



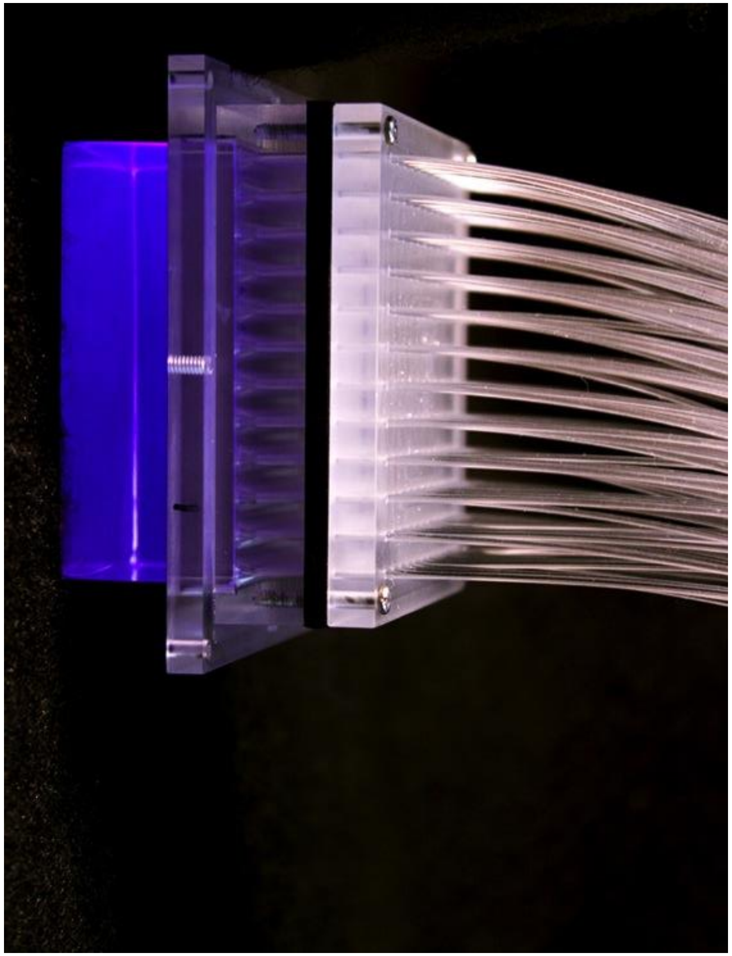
FIT: T0+ Time Resolution





Excellent time resolution !
For TOF Time Zero and Vertex Selection

FIT: V0+ Prototype



- Improved light collection scheme
- Reduced fiber length between the scintillator and PMT
- New sensor MCP-PMT (T0+)
- New electronics & readout (fully based on T0+ solution)

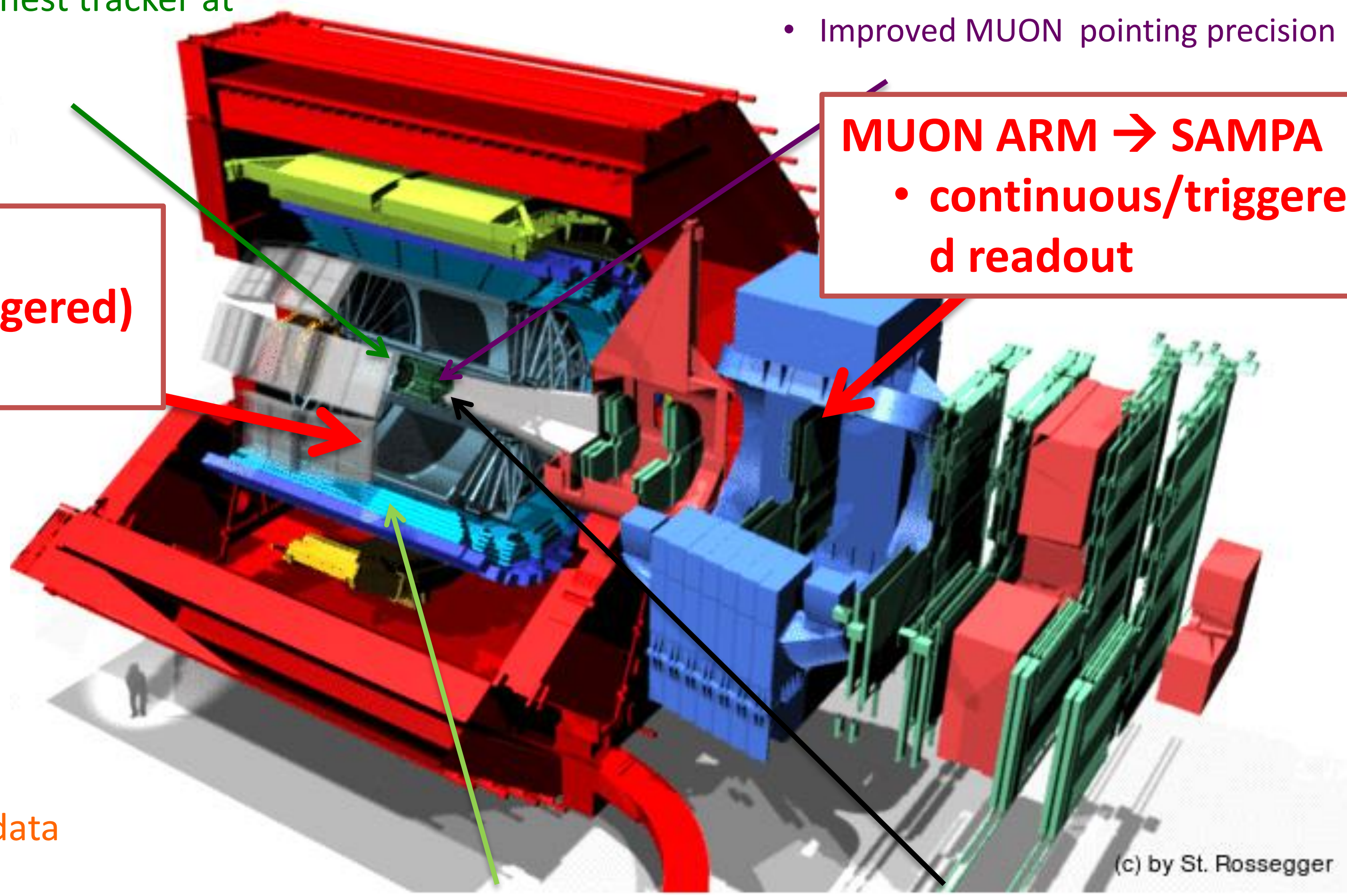
ALICE Upgrade

New Inner Tracking System (ITS)
- improved pointing precision
- less material -> thinnest tracker at the LHC

Muon Forward Tracker (MFT)
- new Si tracker
- Improved MUON pointing precision

MUON ARM → SAMPA
- **continuous/triggere d readout**

TPC → SAMPA
- **Continuou(/triggered) readout**



Data Acquisition (DAQ)/ High Level Trigger (HLT)
- new architecture
- on line tracking & data compression
- 50kHz Pbb event rate

TOF, TRD
- Faster readout

New Trigger Detectors (FIT)

SAMPA

- **SAMPA MPW1**
  - **3 ASICs**
    - ASIC 1, 5 front-end channels
    - ASIC 2, ADC and SLVS driver
    - ASIC 3, 3 channels including DSP and read-out
  - **Submission June 2014**
  - **Delivery Sept 2014**
    - Cut and packaged

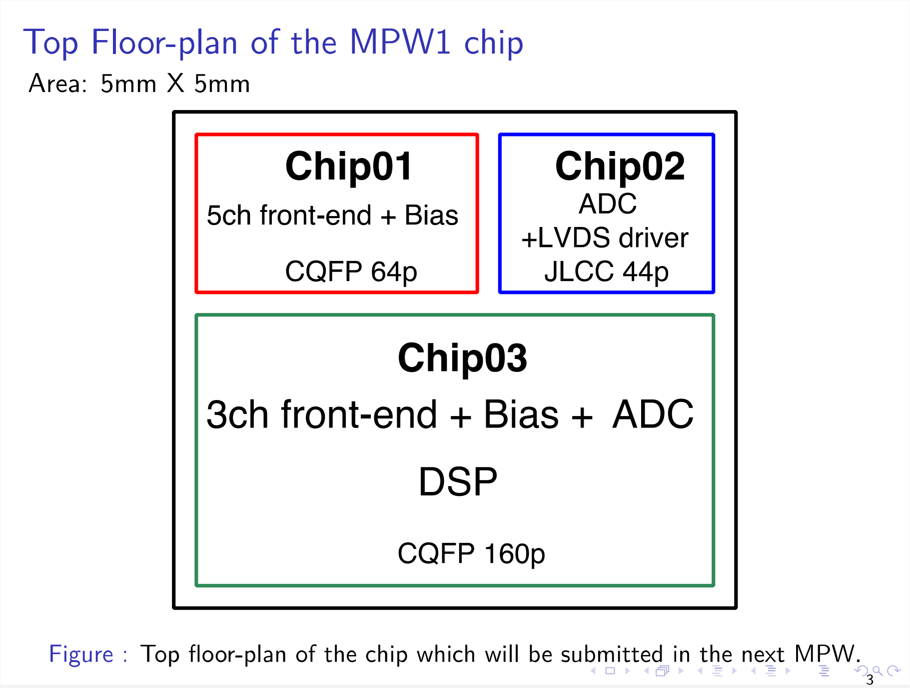
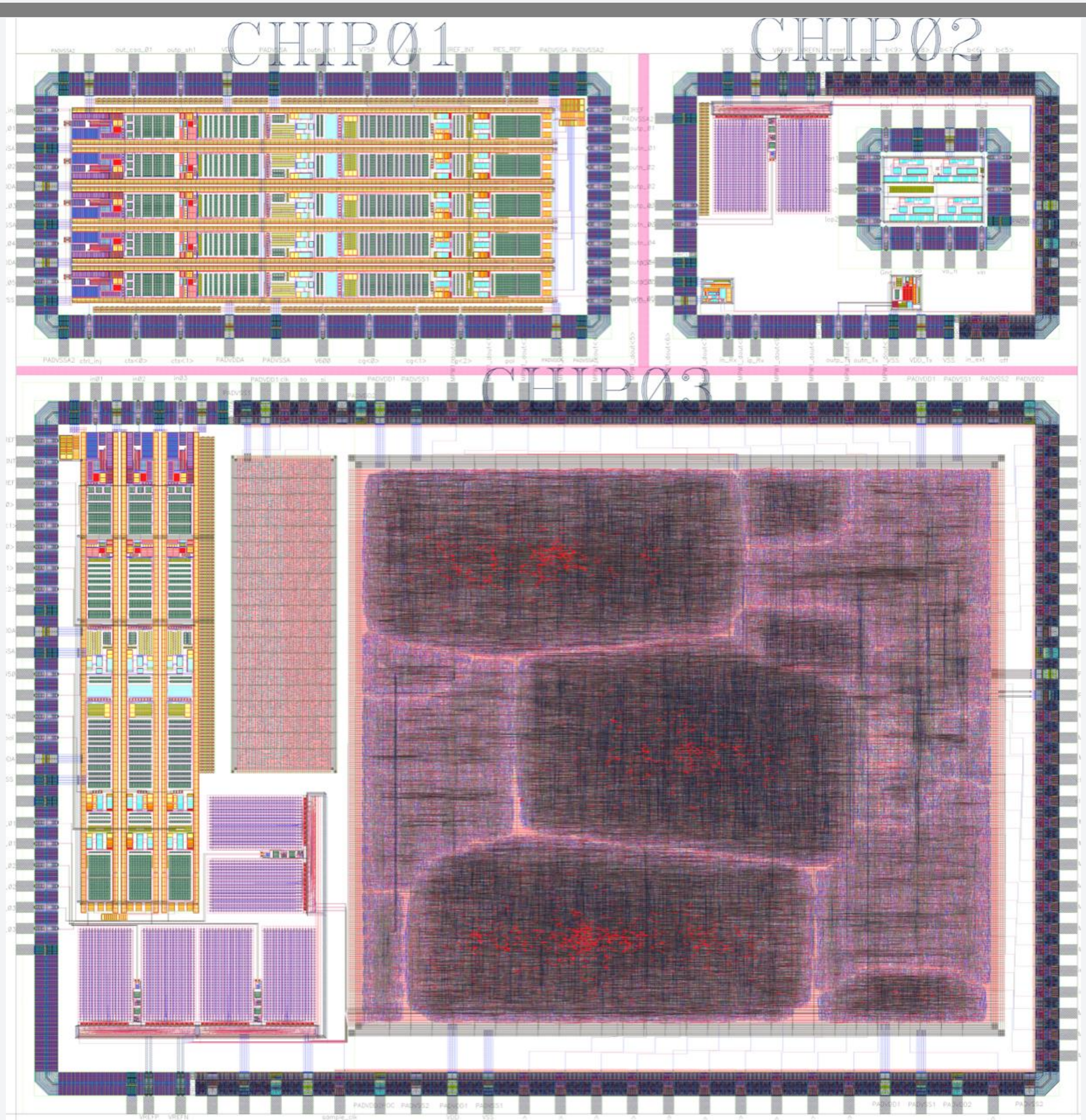


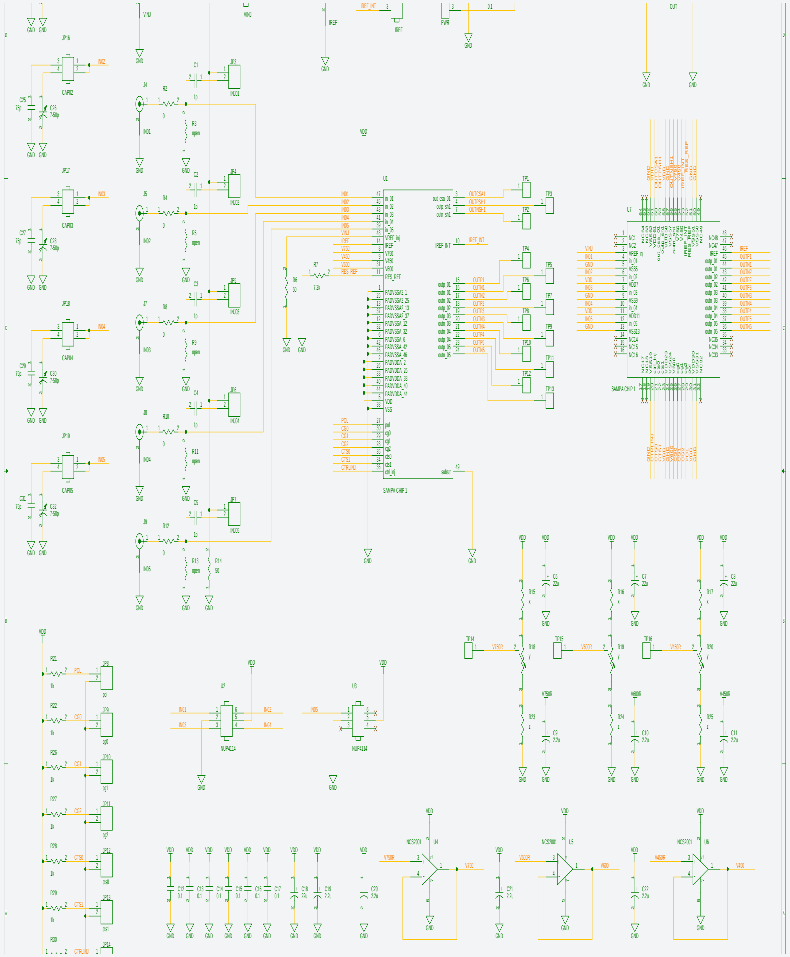
Figure : Top floor-plan of the chip which will be submitted in the next MPW.

SAMPA



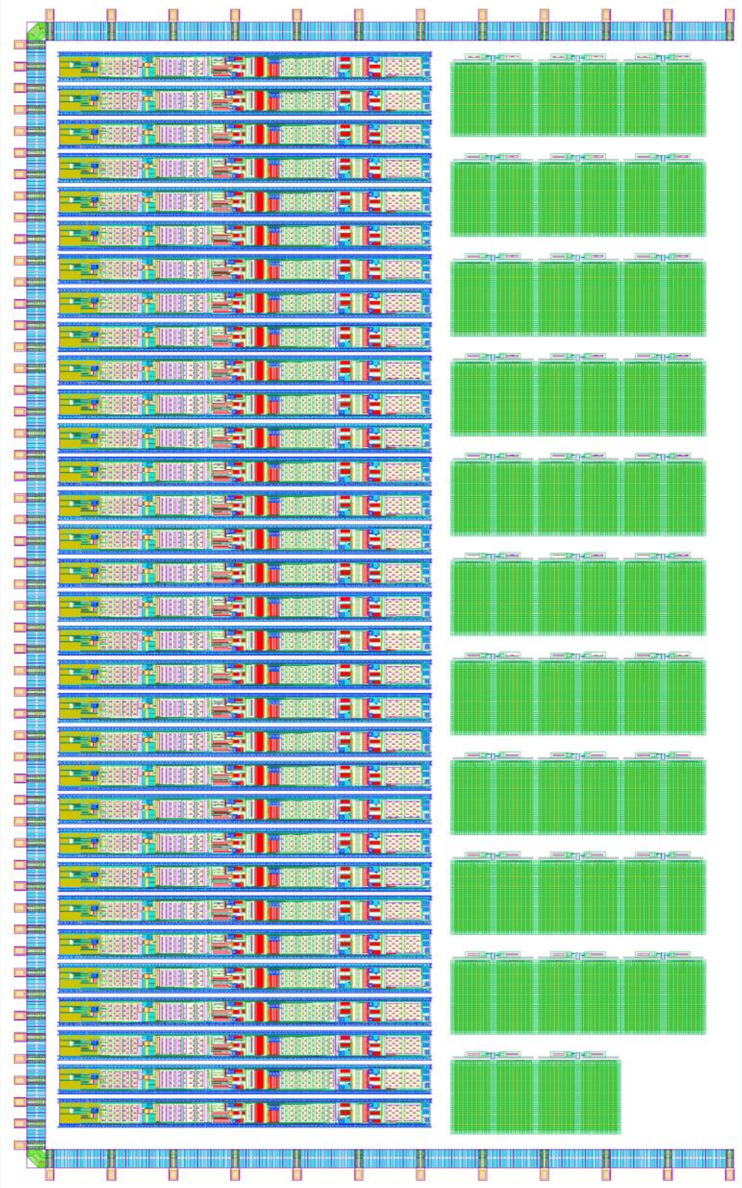
SAMPA

- **Test board design**
  - **Design Cagliari (MCH institute) for ASIC 1/2/3**
  - **Test board 1 & 2 design finalized (Brazil), 3 in the pipeline (Cagliari)**
  - **FPGA based read-out board (GBT – CRU emulator)**
    - Bergen (TPC institute) for ASIC 3
    - Hardware finalized, Firmware under development



SAMPA

- **SAMPA MPW2**
  - **32 – channel full scale ASIC**
  - **full layout presently under design**
    - changes/adaptations after the of MPW1 possibly needed
    - building blocks can be changed in the lower hierarchy without changing top level



Conclusions

Tests of full scale prototype for

- ITS pixel chips are ongoing and very promising
- TPC readout chambers in Nov. and Dec. 2014
- FIT MCPs were performed with very promising results

SAMPA

- MPW1 tests very soon
- Full scale SAMPA chip for MPW2 in preparation

TDR

- for MFT in Nov. 2014
- for O2 in Jun. 2015