WP 9.3 FEI4 telescope arm

Fabian Hügging on behalf of
IFAE Barcelona, U Bonn & DESY

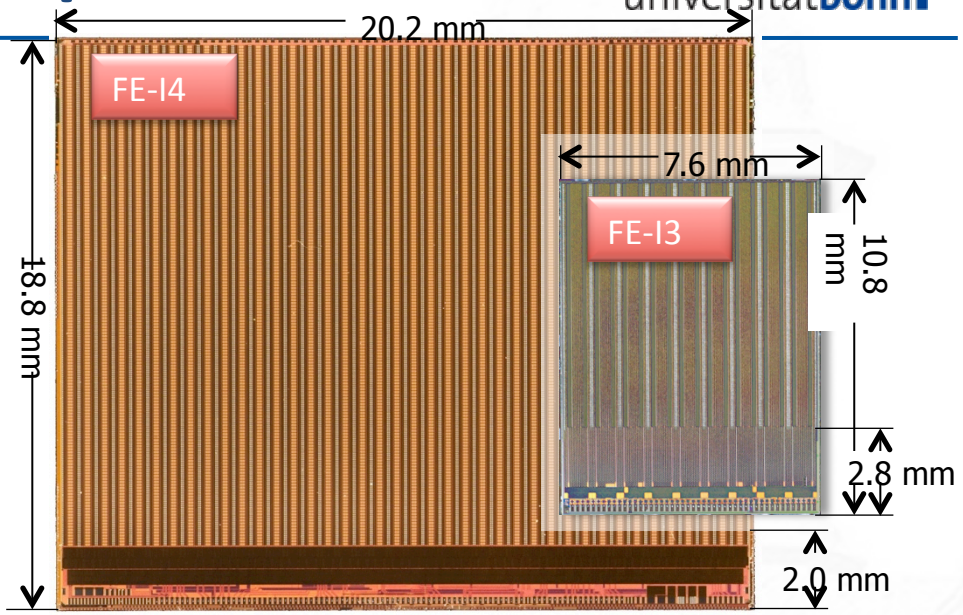
huegging@physik.uni-bonn.de

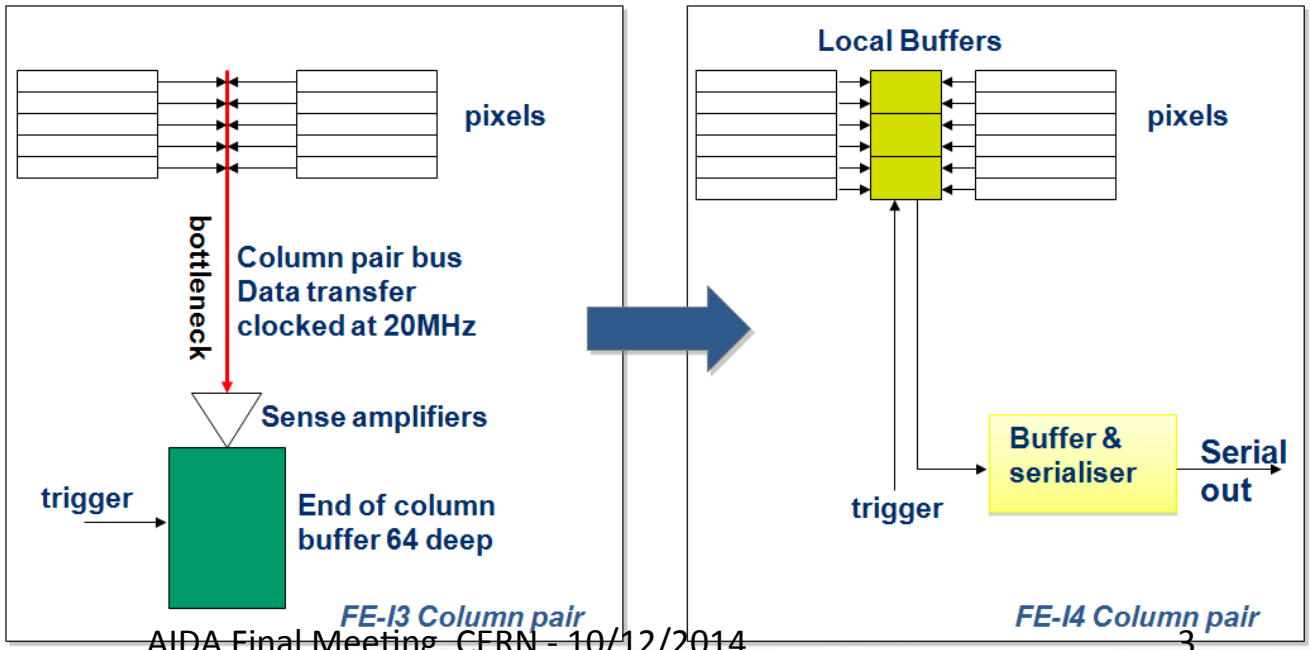
Overview

- FE-I4 pixel readout chip
- FE-I4 telescope arm:
  - Region of interest (ROI) trigger implementation
  - Fast time-stamping feature
  - Quad module FE-I4 arm for the SALAT planes

ATLAS pixel readout chip for IBL: FE-I4

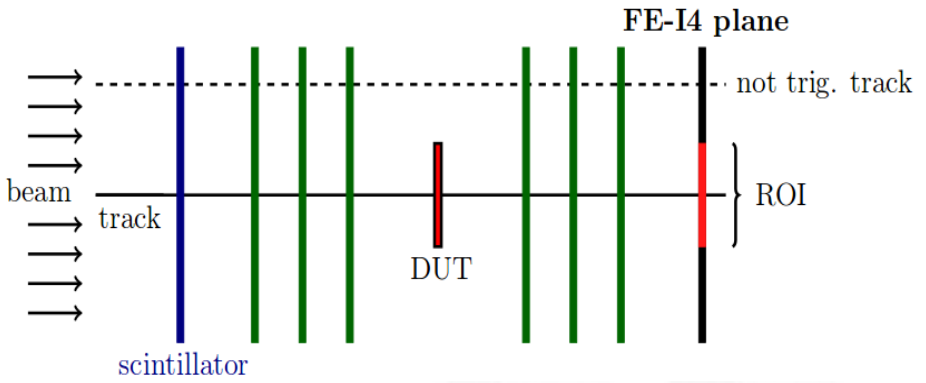
- successor of current (50 x 400 µm²) FE-I3 for IBL
  - smaller pixels (50 x 250 µm²)
  - lower noise and threshold operation
  - higher data rate compatibility
- column drain architecture with local hit storage
- IBM 130 nm
- array size: 80 col. x 336 rows 26880 pixels, 16.8 x 20 mm² active area, 7x10⁷ transistors
- average hit rate @ 1% inefficiency = 400 MHz/cm²
- max. trigger/readout rate: 200 kHz
- time stamping with 40 MHz clock
- **FE-I4 works very well!**

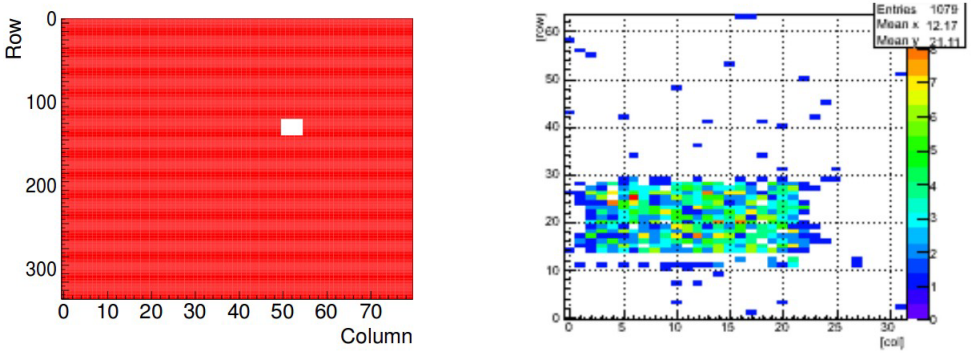




ROI trigger with FE-I4 telescope arm

- FE-I4 features fast asynchronous hit signal of pixel matrix called hitbus:
  - signal is an OR of the output of all pixel discriminators
  - pixel contributing to the hitbus can be configured with a special pixel mask
  - can be used as self trigger (internally) or for telescope trigger (externally)
  - in addition to standard readout path
- hitbus signal needs to be adapted to application:
  - inverted for TLU
  - amplification for long cables





(a) ROI of FE-I4 plane. (b) Hitmap of DEPFET DUT.

Figure 6: Selected ROI, which is smaller than the DEPFET and corresponding hitmap of DEPFET.

ROI trigger with FE-I4 telescope arm

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- ROI trigger successfully implemented into telescope hardware and software since 2012
- It is used by many groups: DEPFET, active CMOS etc. to increase trigger efficiency for small test chips
- for further details see AIDA technical note:
  - https://cds.cern.ch/record/1499551/files/AIDA-NOTE-2012-005.pdf

AIDA-NOTE-2012-005

AIDA

Advanced European Infrastructures for Detectors at Accelerators

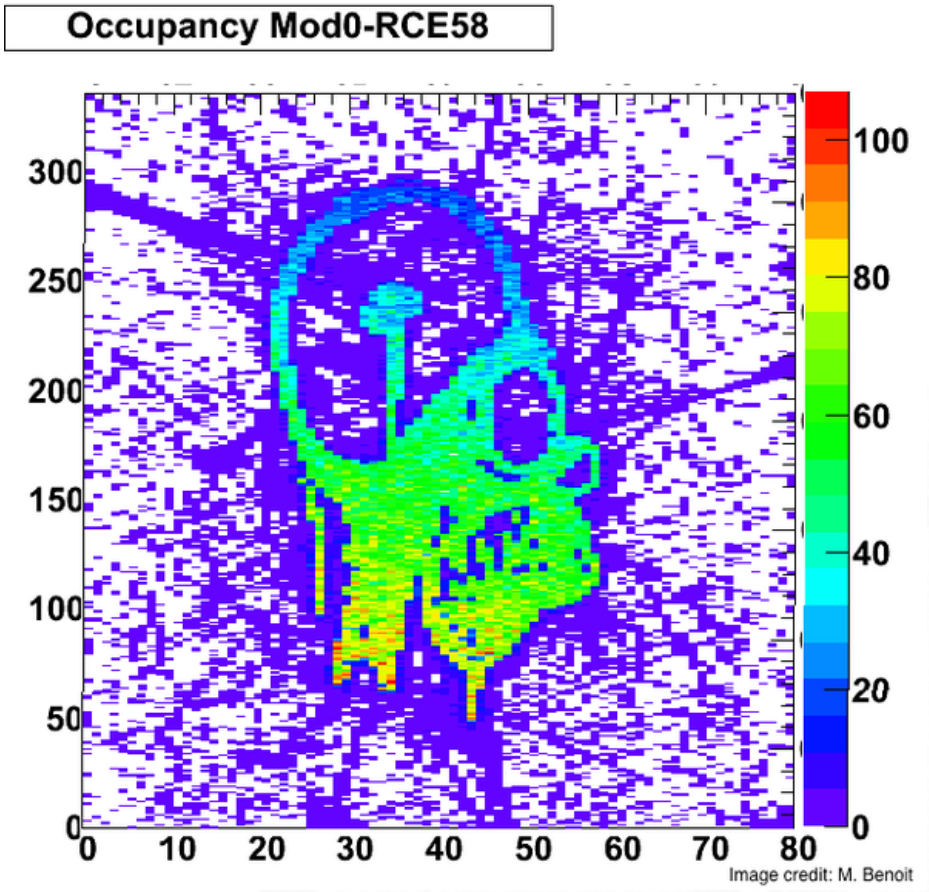
Scientific / Technical Note

Implementation of a Configurable FE-I4 Trigger Plane for the AIDA Telescope

Obermann, Theresa
et al

12 December 2012

Hitmap of ATLAS pixel detector in a muon beam with a selected region of interest



Published by M. Benoit on ATLAS twitter account:
https://twitter.com/ATLASexperiment/status/540178275948314624

Readout system for FE-I4 arm

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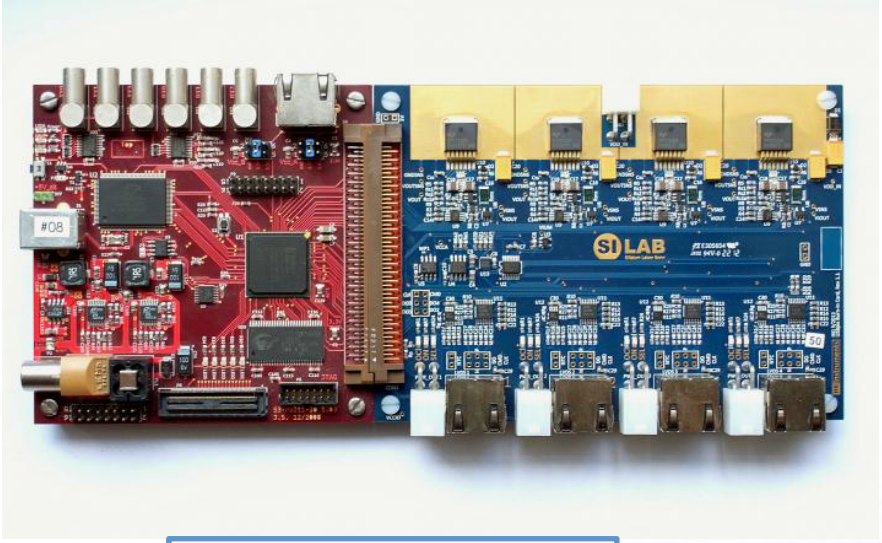
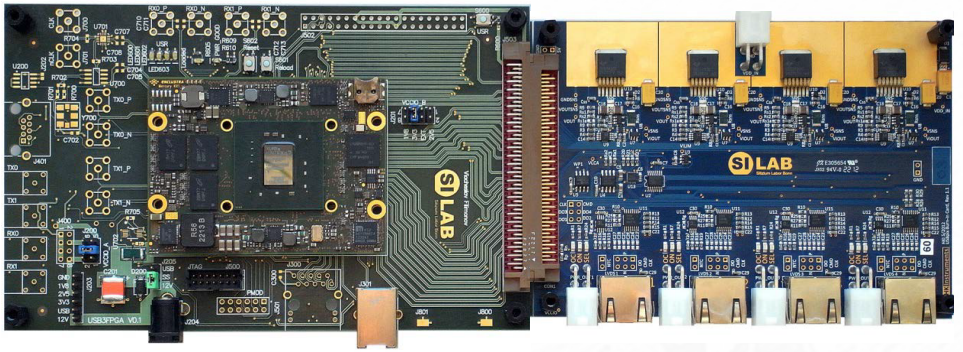
- Readout system is based on Bonn developments for ATLAS pixel:
  - USBpix and new USBpix3:
    - full support of single quad modules using burn-in card
  - Python based software pyBar:
    - full 4-chip readout
    - No interrupt during data taking
    - Continuous trigger rate up to 200kHz
    - higher peak trigger rate possible
    - full support of the TLU and the new miniTLU
  - tested standalone with FE-I4 modules in test beams and with EUDET telescope
  - integrated into EUDAQ2
  - final test with Mimosa planes, EUDAQ2 and miniTLU to be done

USBpix with burn-in card for up to 4 FE-I4 chips

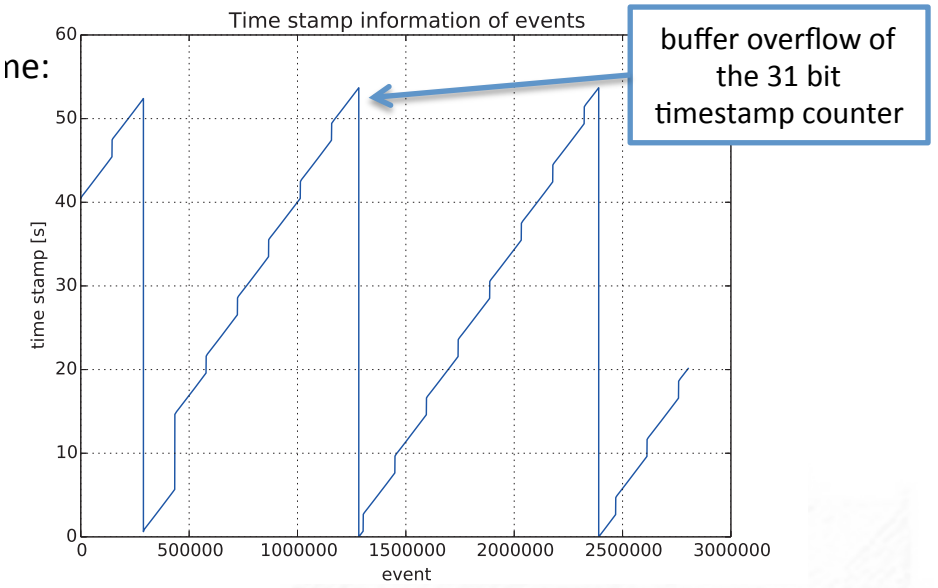


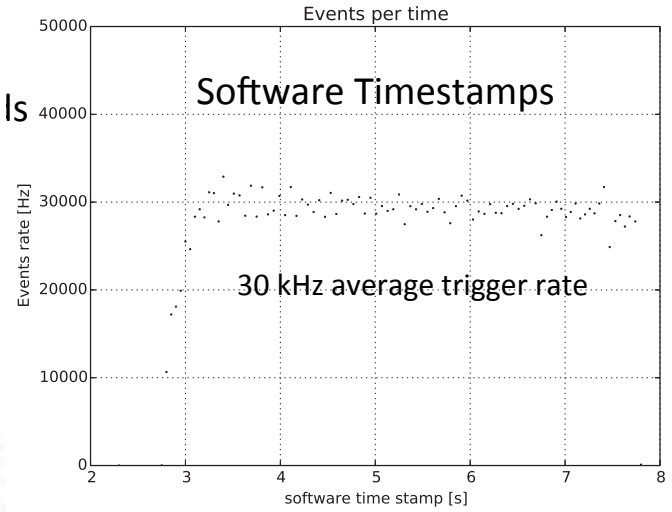
New USBpix3 with burn-in card



Fast time stamping of FE-I4

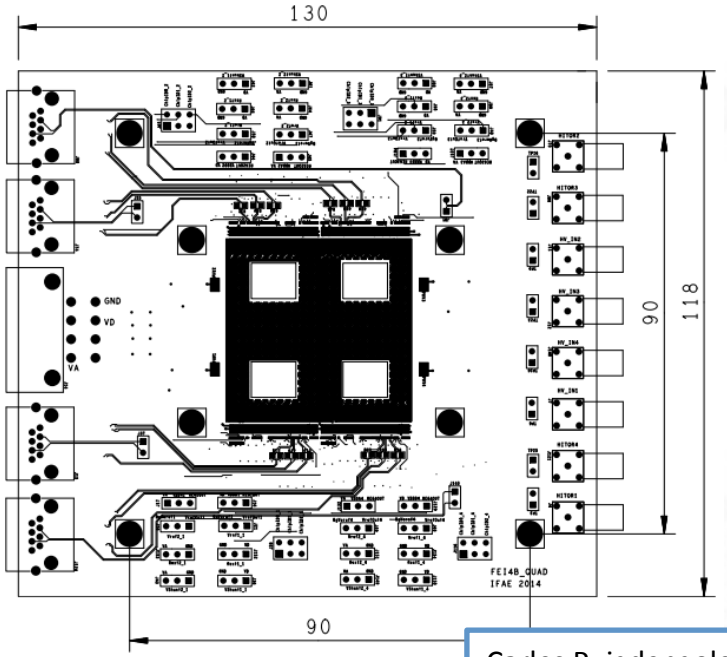
- New AIDA readout architecture requires fast trigger time-stamping.
  - FE-I4 provides an intrinsic time resolution of 40 MHz (25ns)
  - time-stamping feature need support from readout software (producer) and must delivered from/to TLU
- Time-stamping of FE-I4 arm tested standalone in a beam environment:
  - 30 kHz particle rate from accelerator
  - TLU used for trigger/handshake
  - trigger time-stamping rate of 30 kHz could be achieved with no problems by generating the time stamps inside the software
  - higher rates are possible by generating time stamps inside the FPGA (up to 150 kHz peak rate has been achieved)
- Final testing of the trigger time-stamping with EUDAQ2 and miniTLU still to be done.



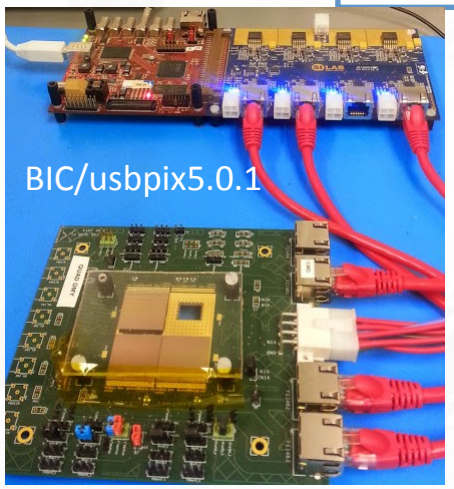


Quad module FE-I4 arm developments

- Dedicated PCB for quad modules:
  - Each FE has a its HitOr output
  - HitOr inverted on PCB
    - require an extra power supply
  - Mechanics compatible with telescope
  - can be equipped with single chip or quad modules
  - Module(s) powered through on chip regulators
- Several PCBs built:
  - 1st equipped with bare FE-I4 chips for testing
  - 2nd is equipped with 2 single chip modules and tested at Barcelona
  - 3rd is being equipped with a quad module at Bonn

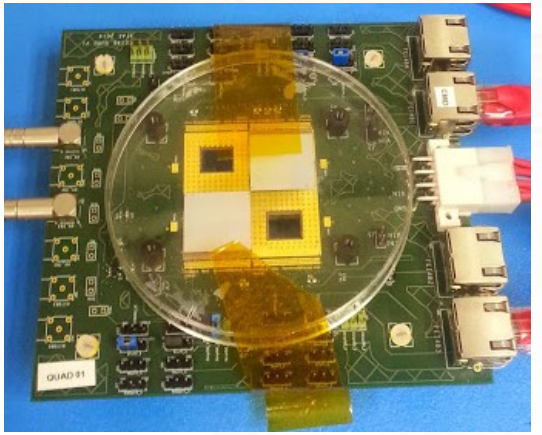


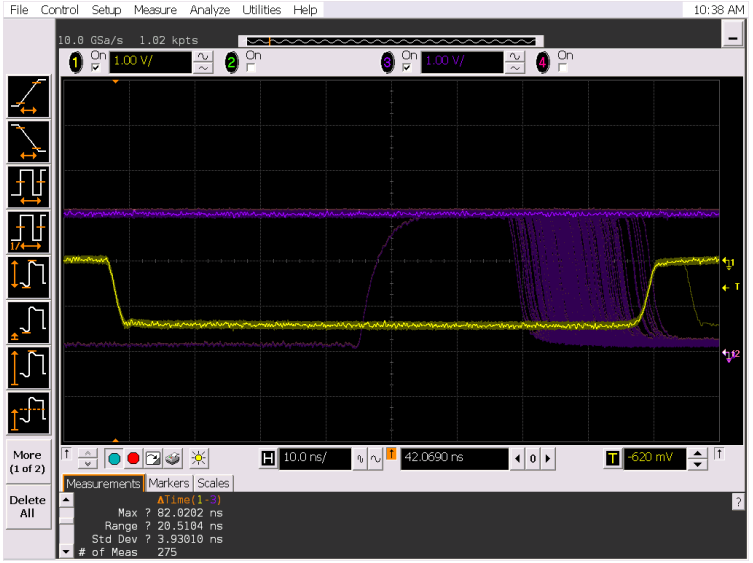
Carles Puigdengoles (IFAE)



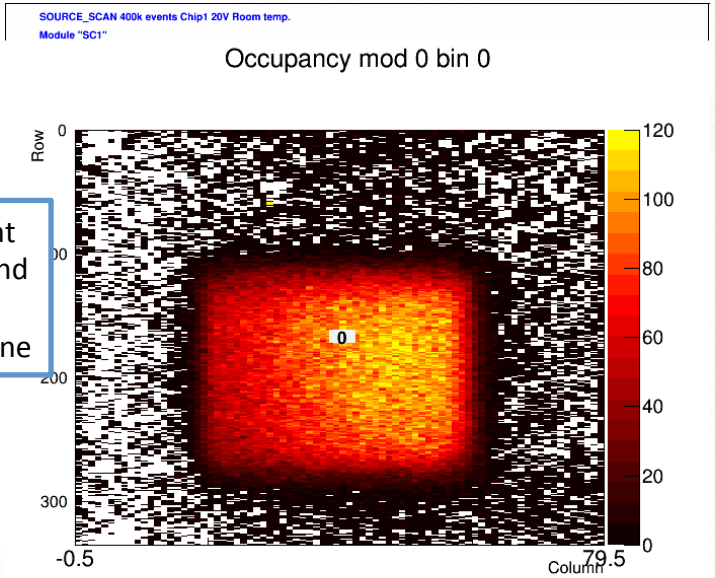
Quad FE-I4 arm equipped with 2 FE-I4

- Quad FE-I4 arm with 2 FE-I4 successfully used in Nov testbeam at Cern:
  - operation with EUDET telescope & RoI trigger works
- Time jitter including FE-I4 timewalk measured to be ~4ns
  - expect 100 ps jitter from the inverted hitbus signal
- Test with new miniTLU still to be done:
  - software for trigger and clock handling in place but not fully tested
- Final test together with large area AIDA telescope (including SALAT planes) to be done





Time jitter measurement done with ^{90}Sr source and a szintillator trigger behind the detector plane



source scan of 1 FE-I4 chip

Conclusions

- A fast telescope telescope arm with FE-I4 has been developed
  - Region of interest trigger capabilities implemented, tested and in use.
  - fast trigger time stamping (25 ns) architecture implemented and tested standalone
  - quad FE-I4 plane(s) are almost done for the final AIDA telescope
  - FE-I4 telescope arm and readout system has been re-designed taking into account requirements with miniTLU trigger/CLOCK distribution, and already tested with EUDAQ2
  - documentation (AIDA notes, thesis and manuals) are done or in preparation