WP3-3
IP blocks

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OMEGA/IN2P3

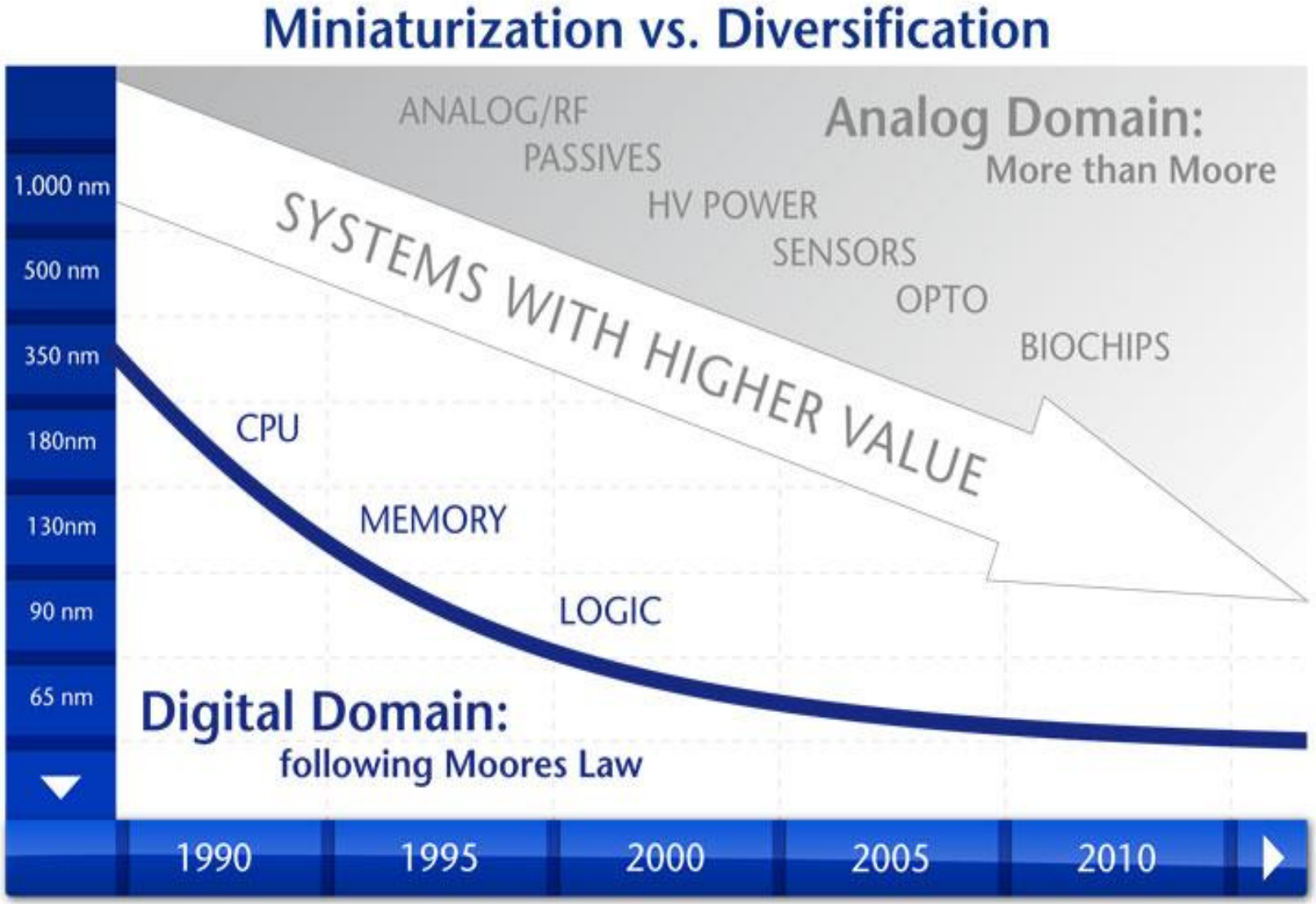
WP3-3 task

Goal : provide 2nd lot of IP blocks for needs in HEP with full documentation and laboratory tests.

This 2nd set was organized by OMEGA in XFAB SOI 180nm technology.

This chosen technology is more dedicated for analog domain (calorimetry, TPC,…)

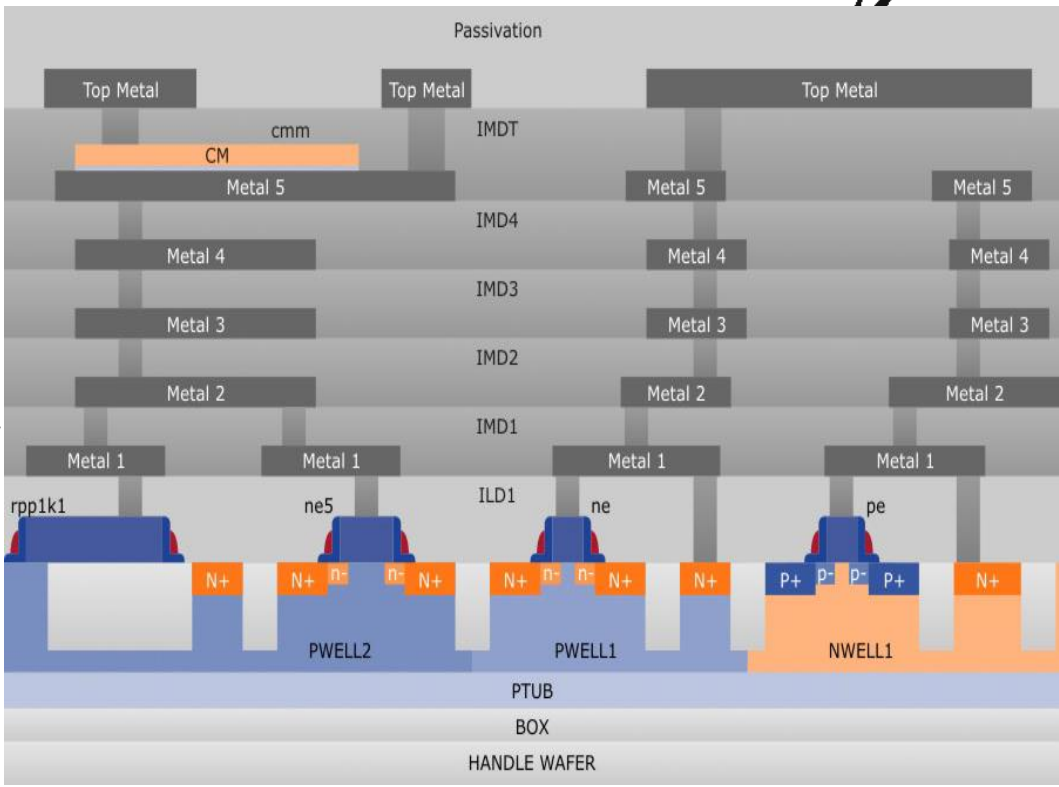
More than Moore



XFAB 0.18µm SOI CMOS

XT018 0.18µ HV SOI CMOS:

- Up to 6 Metal (one thick)
- 1 poly (high res) – MIM capacitors
- Deep N-well and P-well modules
- power supply : 1.8V, 3.3V or 5V (option)
- 200V MOS
- digital cells



- **Price : from 1000€/mm2 to 1200€/mm2 (10mm2 minimum area and 5 samples**
- **3 MPW runs /year : 10 feb. , 19 may, 22 sept**
- **Chosen run : 19 may 2014 delayed to mid july 2014**

2nd set of IP blocks (I)

- Techno : XT018 0.18µ HV SOI CMOS
- NDA signed with XFAB
- Design kit provided directly by XFAB
- Chosen run : mid May 2014 delayed to mid July 2014
- 3 labs involved in the IP blocks (CCPM,LLR,OMEGA)
- 10 dies received last week to be packaged and measured

2nd set of IP blocks (II)

Blocks submitted :

- CCPM :
  - Sensors
  - Transistors for test
- LLR :
  - Serial link
  - Analogue memory
  - Delay box
  - Premplifiers, shapers, discriminator
- OMEGA
  - Bandgap, Wilkinson ADC

Omega also assembled all the IPs blocks to send them to the foundry

All the blocks are described in the report : AIDA-Del-D3-9

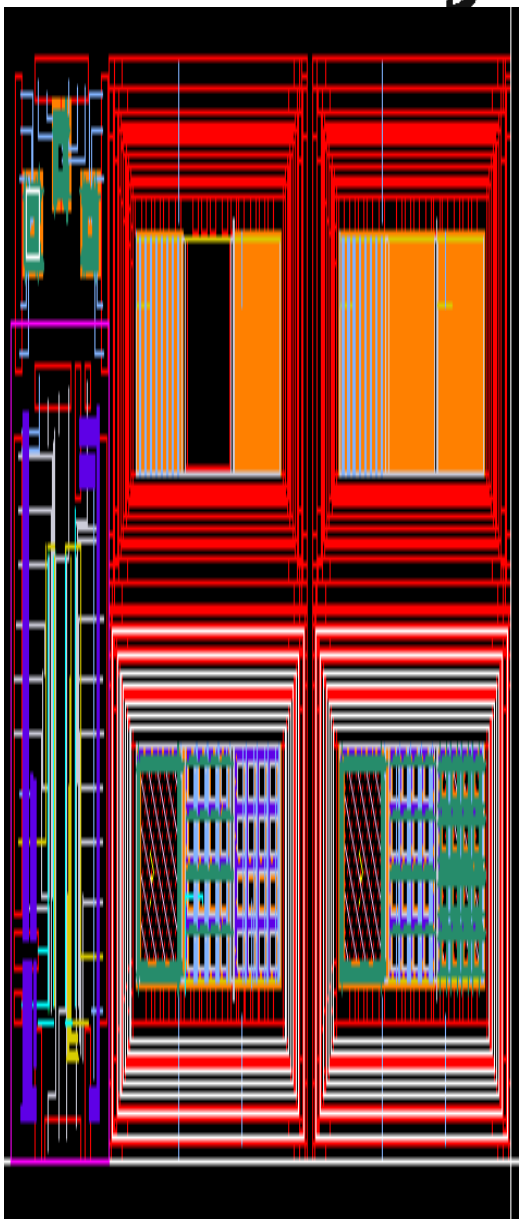
Blocks from CCPM

Test structures of transistors and diodes :

The main objectives are to be able to test several pixel layouts and several guard ring strategies for the upgrade of the ATLAS pixels detector.

Complete layout size : 2 x 5 mm2

Contact : Patrick Pangaud and Alexander Rozanov at CCPM



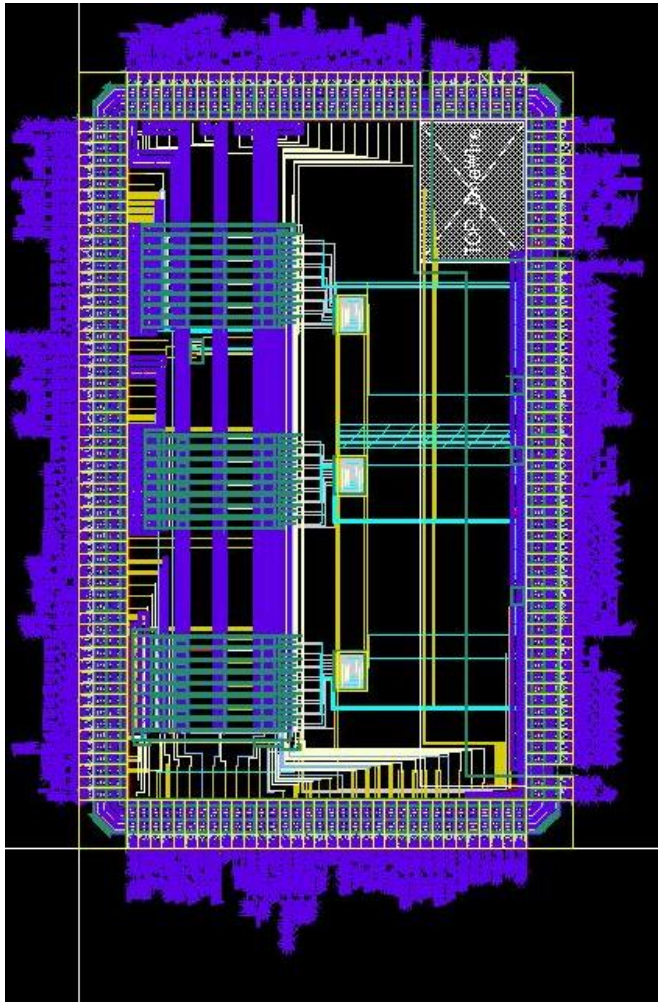
Blocks from LLR and OMEGA

All the blocks are gathered in a same chip

Power supply used 1.8V

Complete layout size :
2.5 x 4 mm2

The various blocks were presented at TWEEP 2014 :
J.B. Cizel et al, “Building Blocks X-FAB SOI 0.18 µm” in *TWEPP*, Aix-en-Provence, 2014

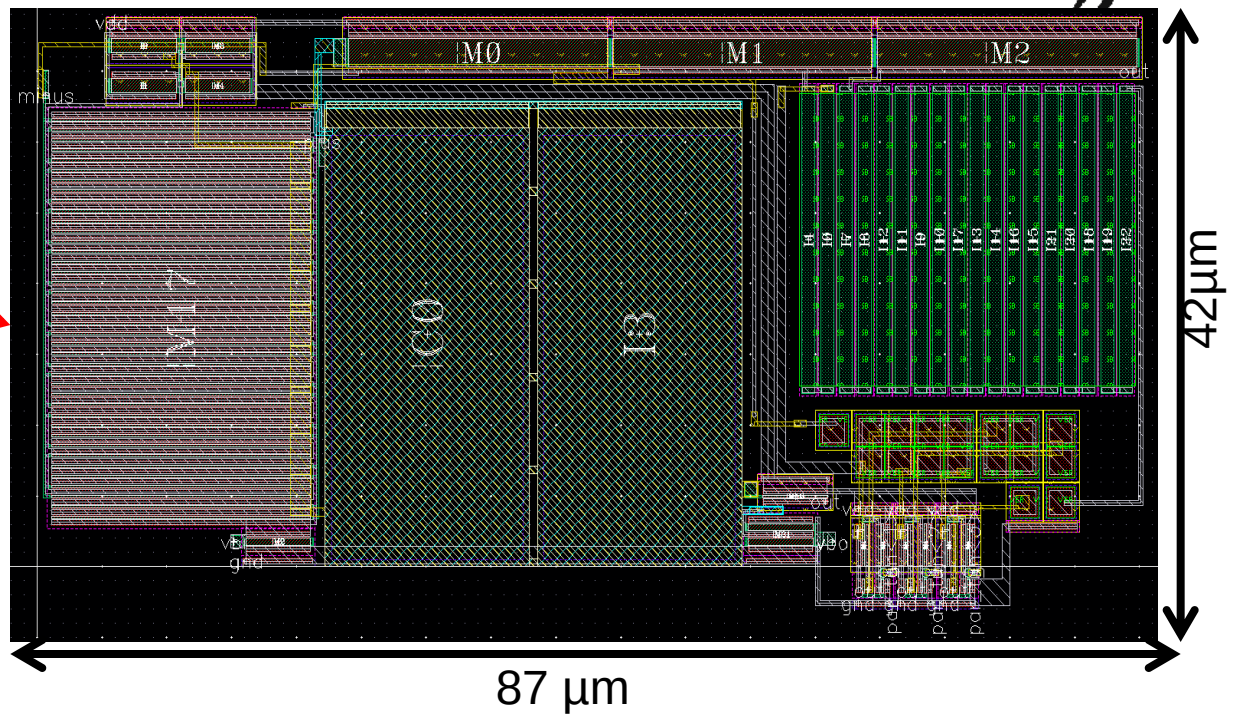


Blocks from OMEGA

Bandgap

Voltage : 1.1V

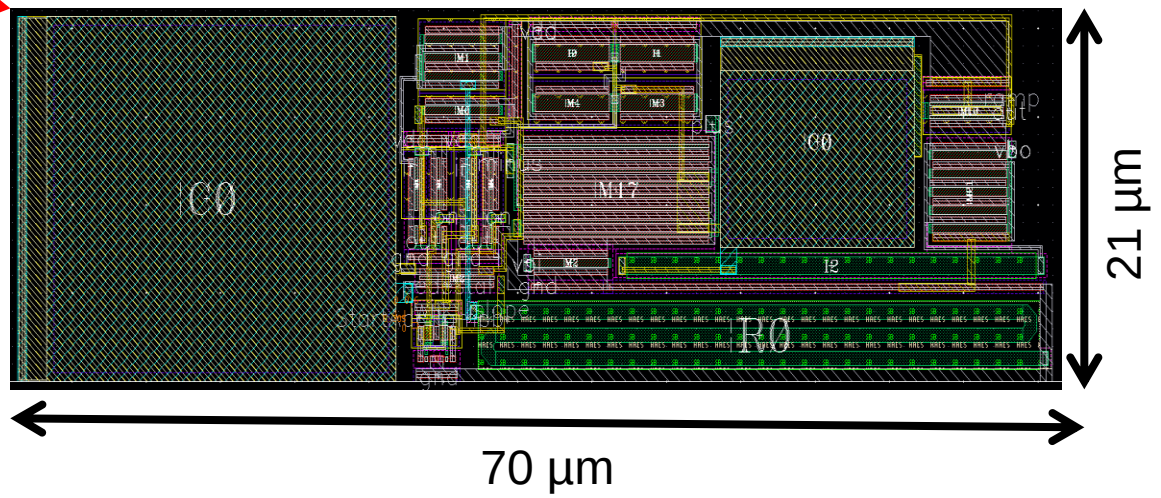
Disspation < 30µW



Wilkinson ADC

10bit @160MHz

Ramp dissipation < 20µW

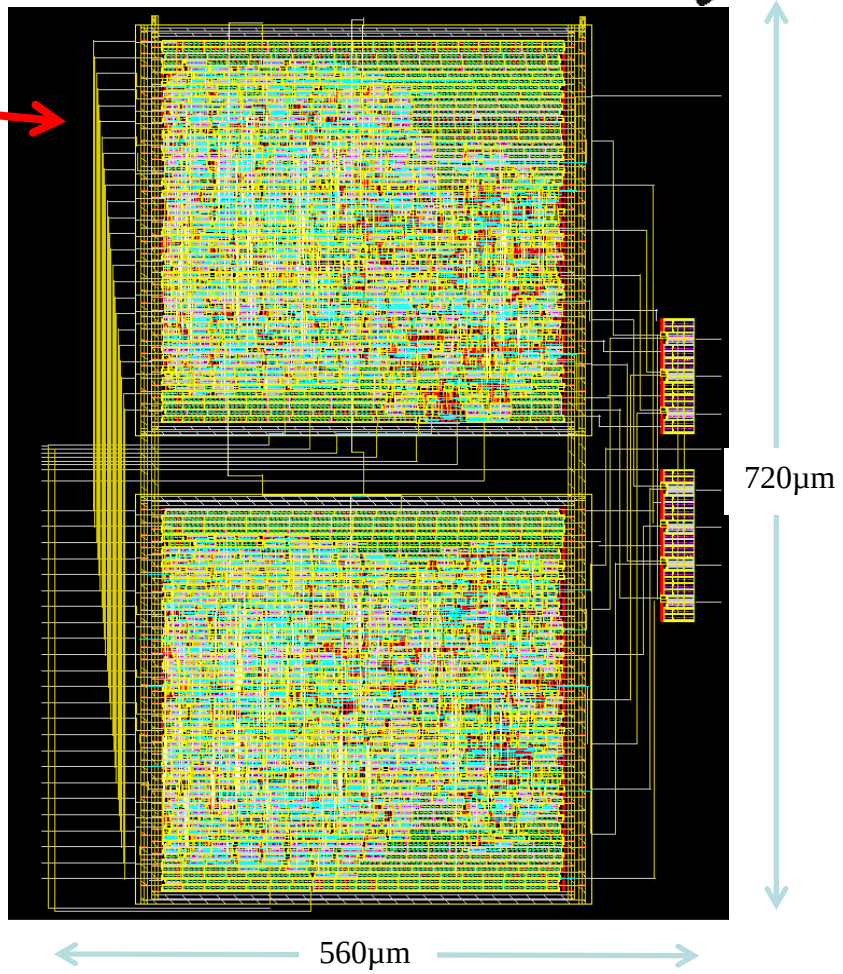


Contact : Stephane Callier,
Gisele Martin-Chassard
at OMEGA

Blocks from LLR

Serial link :

Power supply : 3.3 V
Clock frequency :125 MHz



Preamplifier :
3 types : PMOS, NMOS or differential pair at the input
Dissipation : 1mW
Noise < 1000 e-
Dynamic range > 2000MIP

Shapers :

Fast shaper :
time constant : 30ns, gain : 100, dissipation 300µW
Slow shaper :
Time constant :180ns, gain 30 and 2, dissipation : 50µw

Contact : Jerome Nanni , Jean-Baptiste Cizel at LLR

Conclusion

2nd set of IPs block was sent in fab last July

Dies were received last week

Packaging will be performed soon

Characterization of these blocks will follow

→ Deliverable report D3.9 published in november

Thank you
for your attention