# CERN 65nm IP blocks

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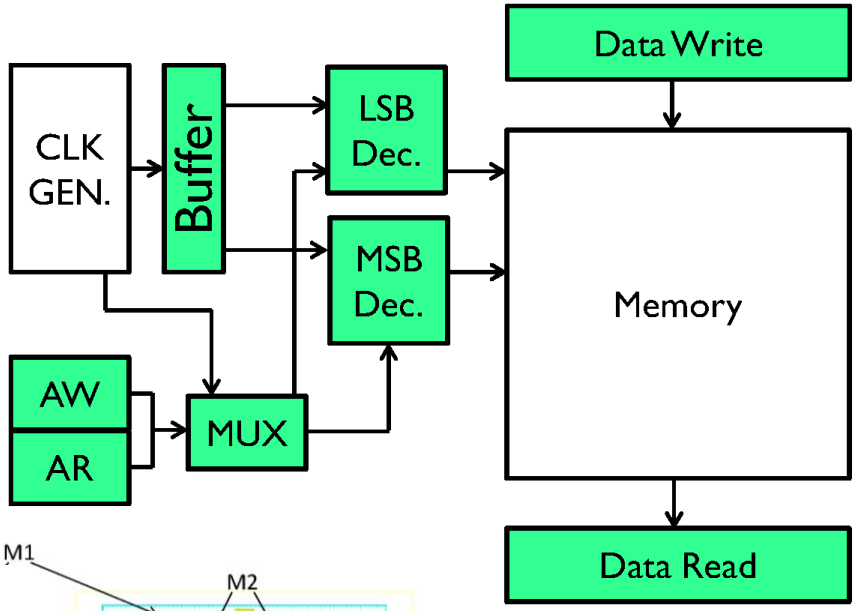
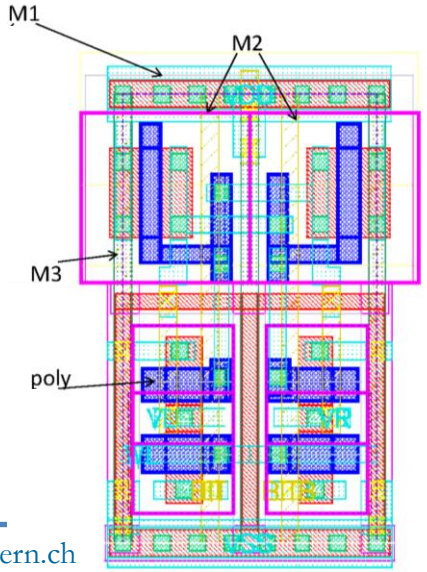
# Rad-hard IP Blocks in 65nm

- SRAM compiler
- I/O pad library
- Monitoring ADC
- Bandgaps
- Rad-hard to 200Mrad according to specifications
- Deliverables
  - Schematic (OA)
  - Layout (OA)
  - Abstract (OA)
  - .lib (Liberty) capacitance limits and timing if applicable
  - Verilog / Verilog-AMS models
  - Datasheet

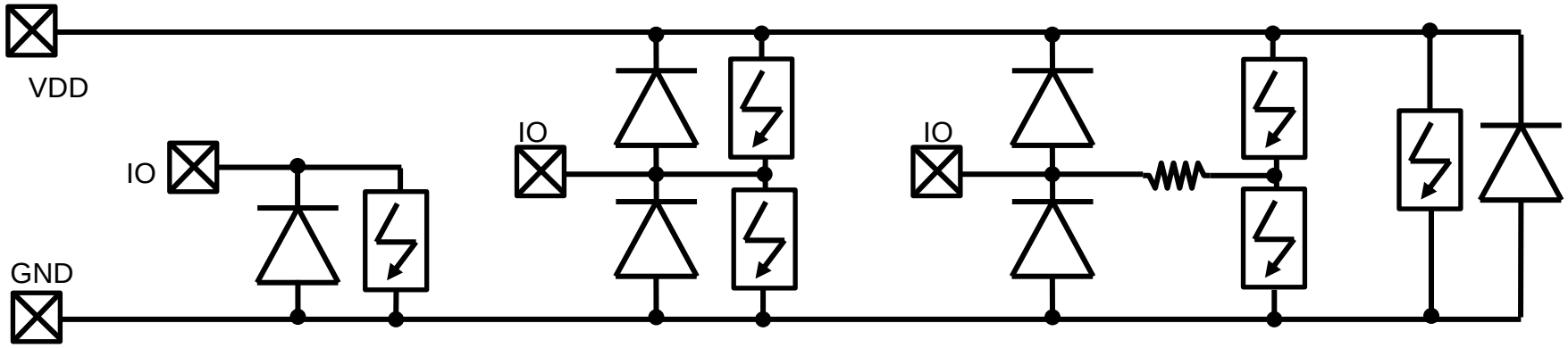
# SRAM Compiler

- Pseudo-dual-port (one read + one write in one clock cycle)
- 80 MHz operation
- Minimum size: 128 words of 8 bit
- Max size: 1k words of 256 bits
- Specifications on minimum W of transistors for radiation hardness
  - WPMOS>500nm, WNMOS>200nm
  - Cell size: 1.450 x 2.535 um2
- Part of the blocks are SET tolerant (in green in the figure)
  - If Hamming or other coding is used, SRAM becomes fully SEU tolerant
- Power consumption (simulated for a 1024x32 SRAM)
  - Read+write: 30 uW/MHz
  - Only read: 16 uW/MHz
  - Only write: 17 uW/MHz
  - Idle/static: 3 uW
- Test chip back from fabrication 21/11/2014
  - Silicon & radiation tests will follow
- Presented at AMICSA: https://indico.cern.ch/event/277669/session/5/contribution/12



# ESD structures and I/O pads



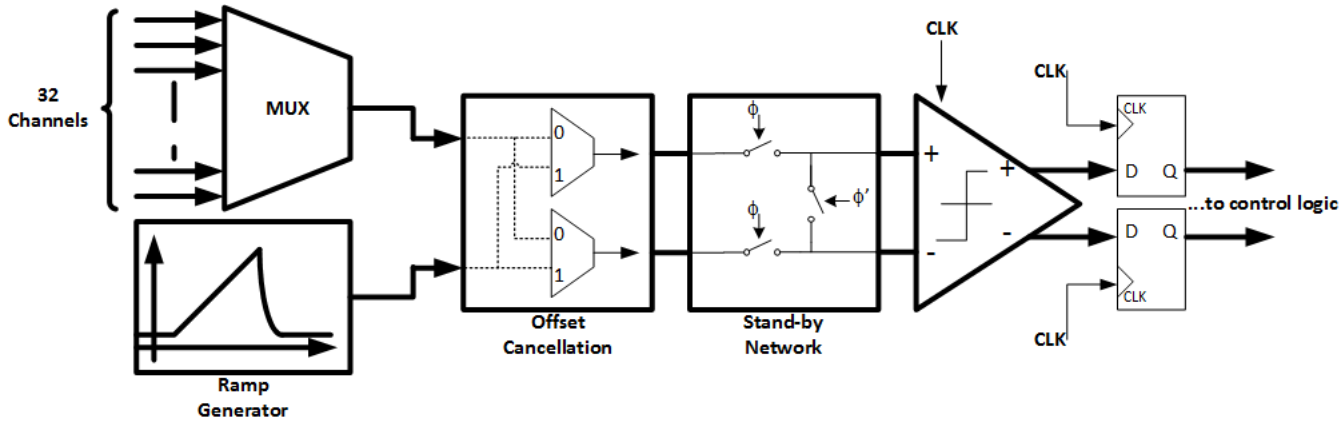

- Rated for 1.2V
- Only core devices, thin gate oxide
- Outsourced the development work for rad-hard ESD circuitry
  - Power clamps
  - Low-capacitance analog I/O (160 fF, 1 kV HBM ESD)
    - No connection to VDD/DVDD to avoid power supply noise
  - HBM+CDM ESD-protected I/O for digital (200fF, 2 kV ESD)
  - Delivered May 2014

- I/O drivers and receivers designed at CERN
  - Bidirectional digital CMOS I/O cell with slew-rate-controlled output
    - Driving strength control: 16 or 5 mA
    - Enable-controlled pull-up/down resistors (40kohm)

# Monitoring ADC

- ADC
  - Outsourced to Sparkling IC
  - 12 bit, 32 channels, single-slope
  - Temperature range -30 C to 80 C
  - Sampling rate 1 kS/s
  - power <500uW
  - input max slew rate 1 V/s
  - Wishbone digital interface (commands and I/O via registers)
- Digital logic implemented at CERN
- Test chip back from fabrication
  - Test board design in progress

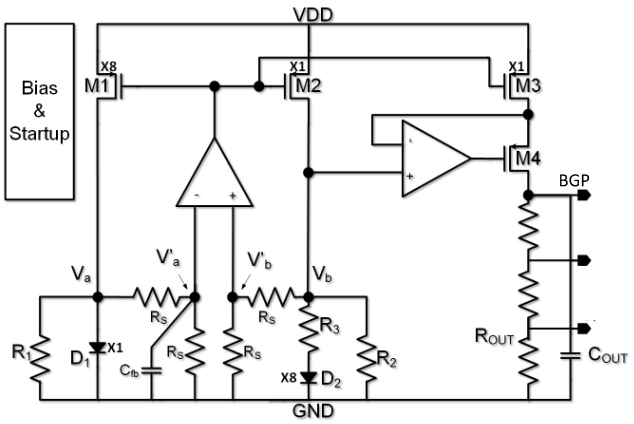
| Parameter | Value | | |
|---|---|---|---|
| # of channels | 32 | | |
| Resolution | 12 bits | | |
| Input Range | 0V ÷ 800 mV | | |
| Quantization Error (max) | < 1.5 LSB | | |
| Noise $_{0.1Hz \div 1GHz}$ | **Input** | **Ramp** | **Comp** |
| | 117 µV | 145 µV | 138 µV |
| Power Consumption (max) (Analog Only) | ≈ 400 µW | | |
| Conversion Time (max) | ≈ 430 µs | | |
| Supply Voltage | 1.2V ± 10% | | |
| Area | 0.163 mm$^2$ (analog part only) | | |



| IP Block name: | CERN Bandgap V1 diode |
|---|---|

| Parameter | Size |
|---|---|
| Dimension | 160x520um2 |
| Bandgap voltage | 330mV |
| Required supply voltage | 1.08-1.32V |
| Power consumption | 200uW |
| Temperature range optimization | -20C +50C |
| Max variation (process, T, mismatch, corners) | 3.2% |
| Min PSRR | -20dB @100KHz |
| Capacitor used | Momcap (for compatibility with all possible metal stacks) |
| Active element used | Diode between bulk and source of an ELT Pmos (to have gate oxide around the diode instead of STI) |
| Designers | Tommaso Vergine, Stefano Michelis |
| Status | Back from fabrication, test will follow |
| Schedule | Submission in September-October with Pavia/Bergamo and CPPM bandgaps |

## Block Diagram

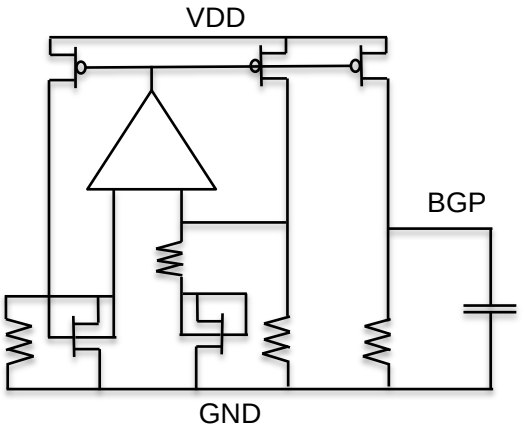



| I/O signals | Function |
|---|---|
| BGP | Bandgap output |
| VDD | Supply voltage |
| GND | Ground |

| IP Block name: | CERN Bandgap V2 DTNMOS |
|---|---|

| Parameter | Size |
|---|---|
| Dimension | layout to be done |
| Bandgap voltage | 300mV |
| Required supply voltage | 1.08-1.32V |
| Power consumption | 50uW |
| Temperature range optimization | -20C +50C |
| Max variation (process, T, mismatch, corners) | 6-8% (models to be trusted?) |
| Min PSRR | -30dB @1MHz |
| Capacitor used | Momcap (for compatibility with all possible metal stacks) |
| Active element used | DTNMOS (NMOS biased in weak inversion to have the exponential behavior of diode) |
| Designers | Tommaso Vergine, Stefano Michelis |
| Status | Back from fabrication, test will follow |
| Schedule | Submission in September-October with Pavia/Bergamo and CPPM bandgaps |

## Block Diagram




| I/O signals | Function |
|---|---|
| BGP | Bandgap output |
| VDD | Supply voltage |
| GND | Ground |


Thank You


# Backup Slides

# Foundry IP library

- Foundry provides a wide range of IP blocks
  - Electrical fuse blocks / NVM
  - PLLs
    - 100MHz – 1600MHz
    - Jitter enhancement
  - Specialty I/O
    - USB 2.0 / UTMI+
    - DDR2 (up to 800Mpbs), DDR1 (up to 533 Mbps)
    - Crystal oscillator, 32kHz
  - ROM compiler
  - Register File compiler
    - Single- and dual-port
  - SRAM compiler
    - Single-port and dual-port
    - Low-power and low-leakage
- Not made / not tested for radiation performance

# Soft IP blocks

- I2C slave
  - 7- and 10-bit addressing
- HDLC communication protocol
  - Variable bit-rate
  - Average 7% bandwidth overhead
- 7b8b communication protocol
  - DC balanced
  - Fixed latency
  - Control characters available