AIDA
Advanced European Infrastructures for Detectors at Accelerators
EU-FP7 Grant Agreement 262025

D 9.7: Infrastructure for highly granular calorimeters

Roman Pöschl

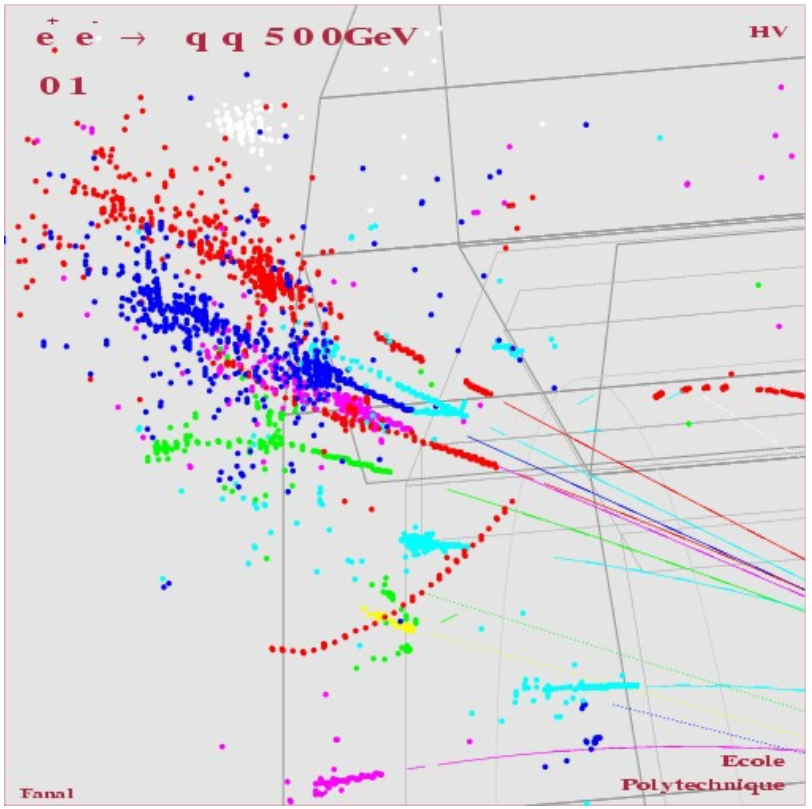
AIDA Final Meeting – CERN December 2014

Motivation for granular calorimeters

- Reconstruct jet energy on the basis of the measurement of individual particles

Particle Flow

- Base measurement as much as possible on measurement of charged particles in tracking devices
- Separate of signals by charged and neutral particles in calorimeter



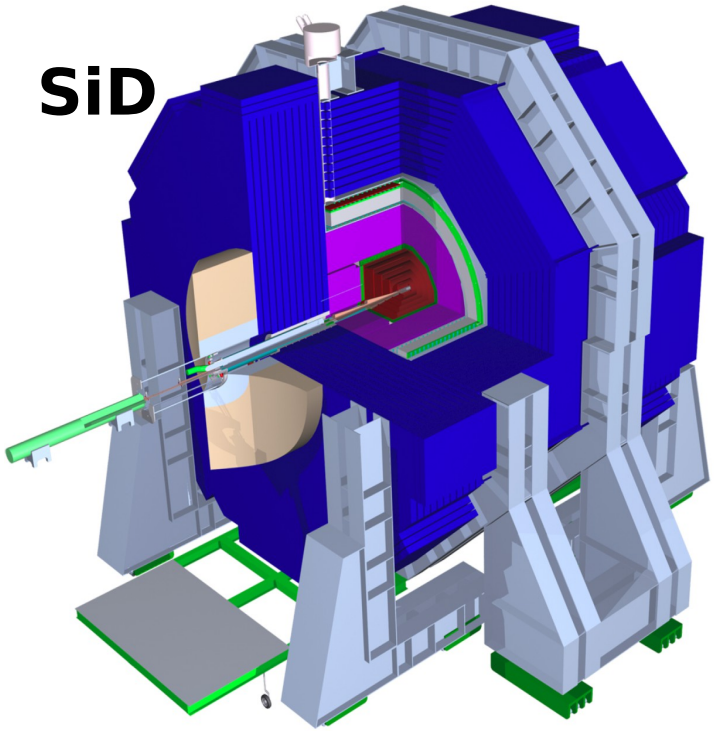
- Complicated topology by (hadronic) showers

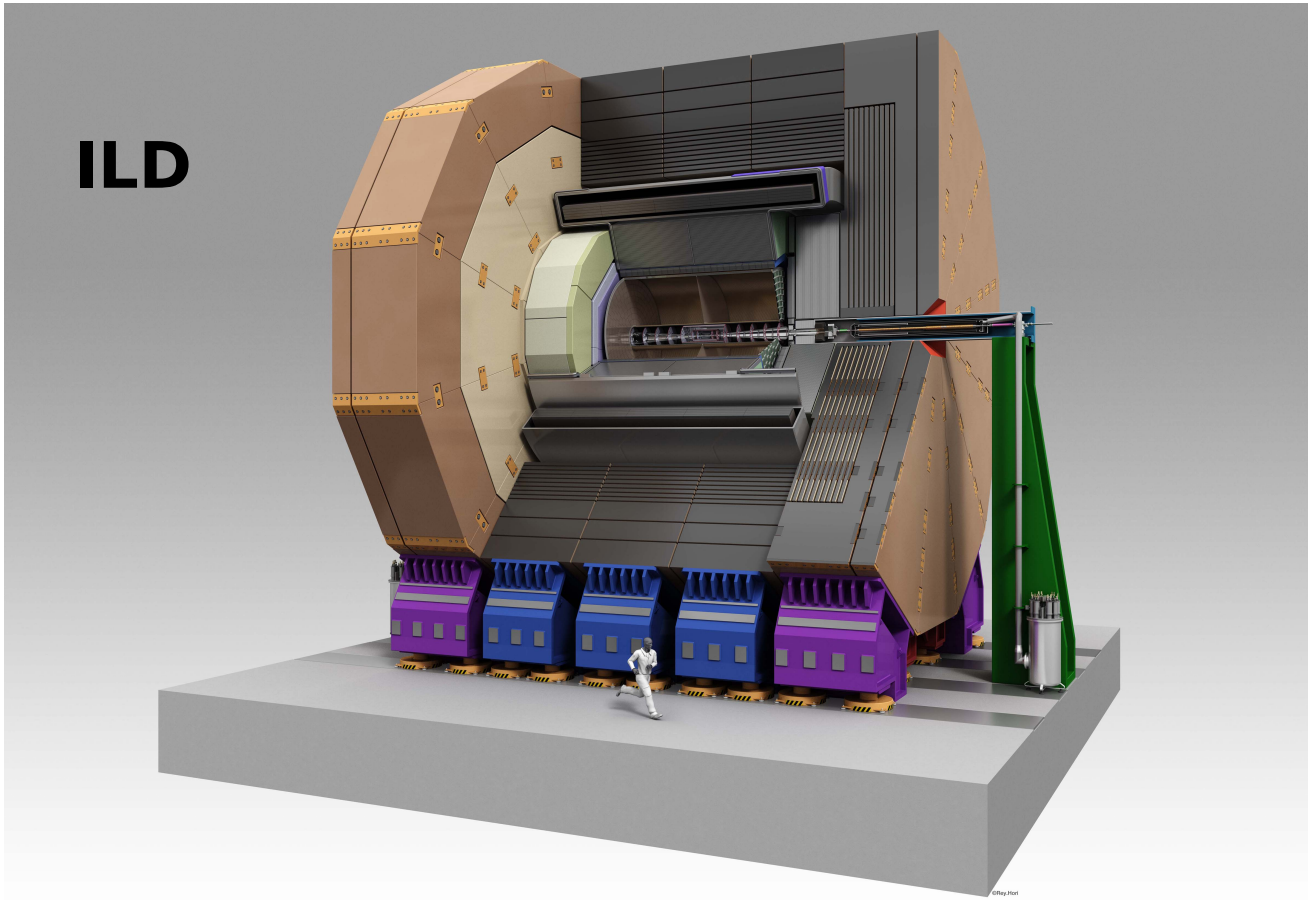
- Overlap between showers compromises correct assignment of calo hits

 Confusion Term

Control of confusion term by highly pixelised calorimeters

Concepts for LC Detectors





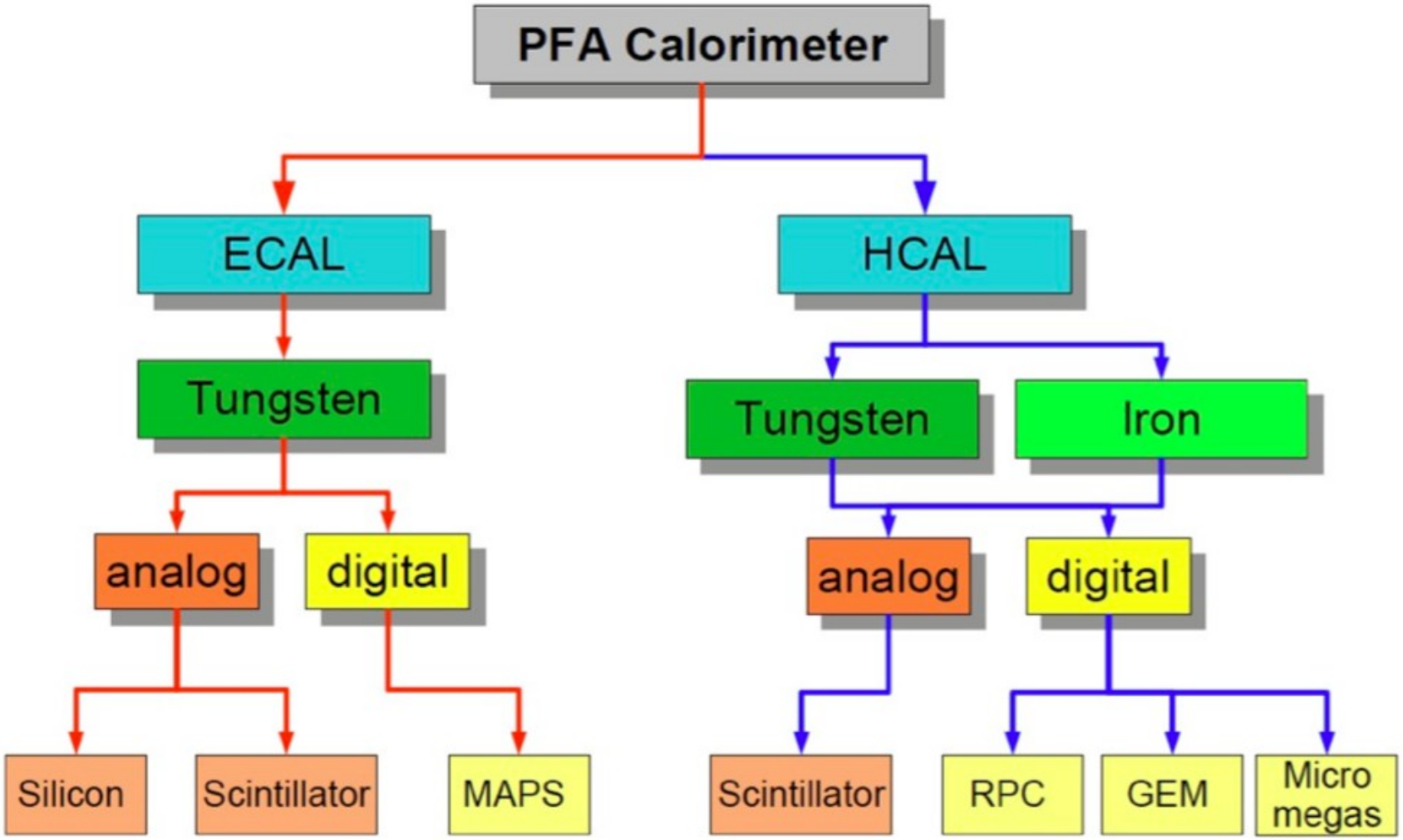
Highly granular calorimeters

Central tracking with silicon

Central tracking with TPC

Inner tracking with silicon

Technologies for PFA Calorimeters



Most technologies developed/supported within/by AIDA

Granular Calorimeters in AIDA - Partners

- CERN
- UCL - Louvin
- IPASCR - Prague
- CNRS
  - IPNL Lyon
  - LAL Orsay
  - LAPP Annecy
  - LLR Palaiseau
  - LPC Clermont-Ferrand
  - LPSC Grenoble
  - LPNHE Paris
- DESY
  - third party no funds: UHEI
- MPG-MPP Munich
- Wuppertal
- TAU Tel Aviv
- UIB Bergen
- AGHUST Cracow
- IFJPAN Cracow

Granular Calorimeters in AIDA - Milestones

- MS 42 Gas system, control and bench structure
  - Due month 24 (Jan. 2013)
- MS 43 3rd generation fast read out chips
  - Due month 30 (July 2013)
- MS 44 Multilayer tungsten structure with position control and monitoring for forward calorimeters
  - Due month 30 (July2013)
- MS 45 Calibration and power supply system
  - Due month 36 (Jan 2014)
- MS 46 Electromagnetic calorimeter of at least 18x18cm2 Area
  - Due month 36 (Jan 2014)
- Multichannel readout ASICs for luminosity detector
  - Due month 40 (May 2014)

Granular Calorimeters – Common read out ASICs

2011-2012: Characterization of the 2nd generation ROC Chips

- Dedicated run produced in March 2010
  - 25 wafers received in June
  - 20 000 chips packaged in the US

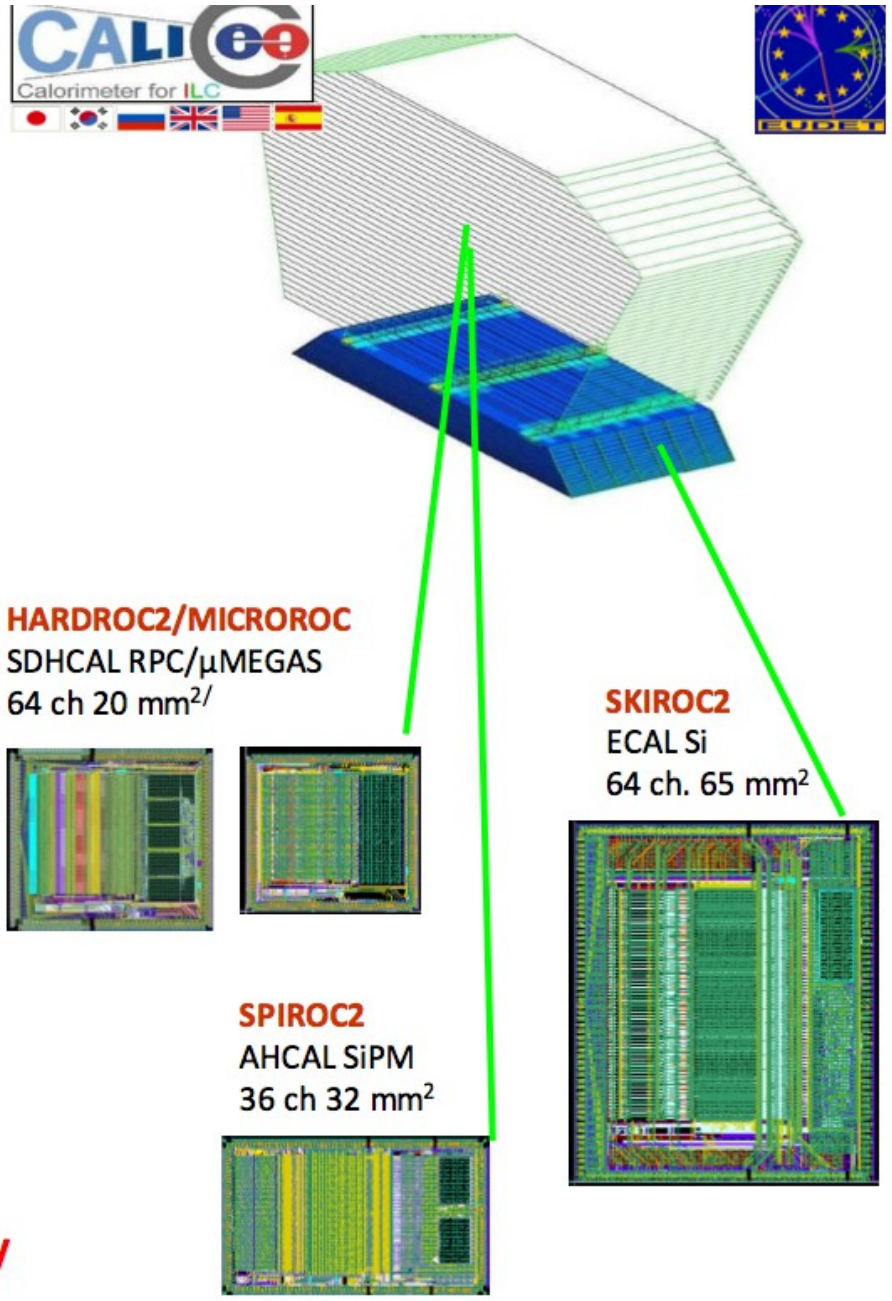
2013: AIDA Milestone = Submission and test of one of the 3rd generation chips (hradroc3)

- Report submitted in August 2013

End of 2014: Engineering run

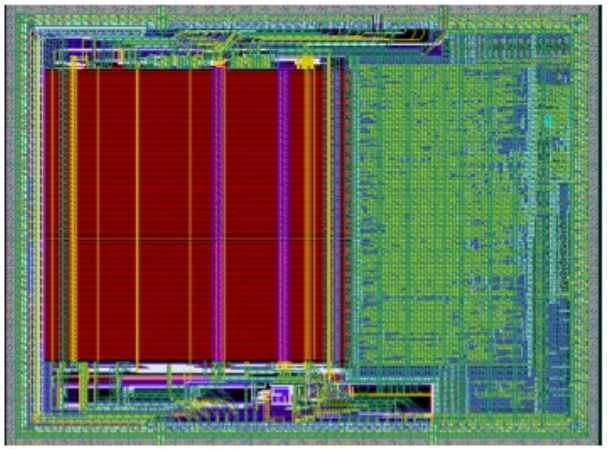
- Budget for 3rd generation of electronics:
  - 81k€ (40k spent so far)
  - 30 ppm (19 ppm used so far)
- Cost:
  - Multi Project runs (MPW): 1k€/mm2
  - Packaging: $3500
  - Testboard: 1500 €

0.35µm SiGe AMS technology



HARDROC3

- **3rd generation chip for ILD**
  - **Independent channels (zero suppress)**
  - **I2C link (@IPNL)** for Slow Control parameters and **triple voting**



- HARDROC3: 1st of the 3rd generation chip to be submitted
  - analog part: extension of the dynamic
  - Complex digital part to handle the channels independently
  - Submitted in Feb 2013 (SiGe 0.35µm), funded by AIDA, received end of June 2013
  - Die size ~30 mm^2 (6.3 x 4.7 mm^2)
  - Packaged in a QFP208
  - HR3: tests at system level should be performed on 2-3m chambers

Production run end of 2014

- MAROC3A
- MAROC4
- HARDROC3B
- SPIROC2D

Technology :

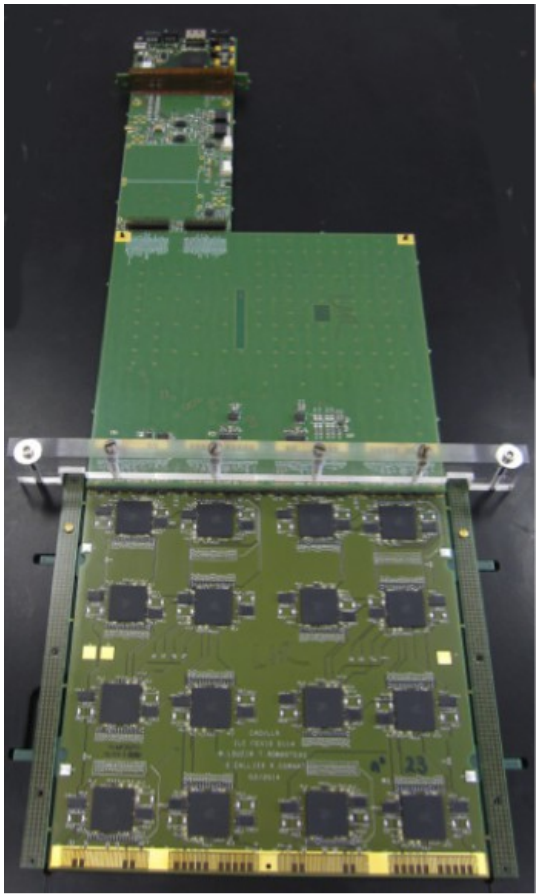
0.35µm SiGe

- PARISROC3
- PETIROC2A
- SPACIROC3A
- CITIROC1A
- CITIROC1B
- (EASIROC2)
- DOSIROC1A
- DOPIROC1B
- TRIROC2

- Production Run 2010
  - EASIROC
  - HARDROC3B
  - MAROC3
  - SKIROC2B
  - SPACIROC
  - SPIROC2A
  - SPIROC2B

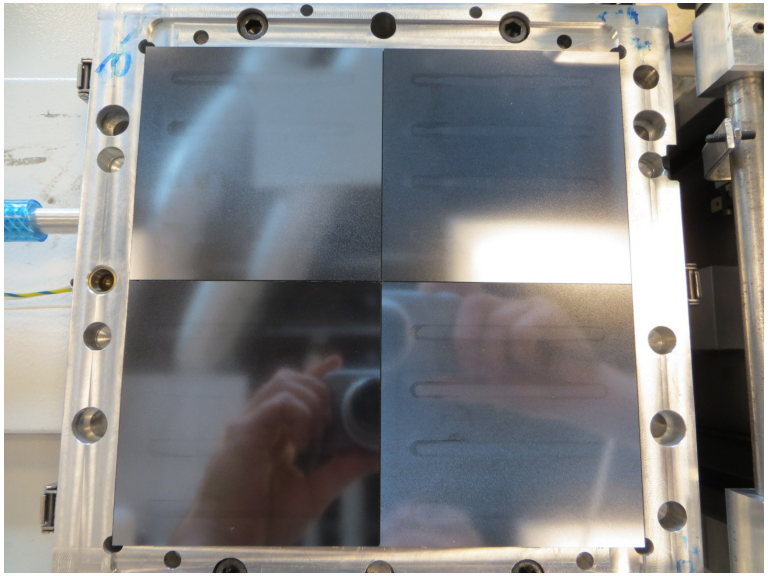
SiW Ecal - Towards detector with 18x18 cm^2 surface

Development of PCBs with 16 ASICs



PCBs are at hand

Wafer gluing – Critical operation!



- Issues
  - → Size of glue dots
  - → Relative size of wafer and PCB
  - → Mechanical properties of PCB
  - → False Si wafers (IEF Orsay) to examine procedure under 'real' conditions

Plan to produce first layers in January 2015
-> Did miss the AIDA deadline (MS 46) but production is imminent

SiW Ecal - Sensors

The simplest design to control the cost

- Glued on PCB : Floating Guard Rings
- Reasonable cost trends

R&D in close collaboration with HPK

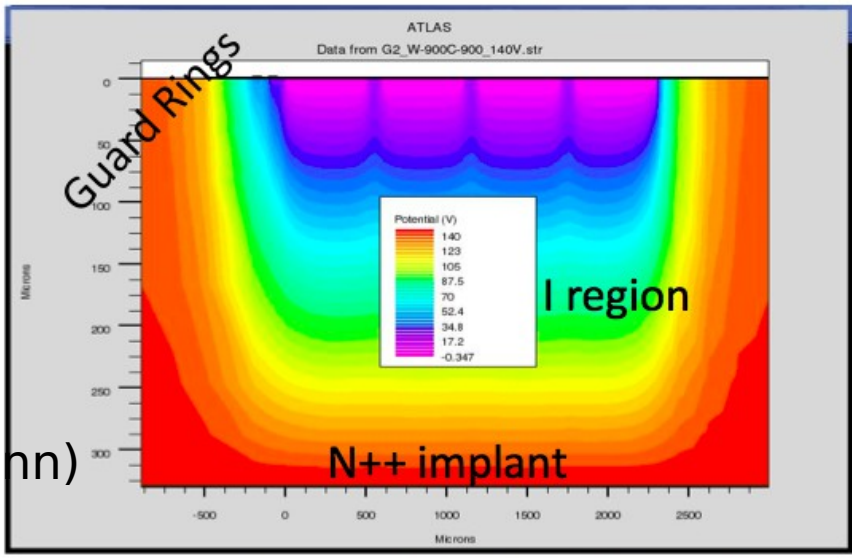
- Split GR and/or complete removal of GR
- Laser dicing : gain a factor 2 on dead zone

R&D with LFoundry (first contact through Uni Bonn)

- 8 inches wafers : width >12 cm

Also tried edgeless techno. from VTT

P++ implants (pixels)

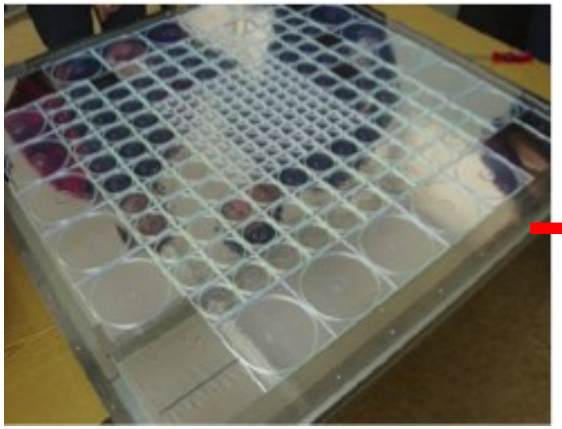


Large matrices, reduced dead zone ✓
Crosstalk ✓
Optimization (dimensions) ✘
Mass production & automated tests ✘

R&D for hadronic calorimeters – Large scale prototypes

~1m^3 absorber structure

Scintillating tiles



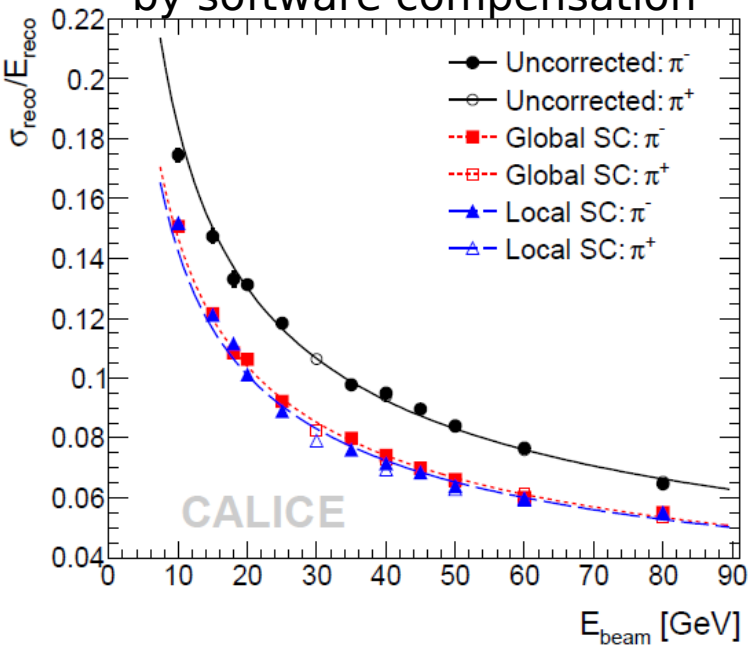
... with SiPM r/o

Steel or Tungsten

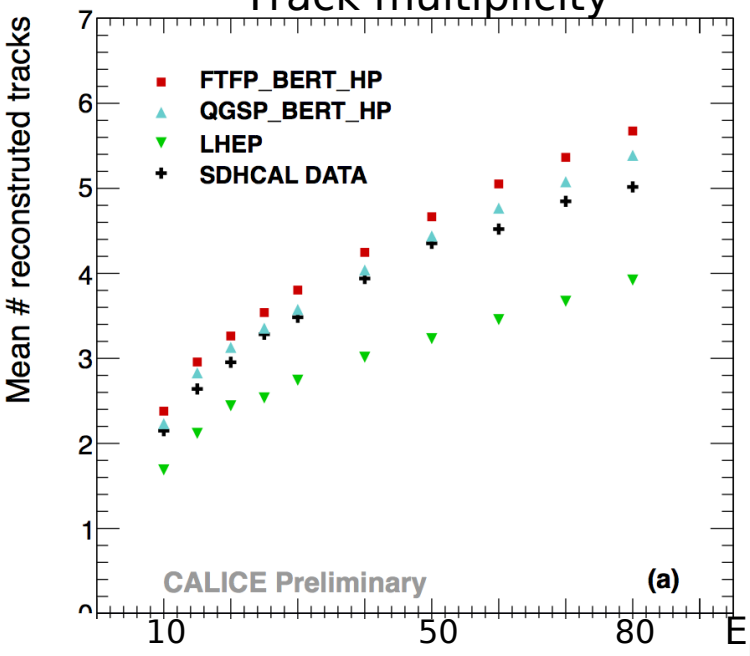
Glass RPCs/Micromegas

... with semi-digital r/o

Excellent hadronic energy resolution
by software compensation



Shower substructure
Track multiplicity



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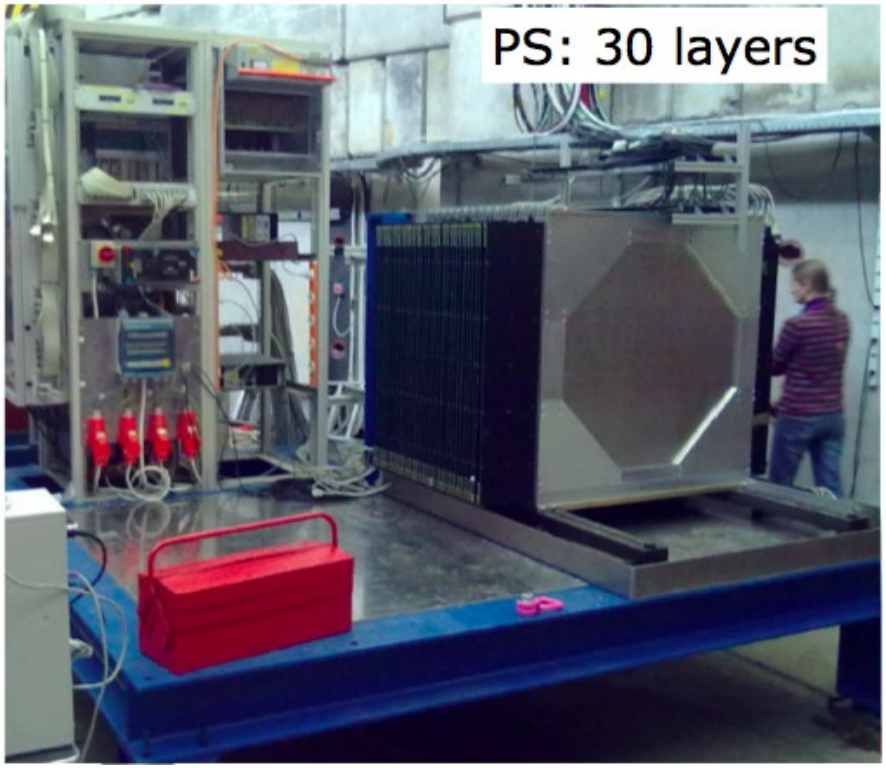
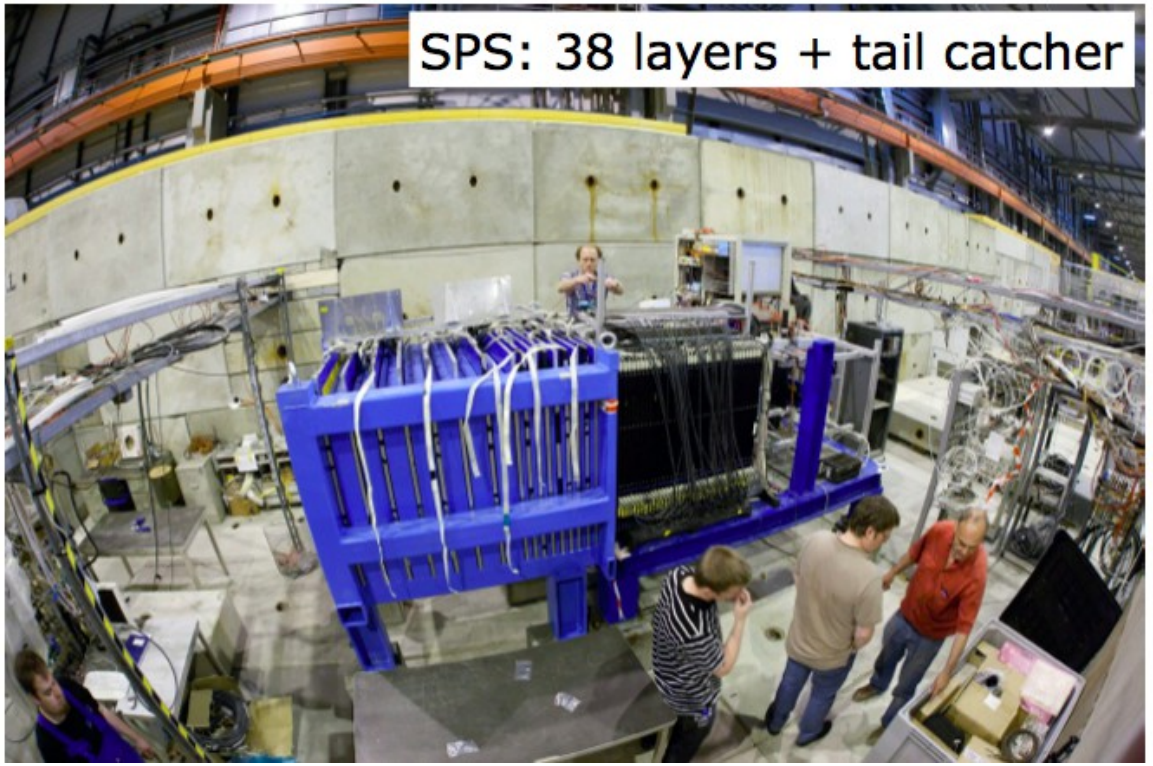
Tungsten absorber infrastructure (MS 44)

- 2010: PS, 1 - 10 GeV Published results
- 2011: SPS, 10 - 300 GeV
- 2012: gaseous DHCAL
- T3B: Fast timing Published results

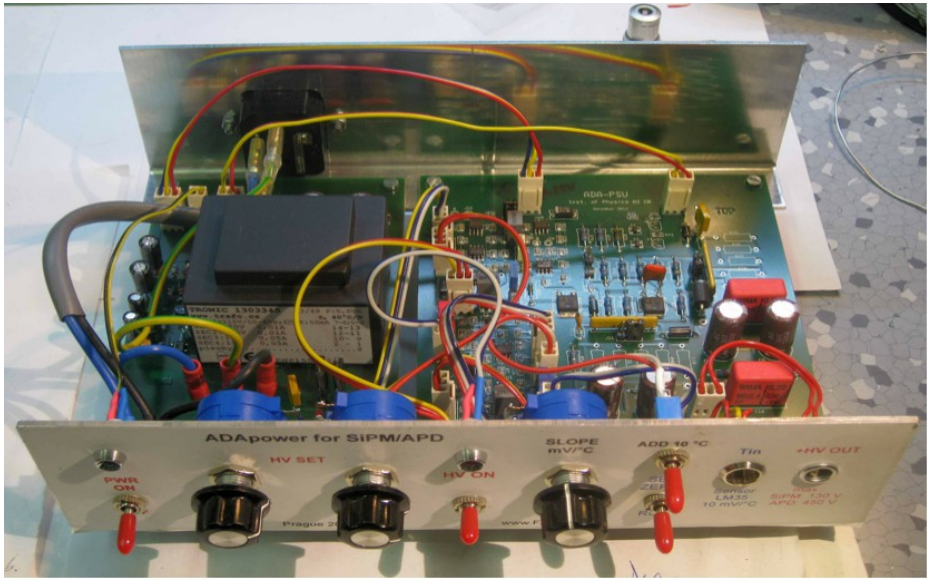




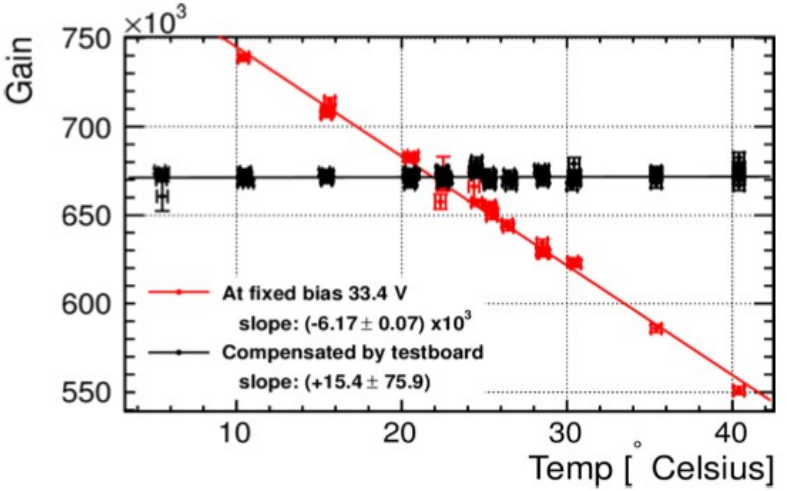
HV Control and monitoring system for AHCAL prototype

"ILD like" absorber structure with up to 14 layers of different size

HV system for future use with AHCAL setup



Adaptive power supply - Test bench results



Infrastructure for versatile R&D programme I

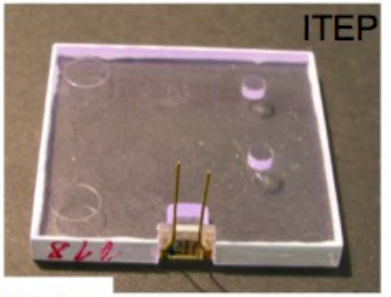
AHCAL Prototypes = Testbed for optical r/o technologies

Existing infrastructure allows for

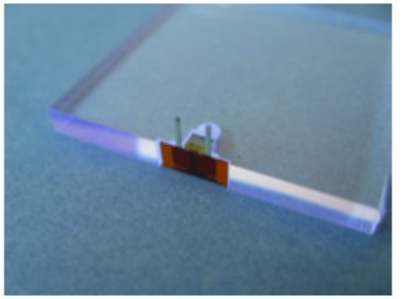
- Testing new kinds of SiPMs
  e.g. with 12k pixels

- Testing several types of
  scintillating tiles
  * With and w/o wavelength
  shifting fibres
  * Different proposals to
  place SiPMs

d



12k px SiPMs



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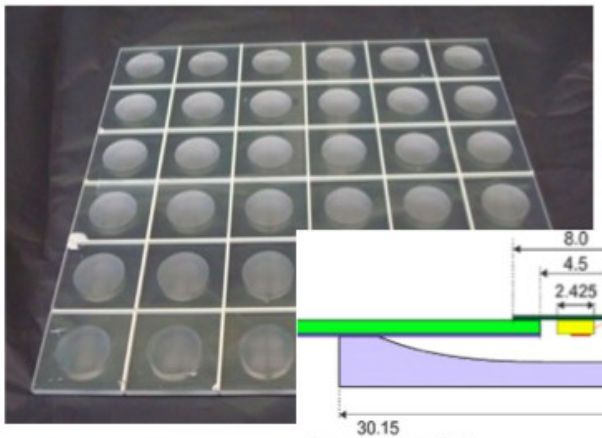
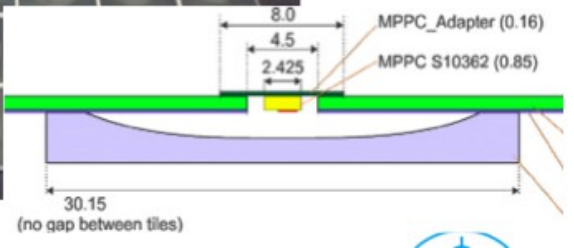




Infrastructure for versatile R&D programme II

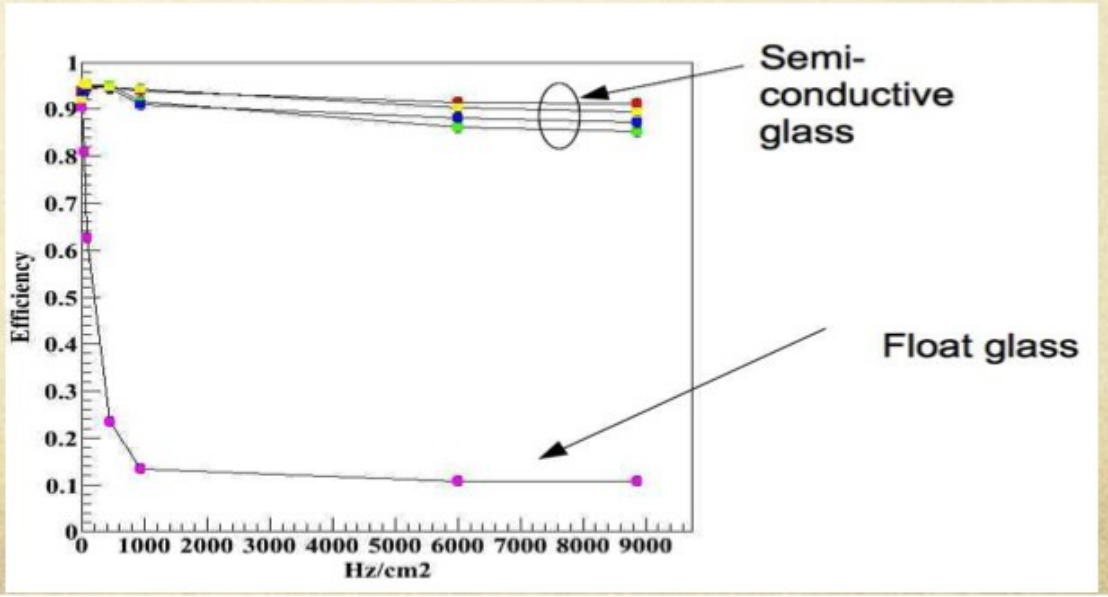
High-Rate GRPC

High-Rate GRPC may be needed in the very forward region

✓Semi-conductive glass (10^{10} Ω.cm) produced by our collaborators from Tsinghua University was used to build few chambers.
✓4 chambers were tested at DESY as well as standard GRPC (float glass)

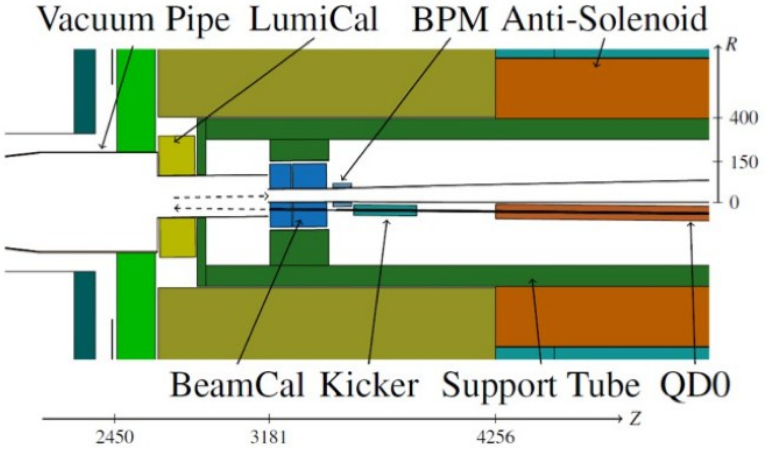
Performance is found to be excellent at high rate for GRPCs with the semi-conductive glass and can be used in the very forward of ILD region if the rate exceeds 100 Hz/cm² in future ILD upgrades as well as for CLIC

It has been also proposed for the CMS muon system upgrade

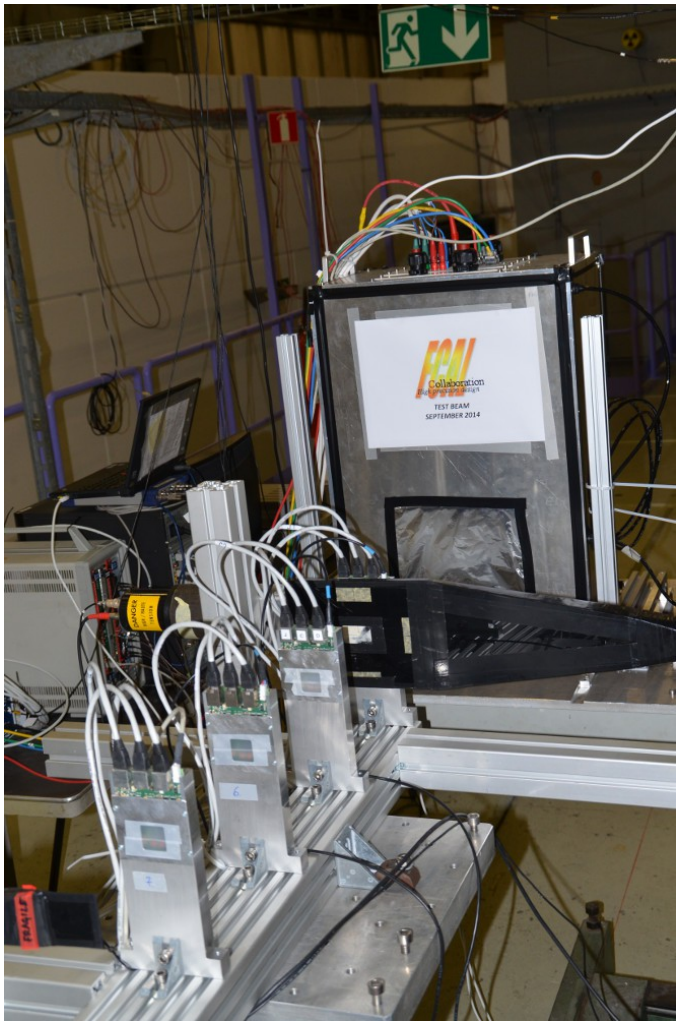


AIDA 3rd Annual Meeting, Vienna March 2014

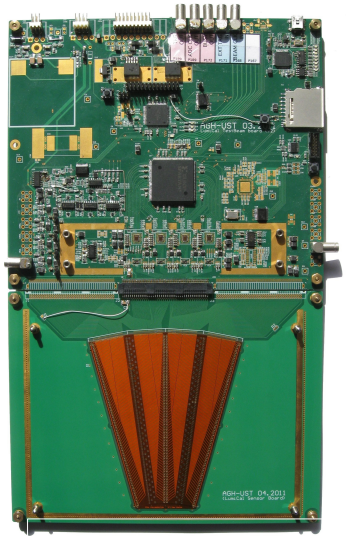
Calorimetrv for luminosity measurement



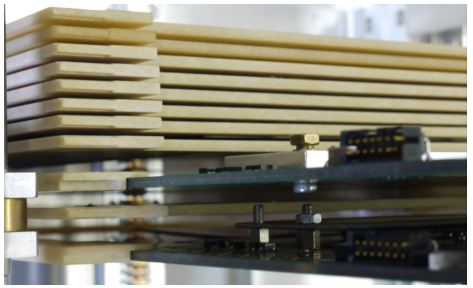
Multilayer LumiCal structure
in beam test

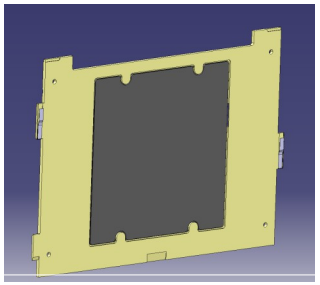


Detector modules for LumiCal and BeamCal



Tungsten plates





Detector modules + Tungsten plates + Mechanical frame were developed and the multilayer LumiCal structure was built

Front end electronics have to meet special requirement in forward region -> Next slide

Multichannel readout ASIC for Luminosity detector

Design specs:

8 channels in 130nm technology

Cdet ≈ 5 ÷ 35pF

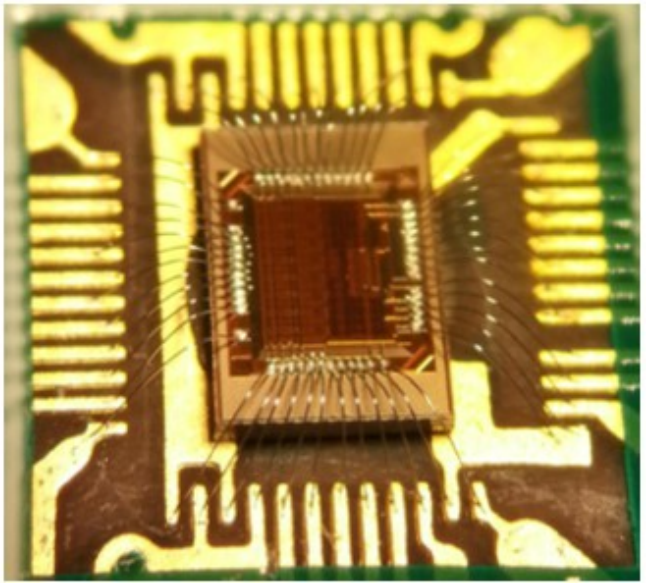
1st order shaper (Tpeak ≈ 50 ns)

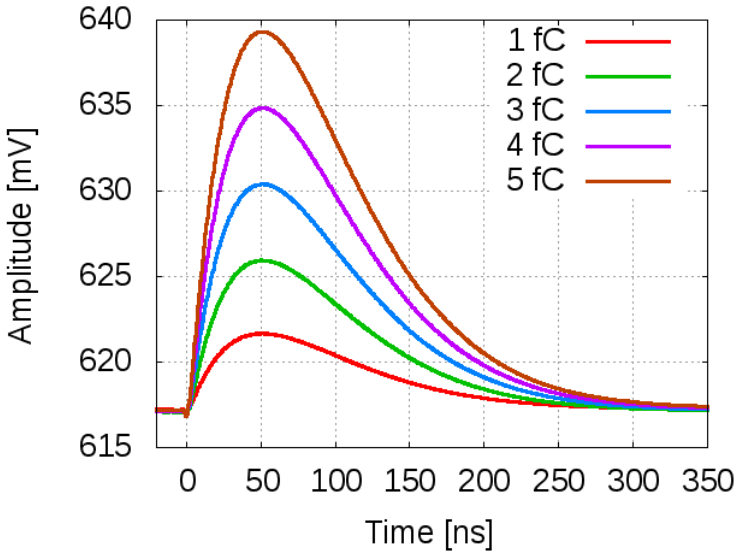
Variable gain:

- calibration mode - MIP sensitivity
- physics mode - input charge up to ~5 pC

Power pulsing implemented

Power consumption ~1.5 mW/channel





Measurements results:

Fully functional with Tpeak ≈ 50 ns

Calibration mode @10pF:

- gain 4.1 mV/fC
- linear range ~60 fC
- ENC 930 e-

Physics mode @10pF

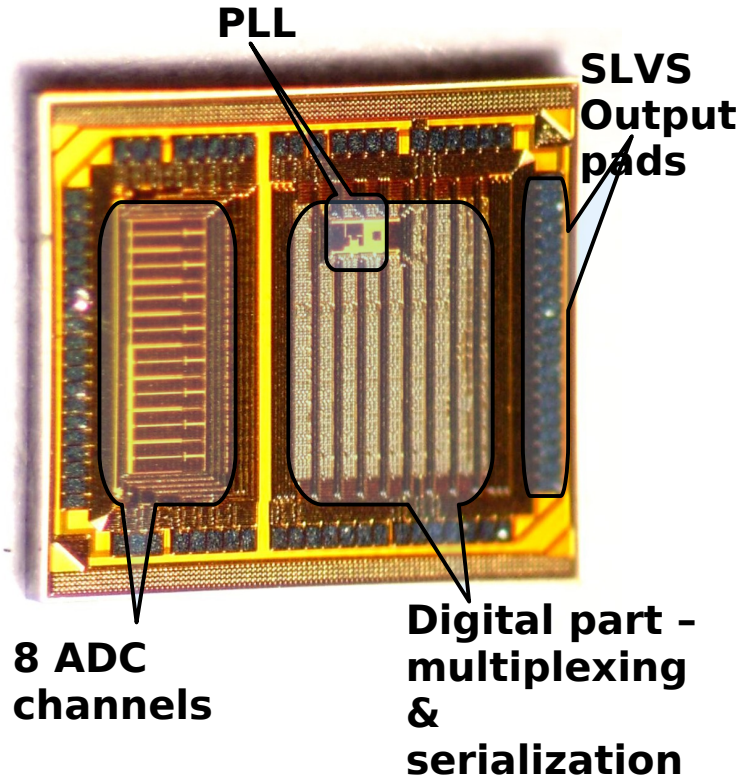
- gain 105 mV/pC
- Linear range ~2.7 pC (saturates >5pC)

8-channel front-end fabricated and succesfully tested

10-bit Multichannel SAR-ADC for Luminosity detector

Main features of single ADC

130nm techology	
Sampling frequency [Ms/s]	>40
Power cons. [mW] @40Ms/s	1
Power pulsing	Yes
Size [mm^2]	0.087 146x600mum2



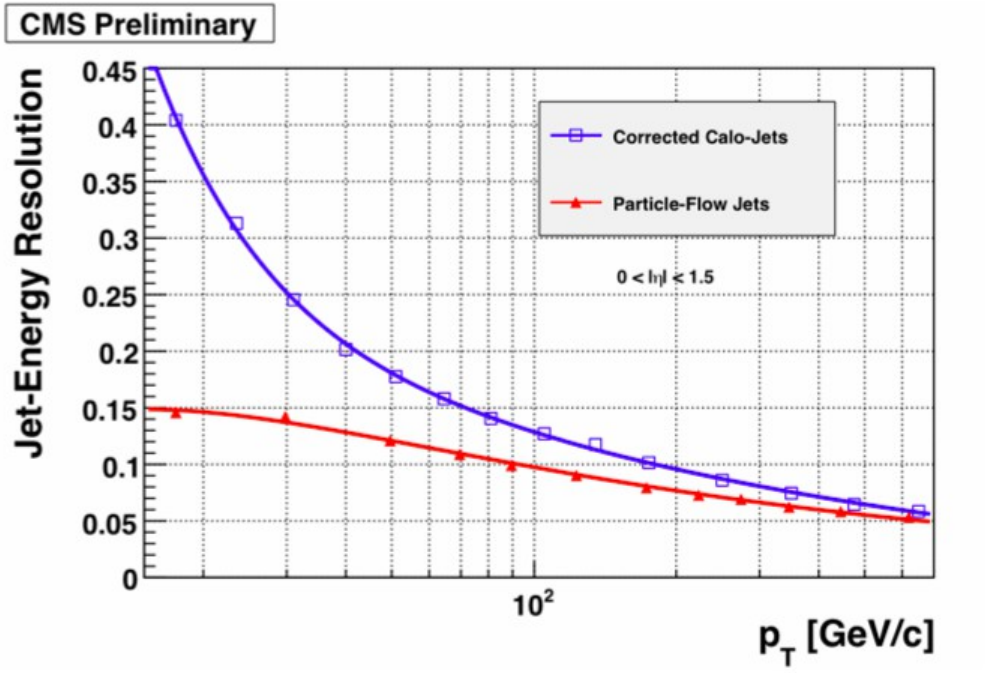
Measurements of single channel 10-bit ADC show that its performance is similar to State-of-the-Art designs

8-channel ADC was fabricated, measurements are just starting...

J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek. "Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology", TWEPP2013 23-27 September 2013, Perugia Italy

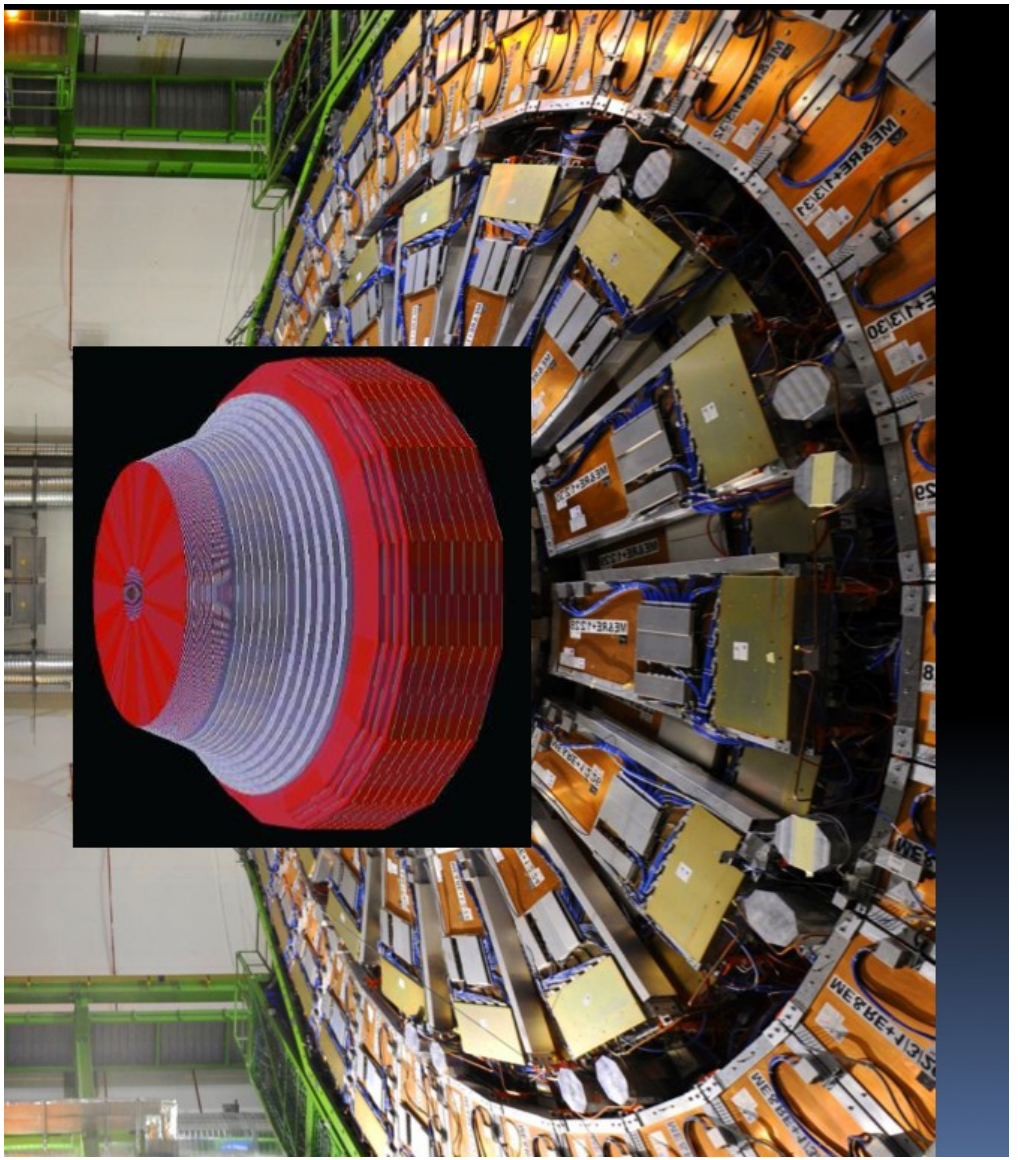
PFA outside LC activities – Example CMS

PFA idea applied in CMS



=> Significant improvement of jet energy resolution

Highly granular calorimeter for forward region in CMS



Summary and conclusion

- One step further on the way towards the realisation of highly granular calorimeters
  - Promising technology for many (all?) future calorimeter concepts at future colliders

- Various variants of this calorimeter type were built and successfully tested

=> The participating groups have created a network of detector infrastructures with different readout technologies

Milestones were reached or are imminent

Consolidation of network fostered through AIDA funding

- Infrastructures allow for testing novel technologies

- Interoperability through common readout devices, e.g. ASICs

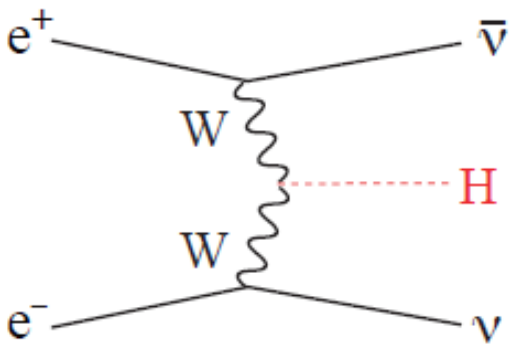
- The next steps are:
  - combined running of the prototypes
  - move from R&D phase → full detector systems

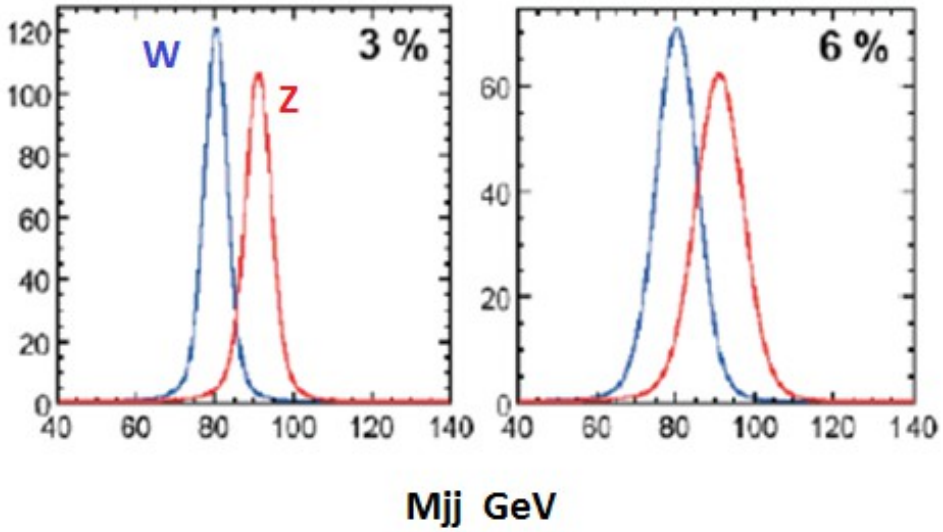
AIDA-2020

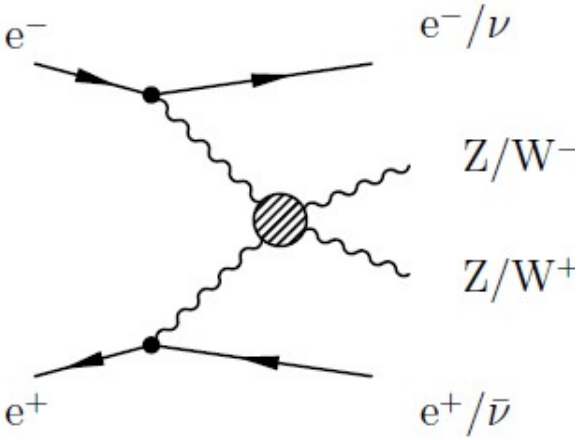
Backup slides

Examples

- W Fusion with final state neutrinos requires reconstruction of H decays into jets
- Jet energy resolution of ~3% for a clean W/Z separation







F. Richard at International Linear Collider – A worldwide event

Detector requirements of LC Detectors

Track momentum: $\sigma_{1/p} < 5 \times 10^{-5}/\text{GeV}$ (1/10 x LEP)

(e.g. Measurement of Z boson mass in Higgs Recoil)

Impact parameter: $\sigma_{d0} < [5 \oplus 10/(p[\text{GeV}]\sin^{3/2}\theta)]$ μm (1/3 x SLD)

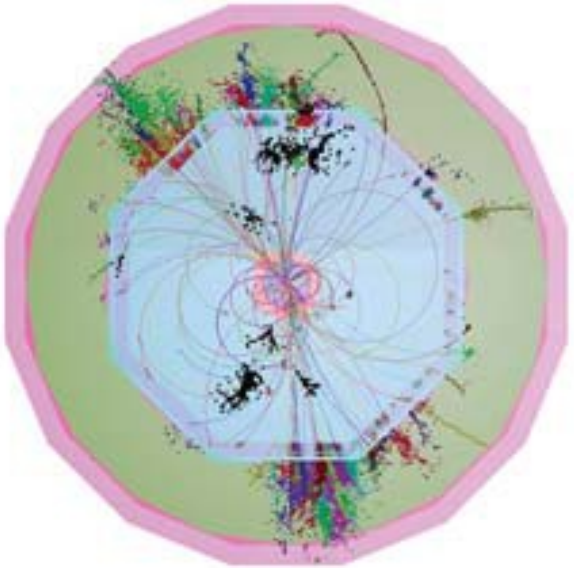
(Quark tagging c/b)

Jet energy resolution : $dE/E = 0.3/(E(\text{GeV}))^{1/2}$ (1/2 x LEP)

(W/Z masses with jets)

Hermeticity : $\theta_{min} = 5$ mrad

(for events with missing energy e.g. SUSY)



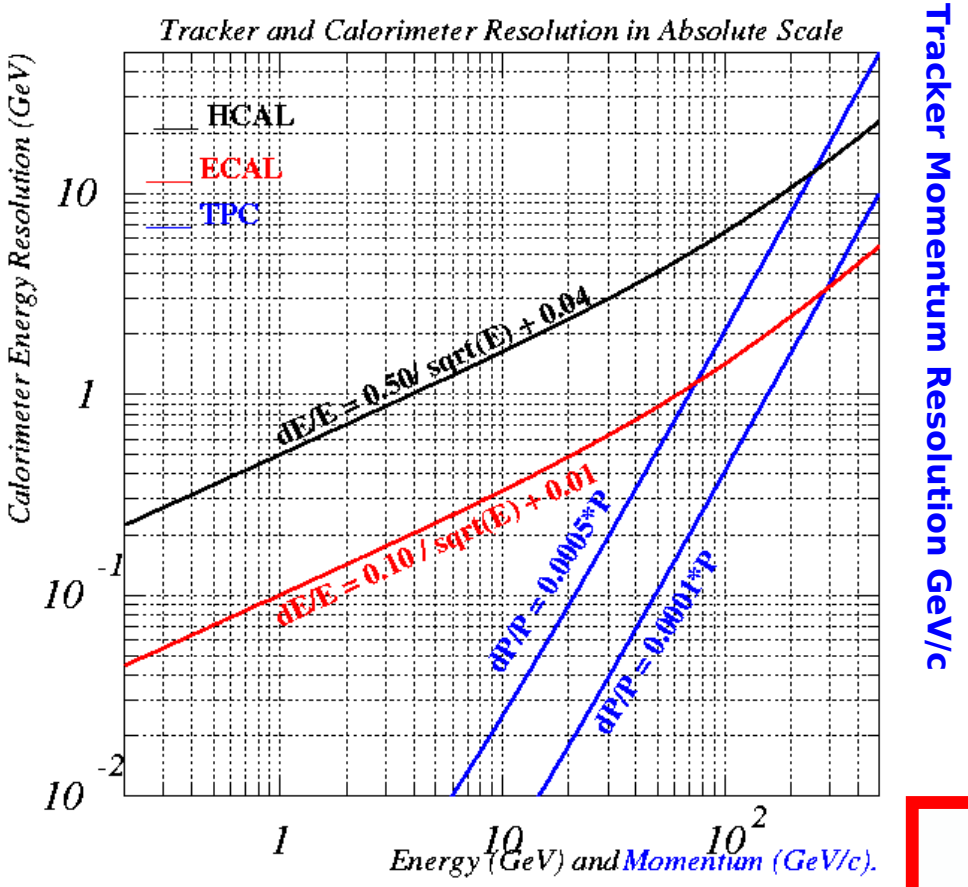
Final state will comprise events with a large number of charged tracks and jets(6+)

- High granularity
- Excellent momentum measurement
- High separation power for particles

Particle Flow Detectors

Jet energy resolution and Calorimeters

Final state contains high energetic jets from e.g. Z,W decays
Need to reconstruct the jet energy to the utmost precision !
Goal is around dE_{jet}/E_{jet} - 3-4% (e.g. 2x better than ALEPH)



Jet energy carried by …

- Charged particles ($e^{\pm}$, $h^{\pm}$,$\mu^{\pm}$65% :((
  Most precise measurement by Tracker
  Up to 100 GeV

- Photons: 25%
  Measurement by Electromagnetic Calorimeter (ECAL)

- Neutral Hadrons: 10%
  Measurement by Hadronic Calorimeter (HCAL) and ECAL

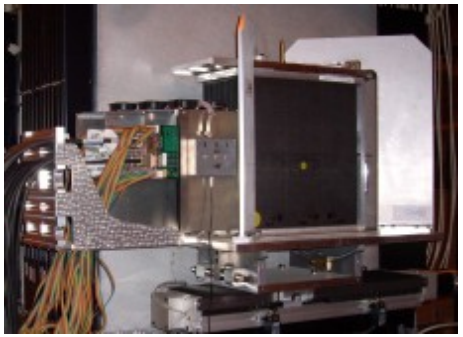
$$\sigma_{Jet} = \sqrt{\sigma^2_{Track} + \sigma^2_{Had.} + \sigma^2_{elm.} + \sigma^2_{Confusion}}$$

Example for R&D cycle – CALICE SiW Ecal

Physics Prototype

Proof of principle

2003 - 2011



Number of channels : 9720

Pixel size: 1x1 cm2

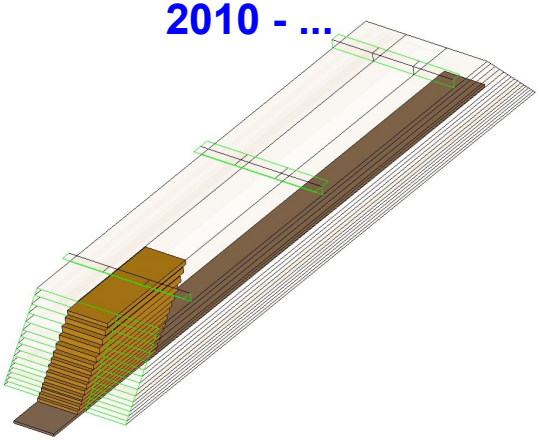
$R_{M,eff}$: ~ 1.5cm

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

2010 - ...



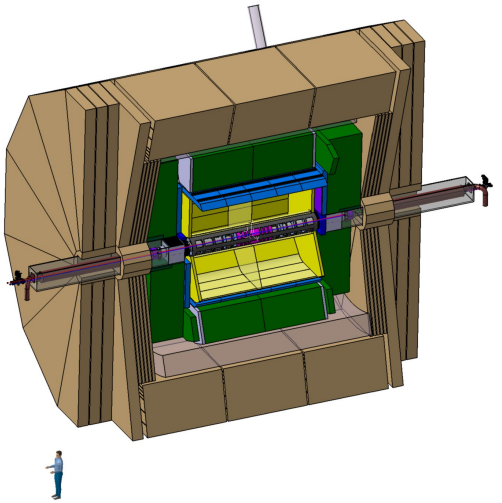
Number of channels : 45360

Pixel size: 0.55x0.55 cm2

$R_{M,eff}$: ~ 1.5cm

Weight : ~ 700 Kg

LC detector



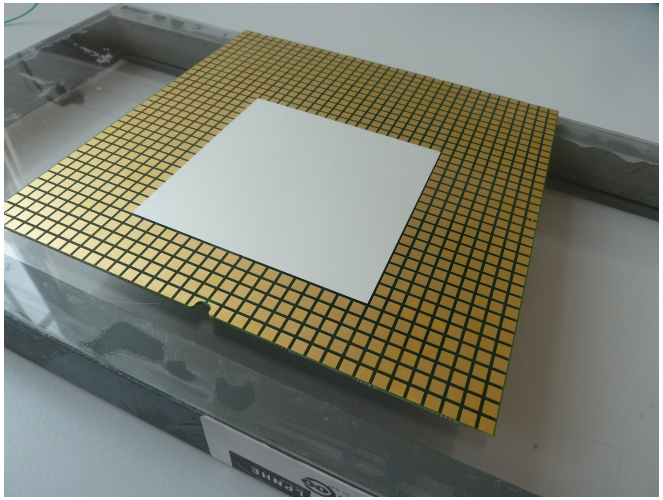
ECAL :

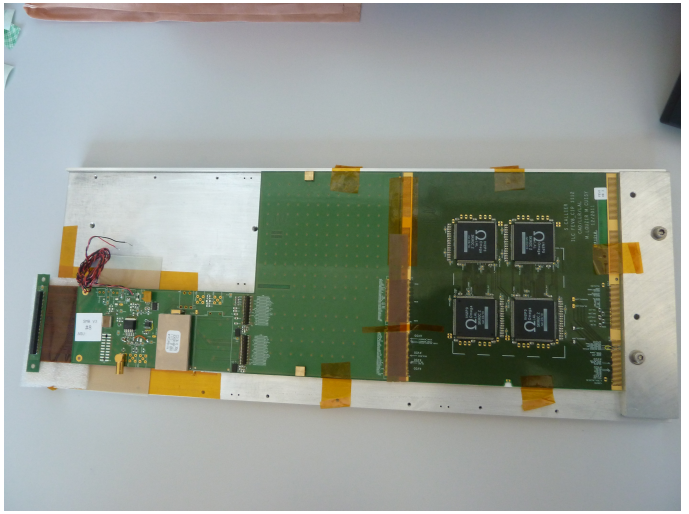
Channels : ~100 10^6

Total Weight : ~130 t

SiW Ecal 1st step - Simplified layers

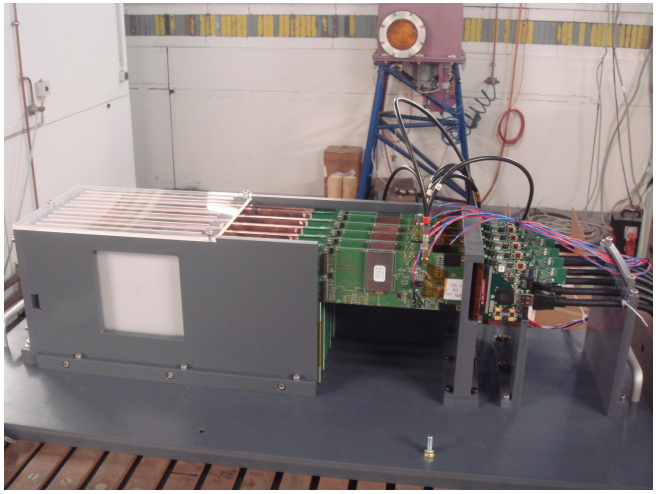
Layer design





- 1 Si Wafer with 256 pixels of 5x5 mm^2 and thickness of 325 mum
  compare with 4 wafers for final design
- Wafer glued onto PCB
  EPOTEK-4110, development of automatised procedure
- 4 ASICs in PQFP package
  Compare with 16 ASICs wire-bonded or in very thin BGA package

Beam test setup @ DESY (Supported by AIDA TA)



Up to 10 layers with
total number of active channels = 1278

- Test program
  - 2012: Commissioning
    - Test of front end electronics
  - 2013 Test of power pulsing, Tests in magnetic field

Tests with simplified layers gave confidence to go ahead

Examples for detector R&D collaborations

Time Projection Chamber
for Linear Collider

Highly granular calorimeters
for Linear Collider

Forward calorimeters
for Linear Collider

Silicon tracking for the
International
Linear
Collider

PLUME

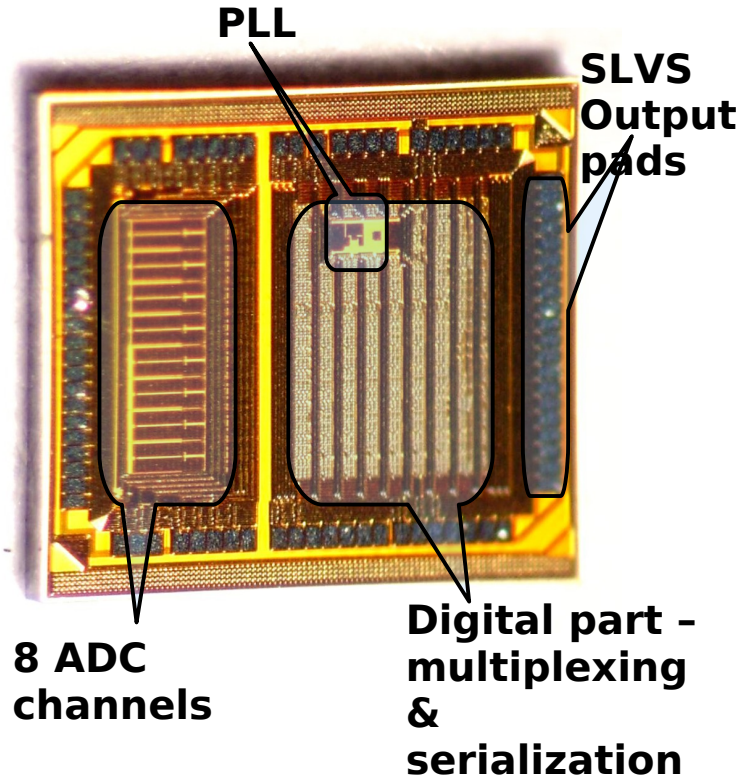
- Oriented towards LC but very generic R&D

R&D RPCs, Micromegas, SiPMs, ultrathin vertex layers, diamond sensors
Large scale integration of electronics, small power consumption

10-bit Multichannel SAR-ADC for Luminosity detector

Main features of single ADC

130nm techology	
Sampling frequency [Ms/s]	>40
Power cons. [mW] @40Ms/s	1
Power pulsing	Yes
Size [mm^2]	0.087
	146x600mum2
DNL/INL [LSB]	<=1.0
SINAD@40MS/s[dB]	>56
ENOB[bits]	9.3 (up to 20MHz)
FOM [fJ/conv]	~50



Measurements of single channel 10-bit ADC show that its performance is similar to State-of-the-Art designs

8-channel ADC was fabricated, measurements are just starting...

J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek. "Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology", TWEPP2013 23-27 September 2013, Perugia Italy