Vertical integration technologies for pixel detectors

INFN/IPHC-IRFU Project

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On behalf of the PICSEL team IPHC- Strasbourg

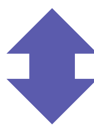
PART 1

Vertical interconnection of **dual-layer CMOS** readout circuit **to a sensing layer**

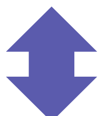
Project description

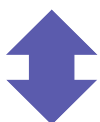
- **Design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a dual-tier readout chip and of a sensing layer**

CMOS readout chip, based on a 130 nm vertically integrated process (Tezzaron/Globalfoundries)



Vertical interconnection process (μ-bumps by Tohoku-Microtec)





CMOS sensing layer

(XFAB, 350 nm, or an alternative process in 180 nm)

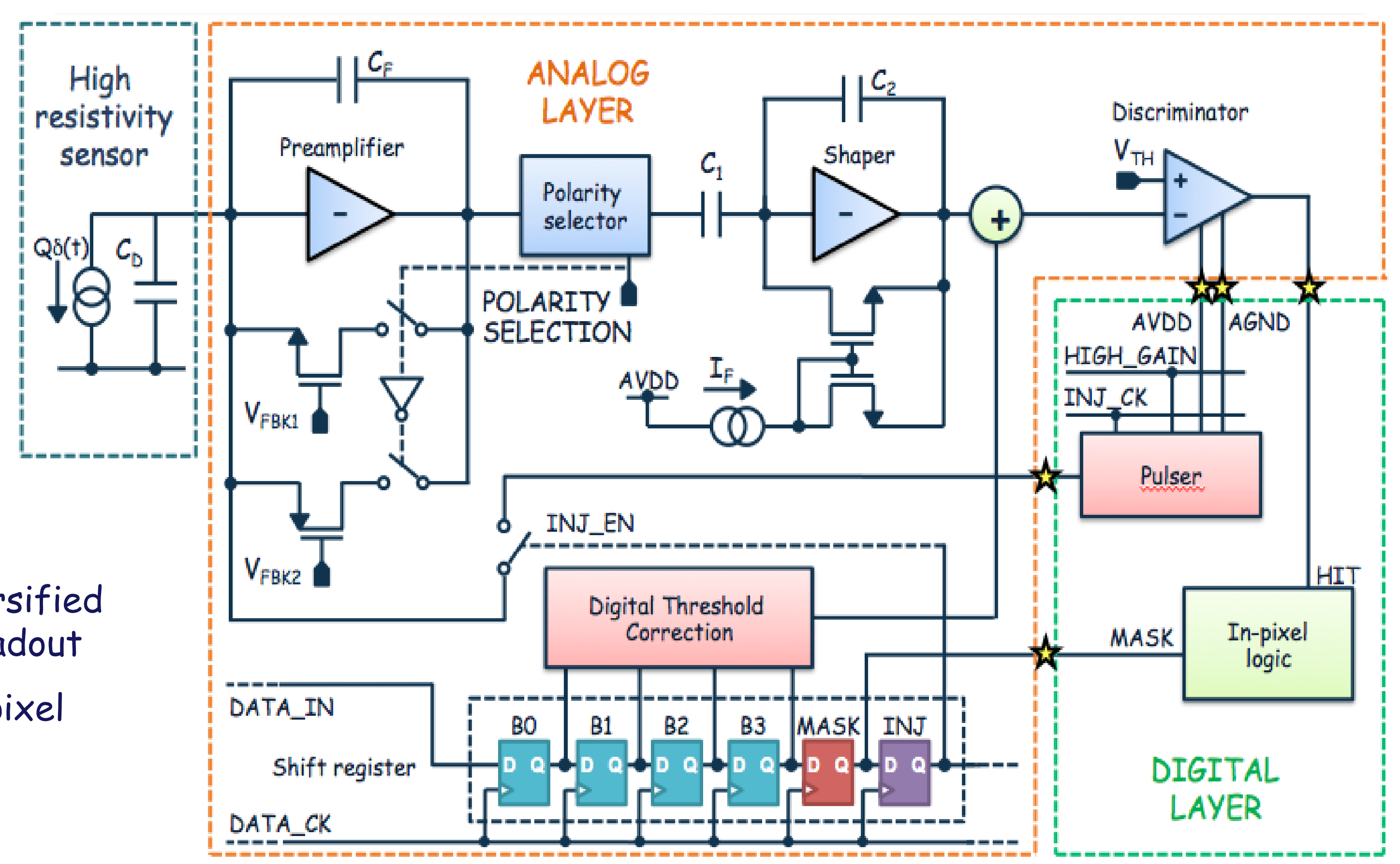
Active edge, fully depleted, planar or 3D silicon detector (from FBK, Trento)

Provided by Lodovico Ratti

Superpix1 front-end

- Design of the 128x32 array completed, including 3D LVS check
- Simulation results, including Monte Carlo and corner case simulations compliant with application to small pitch. low power pixel detectors for HEP

- 50 um pitch
- polarity selection
- pre-amplfication and shaping
- binary readout
- in-pixel threshold correction
- in-pixel logic for sparsified and time-ordered readout
- pulse generator for pixel calibration



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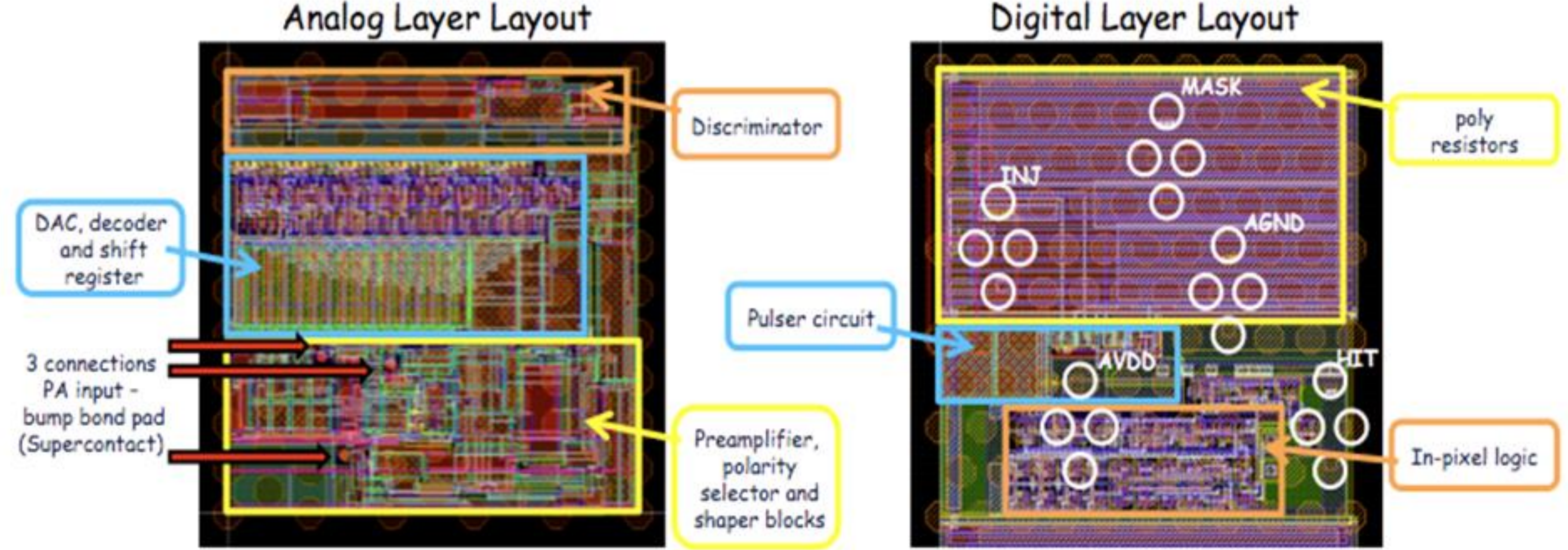
Superpix1 design features

Main front-end design features	
Analog Power Dissipation [μW/pixel]	13.5
Peaking Time (Q_{inject} = 16000 e-) [ns]	250
Charge sensitivity [mV/fC] @ DAC outPUT	48
ENC @ C_D = 150 fF [e- rms]	180
Threshold dispersion (before/after correction) [e- rms]	560/65

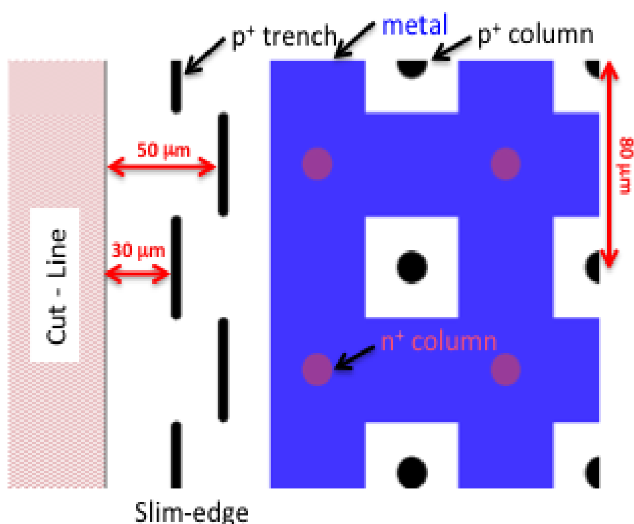


- Chip designed and ready for submission
- Due to the problems with the access to the technology chip was never fabricated

Provided by Lodovico Ratti

Fully depleted edgeless pixel sensors

- **Planar diodes** from a previous batch functionally characterized with X-rays were found to work properly up to a few um from their edge
- Edge response tested in strip sensors with a readout pitch of 50 um (compatible with pixels for AIDA WP3), also including radiation effects ($2 \times 10^{15}\ n_{eq}/cm^2$)
- Electrical tests performed on planar sensors with active edges designed at University of Trento and fabricated by FBK for 3D integration within AIDA: p-on-n batch on epitaxial layers (ALICE) and n-on-p on oxide bonded wafers (ATLAS)



Layout detail for a 3D sensor with an improved slim edge based on dashed trenches measured at 60 V bias voltage.

- Activity on **3D slim-edge sensors** mostly devoted to ATLAS IBL
- A modified slim-edge concept, based on **dashed trenches**, was used to provide a better confinement of the depletion region at the edge of the sensor
- Dashed trenches can be placed closer to the edge, therefore **reducing the dead area to a 50 μm gap**

Provided by Lodovico Ratti

PART 2
Fine pixel chip interconnections of a a **single CMOS** readout circuit **to a sensing layer**

- *Project overview - reminder*
- *Description of the sensors used*
- *Interconnection procedure and status*
- *Future work*

Reminder : Project Overview

Goal :

- **Increase signal processing functionality** of the sensor at the pixel level by introducing another processing layer

- Particularly relevant for CMOS pixel sensors because CIS processes, which provide well suited epitaxial layer parameters, have rather coarse feature size (> 0.15 µm)
  - limited number of transistors per **small** pixel

Project task :

- Establish a procedure allowing to interconnect sensors **at pixel level**, with typical pixels size of ~ 20µm × 20µm
- Procedure should be **reliable, reproducible, affordable** - to be applicable on large scale, typ. $O(10^9)$ pixels per m^2
  - industrial (adds market driven high integration evolution)

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Project deliverable features

Deliverable general features :

- 100 µm thin device composed of 2 stacked CMOS pixel sensors interconnected at pixel level
- 4 interconnections per pixel
- Both tiers have identical pixel arrays
- Only bottom tier has steering logic
- Pads concentrated on "bottom" tier
- Read-out time ~ 10 µs
- (< 25 µs in micro-tracking mode - see below)

10 µm pitch pads

Read-out => column // rolling shutter with 3 options :

- Standard read-out : top tier read out through bottom tier
  - bottom tier only used to steer and read out top tier through in-pixel connections
- Testability : bottom tier may be read out independently
- Micro-tracking : corresponding top & bottom pixel rows are read-out consecutively
  - associate top & bottom hits produced by impinging particle (e.g. from beta source)

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CMOS pixel sensors used

12 Wafers were frabricated in TowerJazz 0.18 µm CIS Engineering Run

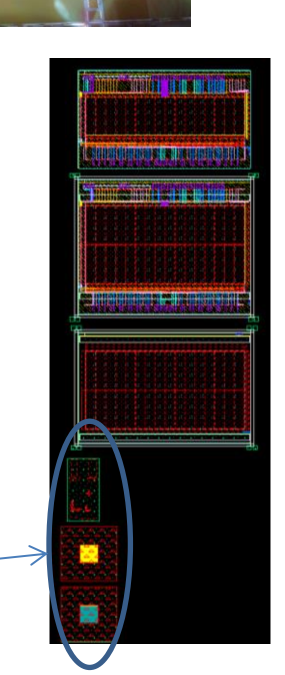
- 6 metal layers
- Quadruple well technology (in-pixel PMOS)
- High resistivity (>1kΩcm), 18 µm thick epitaxial layer

Shared run ALICE-ITS/AIDA

Photos M.Goffe

3 sensors developed

- Bottom and top sensors to be interconnected
- Half sensor for reference test purposes



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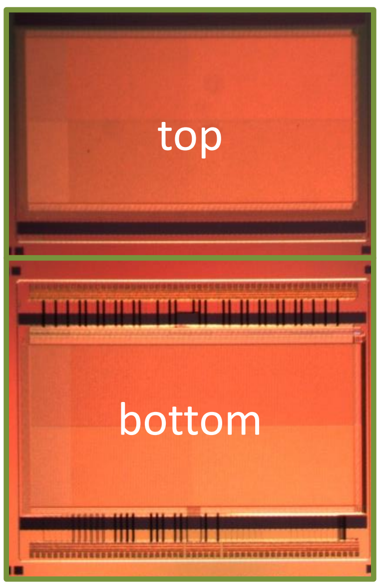
Features of the CMOS pixel sensors used

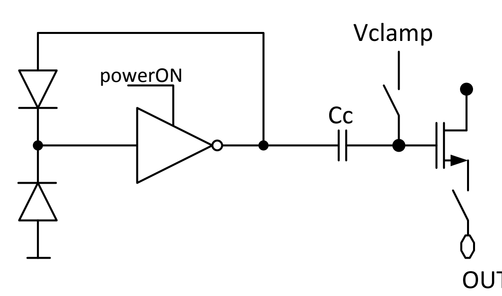
Overview of the sensors:

- Dimensions : 5.6 × 4.5 mm^2 (bottom) & 5.6×3.8 mm^2 (top)
- Pixel array of 32k pixels – 32 sub-arrays of 16x64 pixels
- Separate test chip (5.6×3.2 mm^2) for matrix operation verification



Pixel design:

- Pixel dimensions : 20 µm × 20 µm
- 3 types of pixels (validated with proto. fabricated in 2013)
  - 28 sub-arrays with in-pixel preamplification & CDS
    - 16 sub-arrays with P-MOS input
    - 12 sub-arrays with N-MOS input
  - 4 sub-arrays with "3T" structure (source follower)



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Wafer interconnecting IMS Fraunhofer - Duisburg

- Connection technique: Solid Liquid Inter-Diffusion (SLID)
- 5 step process:
  - Electroplating
  - Wafer thinning
  - Preparation of chip-to-wafer bonding
  - Chip-to-wafer bonding
  - Dicing of the chip stack

  Process duration: 5-6 months
- 6 wafers sent to IMS (+1)

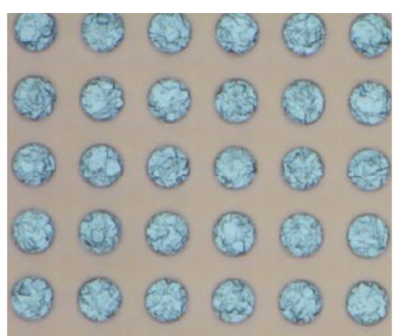
Project started **09.05.2014** due to the difficulties with the IMS Fraunhofer administration -> **no flexibility** (project almost got cancelled)

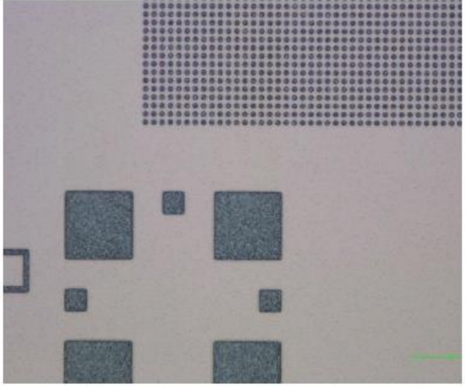
Wafer interconnecting IMS Fraunhofer - progress

- First report received on 24.07.2014
  - Electroplating and wafer thinning on **test wafers** – 95 %
  - Wafer grinding of test wafers – 90 %

Microbumps

- Deposition rates for Cu/Sn electroplating determined
- Uniformity in one chip < 5 %





During processing of this step one wafer broke

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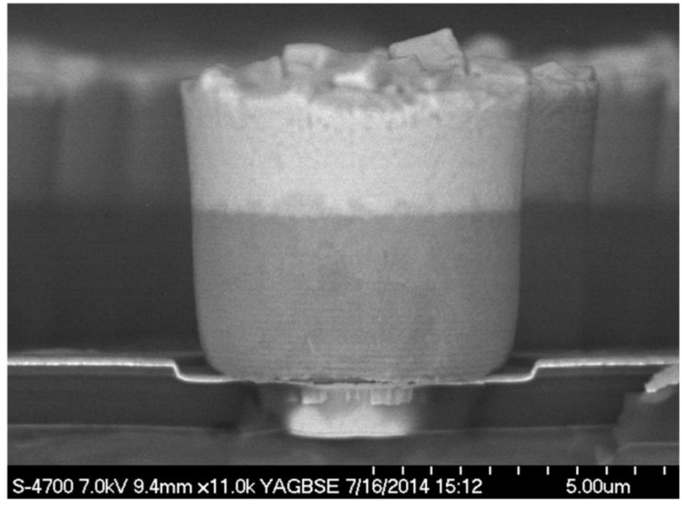
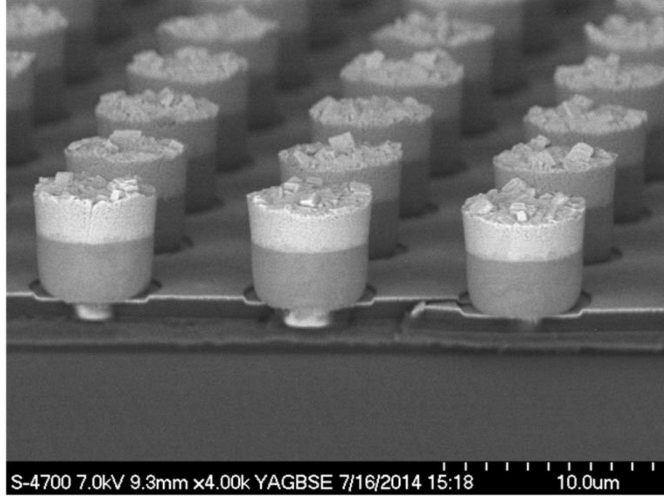
Wafer interconnecting IMS Fraunhofer - progress

- Second report received on 29.09.2014
  - Electroplating -> **done**
  - Wafer thinning -> **done**
  - Preparation of chip-to-wafer bonding –> **done on test wafers**

One wafer broke -> SEM images

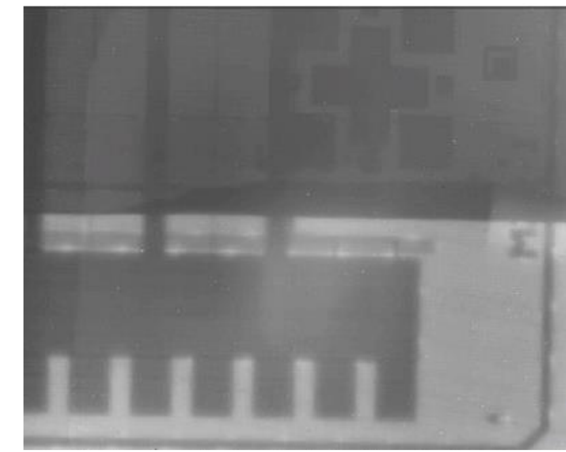


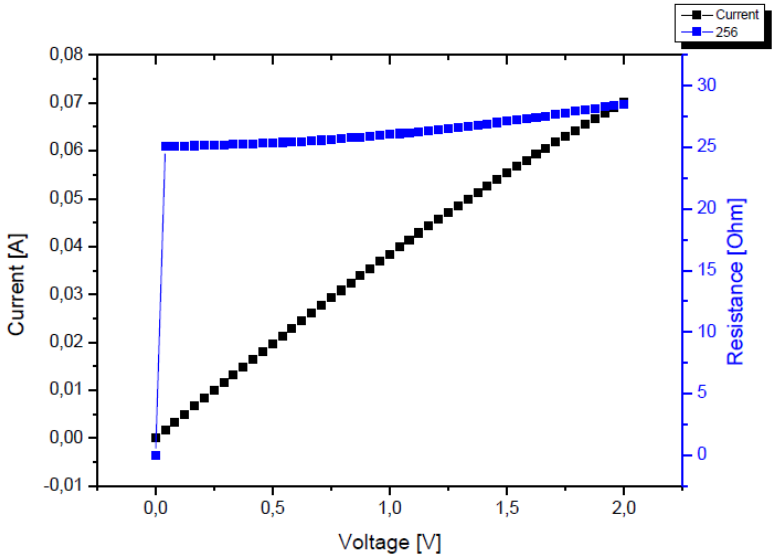


Wafer interconnecting IMS Fraunhofer - progress

- Third report – **8.12.2014**
  - First chip-chip bonding done
  - Daisy-chain measurements

  (256 connections) R ≈ 0.1 Ω / contact





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Wafer interconnecting IMS Fraunhofer - progress

News after intensive phone calls /email exchange in October:

- **One of the wafers broke** in the first step**, another** during second step-> IMS will try to get some dies from this wafer
- One of the machines crucial for finalization of the project was **in maintenance**
- One of the expert technicians went sick..

- Currently the thinned sensors were cut and IMS is testing **chip-to-chip bonding**
- In parallel, two wafers are being processed (with thinning to 100um to avoid braking) for **chip-to-wafer bonding**

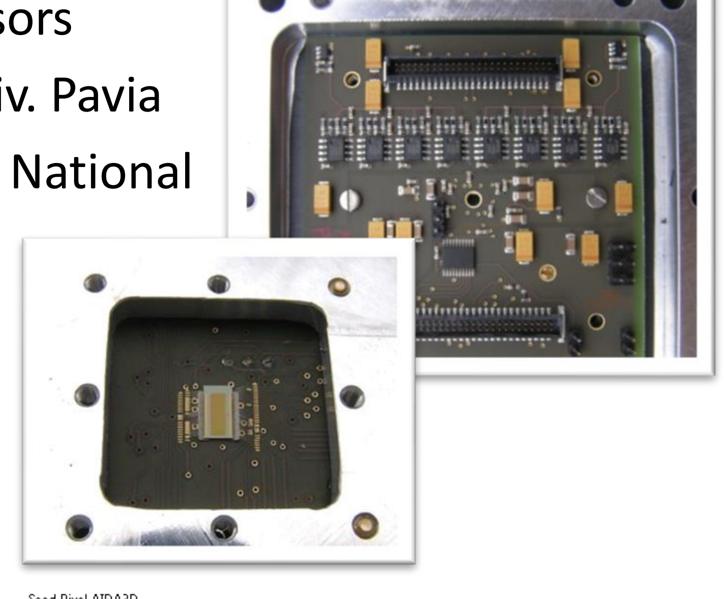
Wafer interconnecting IMS Fraunhofer - summary

- 5 step process:
  - Electroplating -> **done**
  - Wafer thinning -> **done**
  - Preparation of chip-to-wafer bonding -> **done on test wafers**
  - Chip-to-wafer bonding -> in progress ?
  - Dicing of the chip stack …

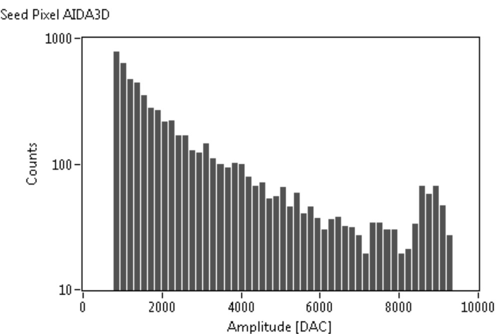
Results should not be expected before middle of December

Work done at IPHC

- Design and production of the PCB for the sensors
- Two PCBs with mounted test chips sent to Univ. Pavia
- Readout setup done from scratch with use of National Instruments FlexRIOFPGA + NI 5751 digitizer
  - 16 channell, 14-bit, 50MS/s



- Setup verified, results with ^{55}Fe obtained
- Adaptation of analysis software (TAF) under way (to be completed in coming days)



We are ready for the 3D chips

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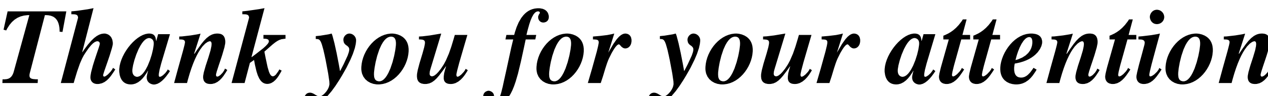
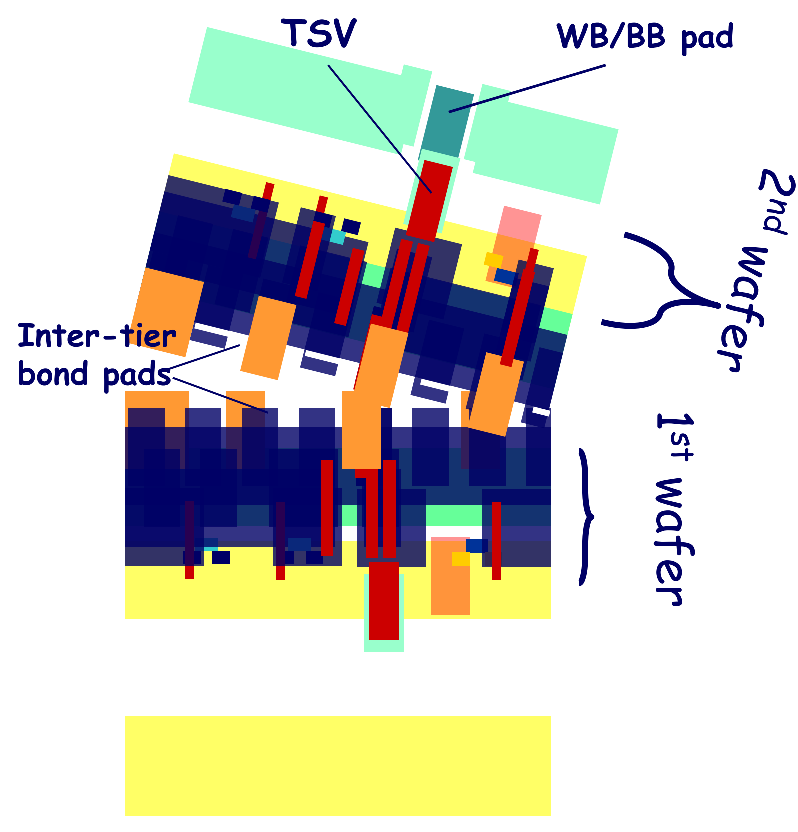

Thank you for your attention

Backup slides

Tezzaron vertical integration (3D) technology

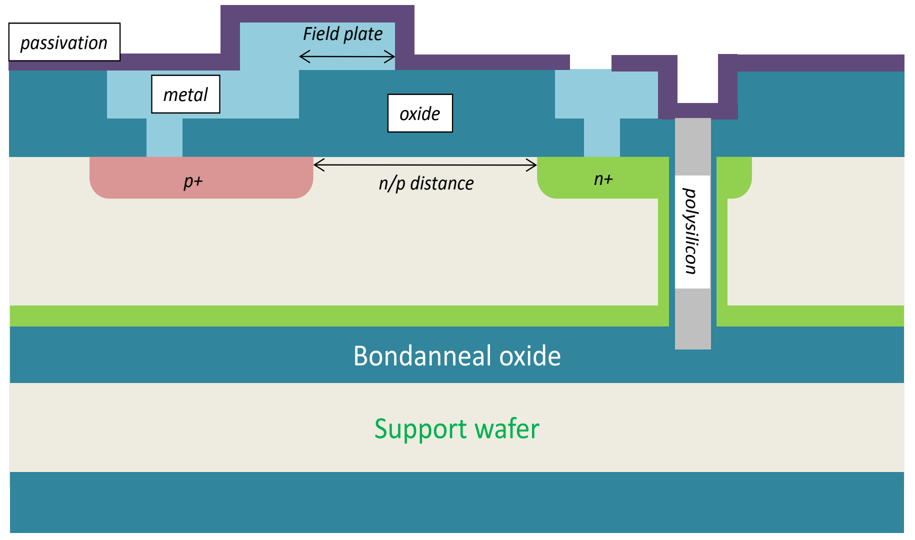


- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon the following enabling technologies
  - Fabrication of electrically isolated connections through the silicon substrate (TSV formation)
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/electrical bonding
- Tezzaron Semiconductor technology (via middle approach, vias are made between CMOS and BEOL) can be used to vertically integrate two 130 nm CMOS layers specifically processed by Globalfoundries

- Globalfoundries provides a 130 nm CMOS process with several different options; chosen one features 1 poly, 6 metal layers, 2 top metals, dual gate (core and thick oxide devices, 3.3 V), N- and PMOS with different V_{th}

Active edge sensors

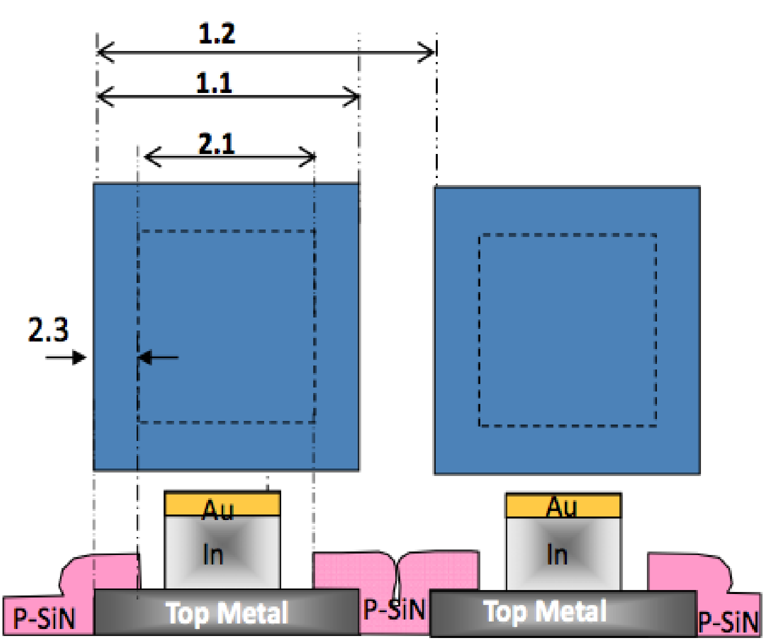
- Active edge pixel sensors used to minimize the gap between the last active element and edge of the detector but avoid high leakage current injection from the damaged cut region ← cut lines not sawed but etched with DRIE and doped to act as electrodes



- Introduced by Stanford as an extension of the 3D sensor technology

- Key steps: trench etching, trench polisilicon filling, support wafer removal

Vertical integration with T-Micro



- Very high interconnect density, with small bond pads (squares with a side of 5 or 10 μm, depending on the bump size, 2x2 μm^2 or 8x8 μm^2) both on the sensor and the readout sides ➔ more room for top metal routing, in particular for power and ground lines, smaller capacitive coupling, less material

Minimum size	DR1 8x8um bump	DR2 2x2um bump
1. Top metal (Landing pad of bump)		
1.1 size	12 um	4um
1.2 pitch	15um	5um
1.2' Pitch (dummy pad)	15um	5um
1.3 minimum space to scribe edge	10um	10um
2. Pad opening		
2.1 size	10um	3um
2.2 pitch	15um	5um
2.3 minimum pad overlap of pad opening	1um	0.5um

Alignment rules

- Markers for rough and fine alignment (through IR imaging) - apparently not mandatory

sensor chip

Sensor chip (Top metal)

RO chip (Top metal)

190μm

150μm

120μm

40μm

40μm

30μm

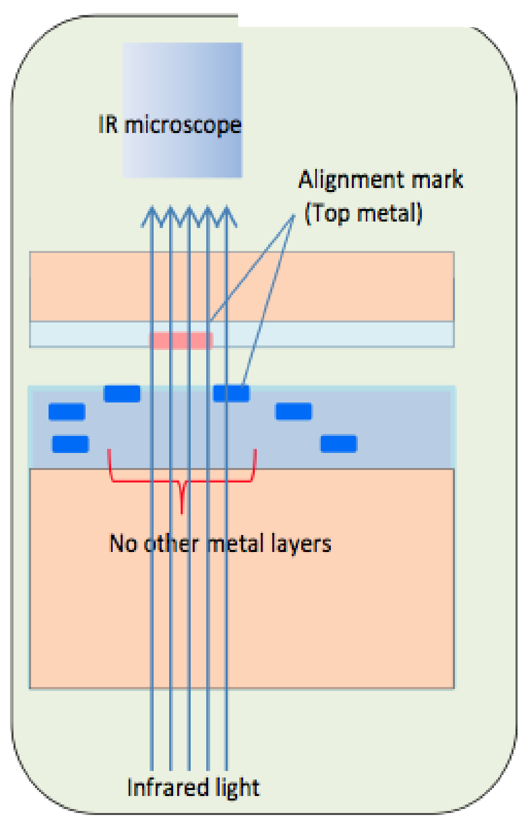
25μm

24μm

4μm

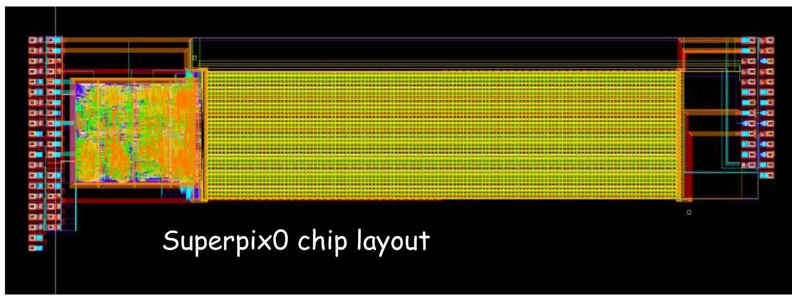
Sensor Chip

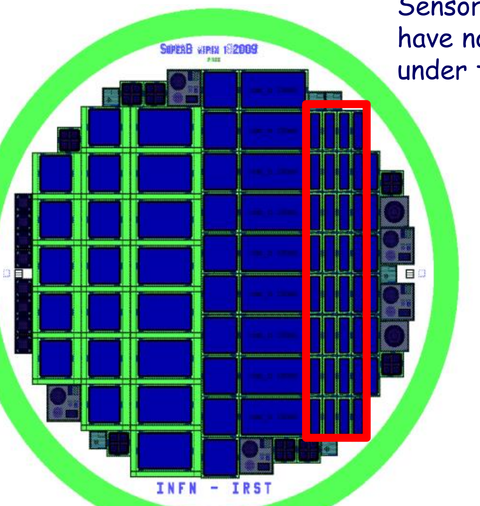
RO chip



Vertically integrated layers

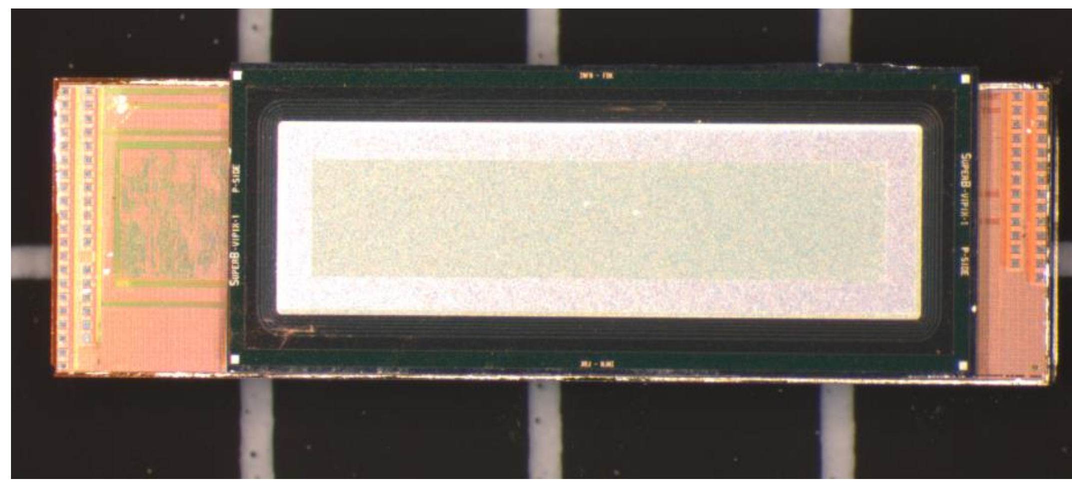
- Preliminary test of the T-Micro integration process performed on pre-existing readout chips (Superpix0) and high resistivity n-on-n pixel sensors (VPix1)





Sensors in the red box have no metal layers under the markers

- Front-end chips and a pixel sensor wafer shipped to T-Micro in Dec. 2012



- 6 vertically integrated chips have been shipped back to Italy, tests are in progress

Surface inspection and alignment

T-Micro

Result of Chip stacking

February 28,2013

	after surface treatment (cleaning)		after bump lithography		after bump formation		after Stacking	Remarks
	ASIC Chip	Sensor Chip	ASIC Chip	Sensor Chip	ASIC Chip	Sensor Chip	(Two alignment mark images using IR microscope)	
Chip_01								Only for process optimization (in another chip tray with broken chips)
Chip_02								
Chip_03								
Chip_04								
Chip_05								
Chip_06								large alignment error
Chip_07								