Science & Technology Facilities Council

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Status of the 3DIC project

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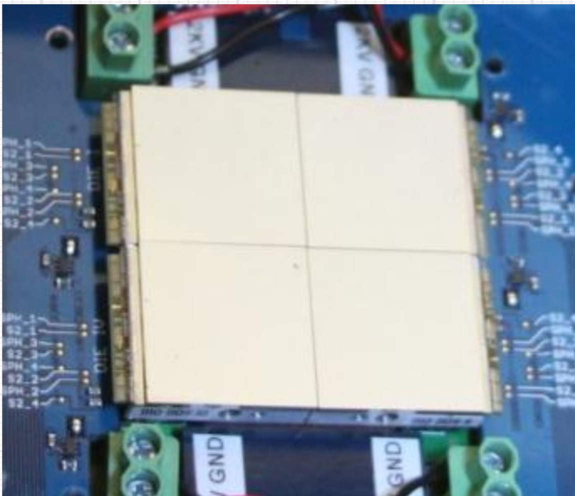
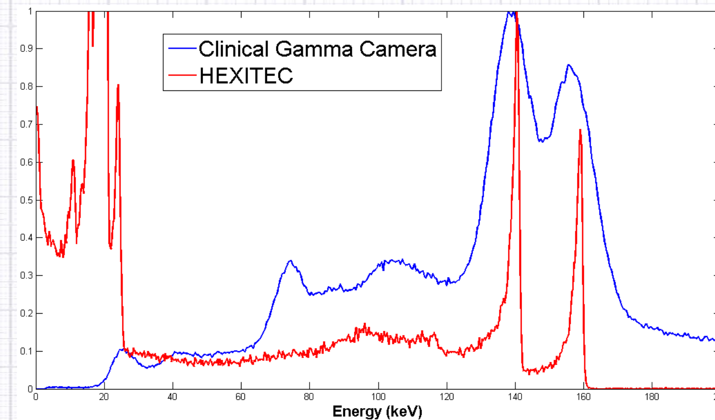
Background

- Demonstrate that 2-tier 3D pixeldetector readout ASIC with vias in every pixels can be done "via last"
  - Analogue tier based on proven Hexitec platform

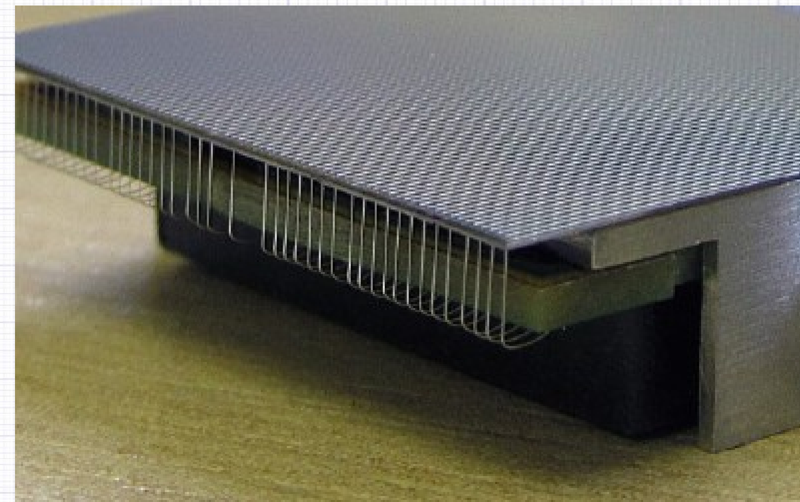




  - Digital tier contains a 12bit (10bit) digitizer in every pixel and readout.

Hexitec 4S

- The STFC group (no Uppsala participation) did develop a 4-sided buttable version of Hextic with I/O made minimal and redistributed to the rear face of the ASIC
- ASIC thinned down to 120 μm
- TSV 70 μm DRIE cut with redeposited SiO2 through the 120um thick silicon. The metal via is mostly copper connecting to the Al pad. Process done by T-Micron (JP)
- Generally successful demonstration of via-last process.
- Problems encounter are high contact resistance in I/O pad and non flat ASICs after thinning

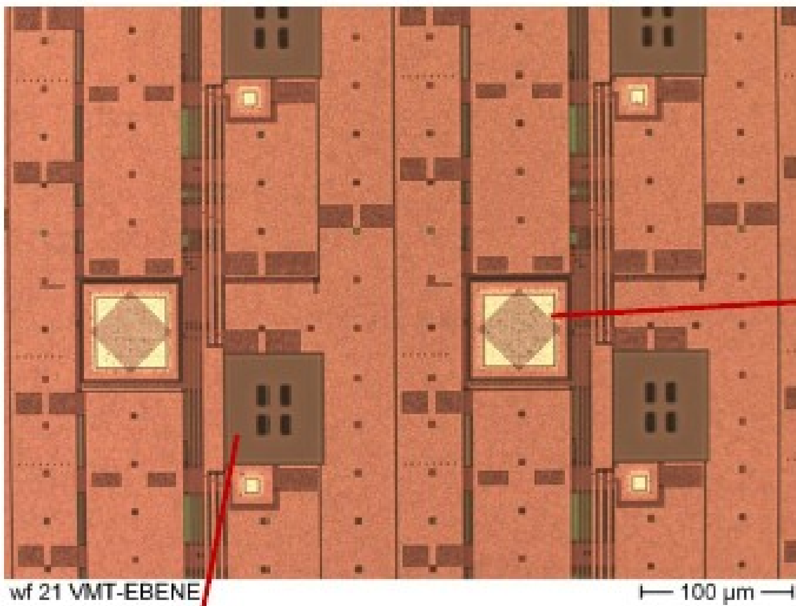


Specifications

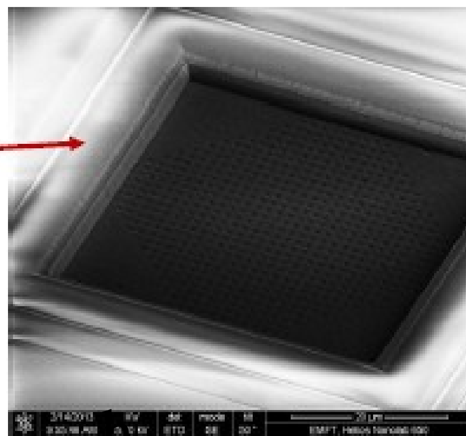
- Technology ASIC: AMS 0.35 μm
- 40x40 pixels
- Effective pixel pitch 250x250 μm
- 4-side buttability
- Digitization modes 12 and 10 bits
- Output of “hit-pixel”
- Each pixel should be able to handle 2 hits/readout (~deadtimeless operation)

Progress

- 12 wafers containing both tiers produced, tested and shown to be well functioning. (pre-AIDA)
- In 2011 EMFT were contracted to thin the "Analogue" wafers
- In 2012 EMFT were contracted to finish the SLID bonding (there was an unfortunate long delay between these two steps because of contract issues)
- The first SLID parts were delivered in Mid 2013 (rather than end 2012)
- The first full wafer of SLID parts were delivered in Oct 2013

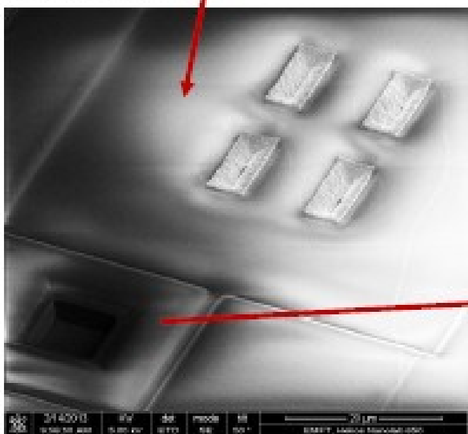


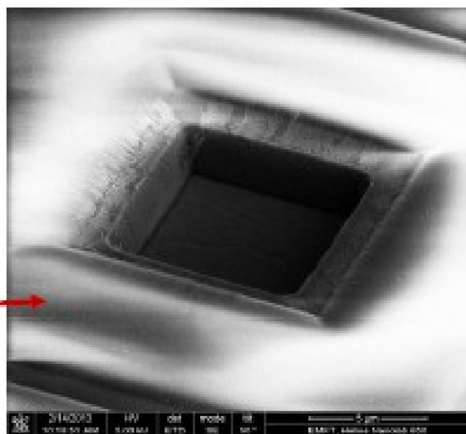
- View of pad and in-chip areas after tungsten etch and oxide opening to device pads;
- Resist is still on top of oxide

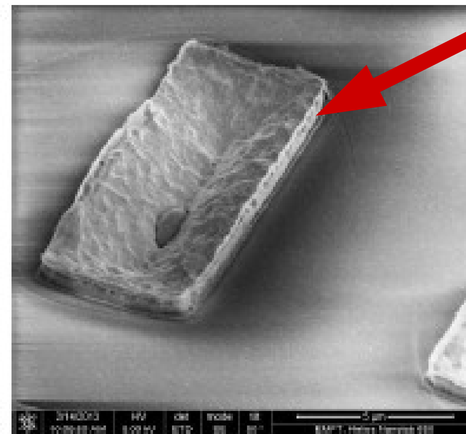


- Oxide on device pads is removed

3umx10um TSV







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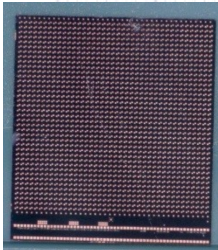
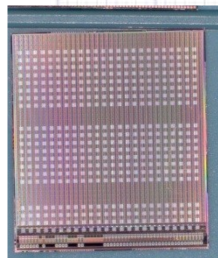
Deliverables (& lessons learned)

- TSV processing and contact metalization went generally OK
- Excessive stress induced in the thinning process (to 50 μm) and this had to be modified to stop the wafers cracking
- Back side metalization critical and is one of the main worries.
- EMFT have now delivered a wafer of SLID bonded ASICs and some non-bonded parts
  - 9 proper devices (thin top analogue to thick digital) on the wafer that are properly SLID bonded together
  - 10 thin top digital bonded to thick analogue. The SLID bonds are not functionally and the devices have a non-functional checker-board Al pattern on top surface. These do have good wire bond pads so can be connected to test boards.
  - 5 thin analogue and 5 thin digital ASICs. One analogue AISC went for stress imaging at ANKA.



Analogue (top)



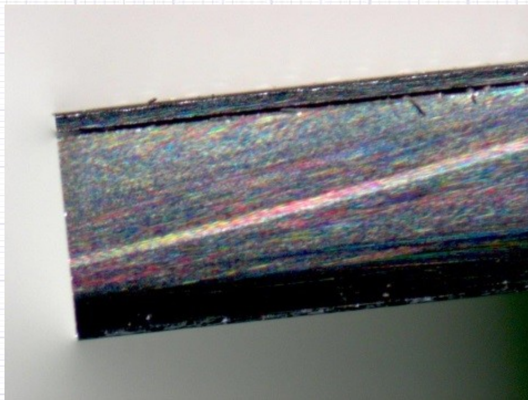
Digital (bottom)

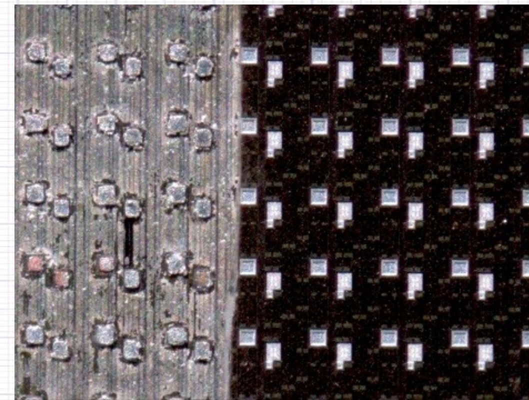
Cont.

The full SLID wafer is visibly very poorly bonded (Fig 2) and we do not expect any good devices but there could be valuable indications by using the new system. We have used some ASICs from the wafer but there were only 6 devices worth taking from the wafer.

Analogue SLID

Digital





Digital (bottom)

Analogue (top)

EMFT agree, that the device SLID looks very poor and there will be very poor yield. 3DIC is still strategically important for them and they have committed to continue the development. They agreed to reprocess devices Free Of Charge if we can provide more wafers.

Current status

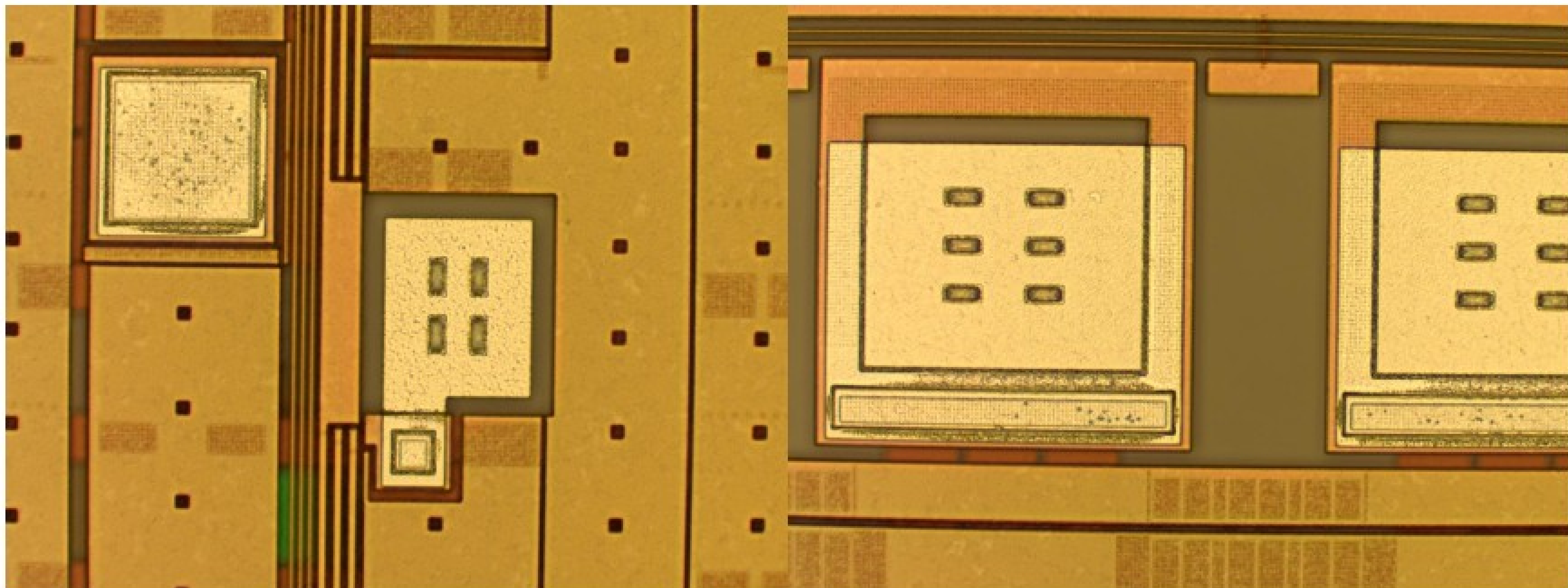
- Reduced depth of TSV and therefore remaining silicon thickness to 24 µm
- Tungsten filling successful to the bottom of the TSV
- Single TSVs without isolation trench to improve mechanical stability nearby through contacts
- Backside preparation shortly before metalization of TSV contacts
- Bottom wafers with copper / tin pads are prepared

Top wafer layers

	ref #	Function	Layer Name	done
front	0	Last-Metall Product Chip	Zero	
front	1	Isolationstrench [& Deep Trench]	TRE	✓
front	2	TSV-Kontact	TSV	✓
front	3	Tungsten Etch	TEB	✓
front	4	Tungsten-Via	VTT	✓
front	5	Via-to-Last Metal	VMT	✓
front	6	Aluminium	MTT	✓
front	7	Passivation Opening	BPO	✓
front	8	Polymer for Thinning		✓
back side	9	Thinning		✓
back side	10	Tungsten-Via Back Side*	VTB	✓
back side	11	Aluminium Back Side*	MTB	next
back side	12	SLID-Pad Top		

Bottom wafer layers

	ref #	Function	Layer Name	done
front	13	Aluminium pad	MTB	✓
front	14	SLID-Pad Bottom	MLB	✓

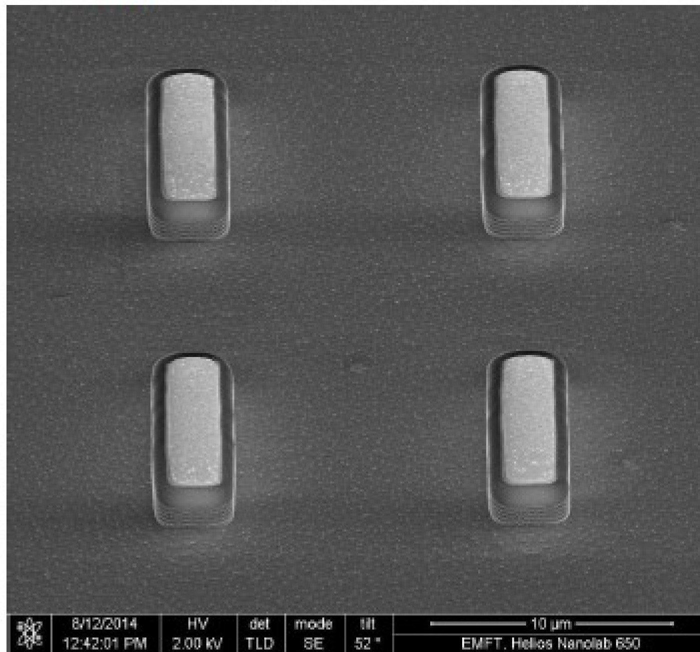


- Aluminium contact of TSV to device within array
- Aluminium contact of TSV to device at bond pad

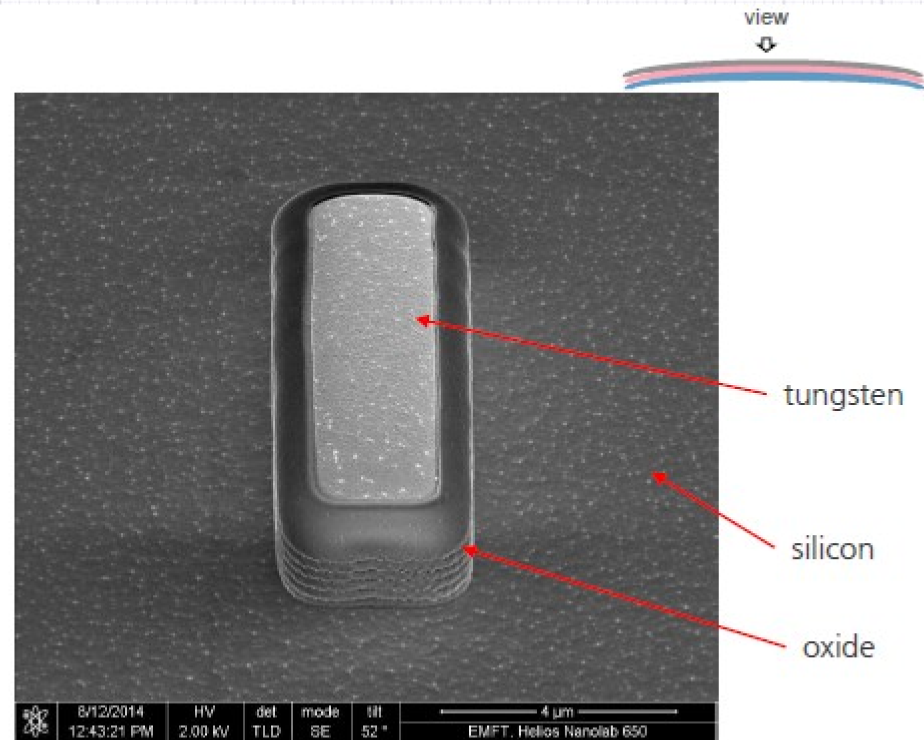
Access TSV on thinned top wafer

Final preparation of TSV access

view



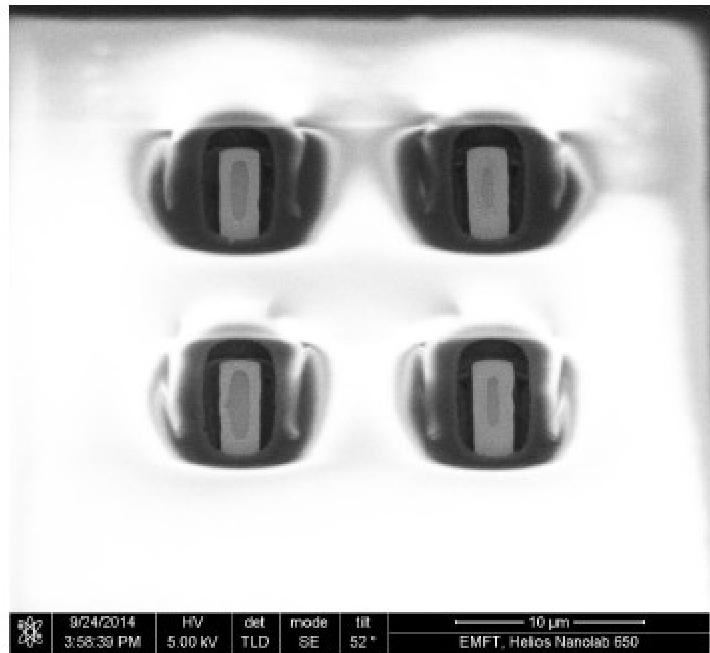
Interchip TSVs array after silicon recess; TSV-sidewall covered with isolation oxide

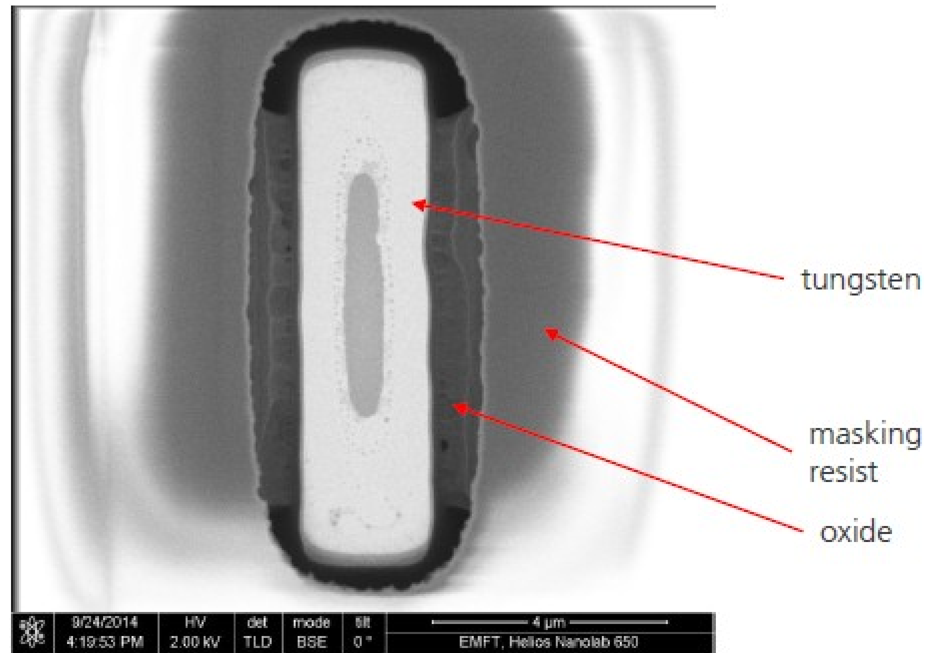


Detailed view of interchip TSVs

Final preparation of TSV access; access to TSV-metal

view





TSVs after coverage with resist, selective opening of resist over TSV and subsequent etch removal of exposed oxide

Summary

- 2-tier via-last ASIC being developed
- 40x40 pixels with TSV's in every pixel
- A full process round completed with successful processing steps on the TSV processed tier but with unexpected problem during SLID interconnection of tiers
- A second run in progress which we hope will result in working devices that can be tested and functionality demonstrated in (existing) test setup in the next month.