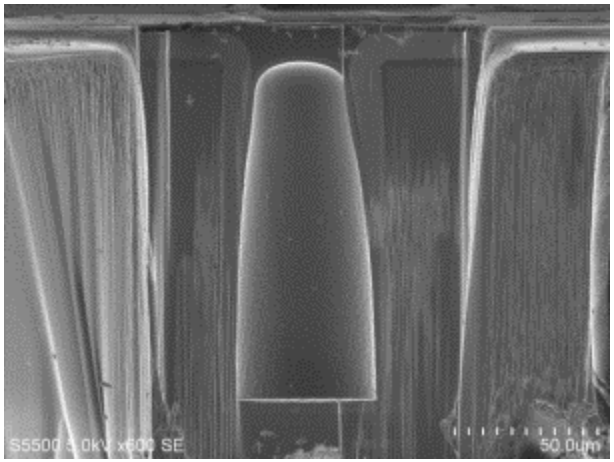
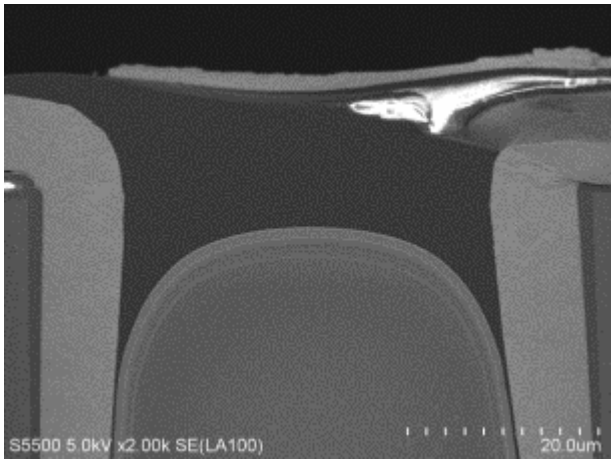
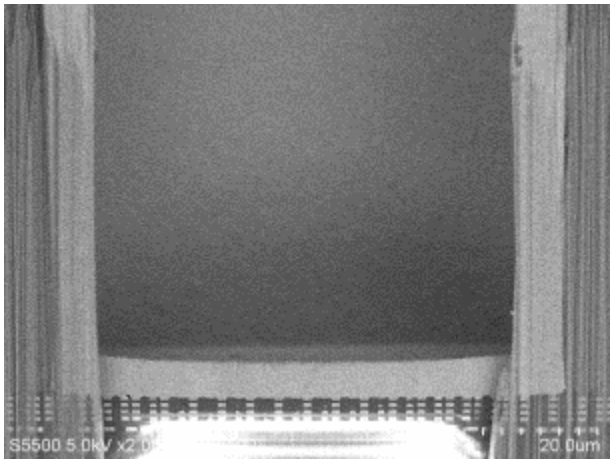
CERN Medipix TSV PROJECT

AIDA FINAL MEETING - WP 3.2







SEM images of a TSV courtesy of CEA LETI

CERN Medipix TSV PROJECT - Introduction

- The goal was to develop a reliable "Via-last" TSV (Though Silicon Via) process for Medipix Hybrid Pixel Detectors and to be able to redistribute interconnects on the back side of the chip.

- The main benefit is to limit the need of classical wire bonding to sensor biasing only. Large area tiling with high percentage of active area is an important feature for both radiation imaging and particle physics

- AIDA has contributed to about 30% of the cost of the 3 first runs of production and the related developments during the last 4 years. The remaining funding was supported by Medipix3 collaboration and CERN-LCD (Linear Collider Detector project at CERN)

- The 3D process developments were done in close collaboration with CEA Leti (Grenoble – France) through the Open3D framework and using their on-site clean room facility

- ADVACAM (Espoo - Finland) VTT spin-off company provided the expertise in sensor fabrication (edgeless) and flip chip assembly

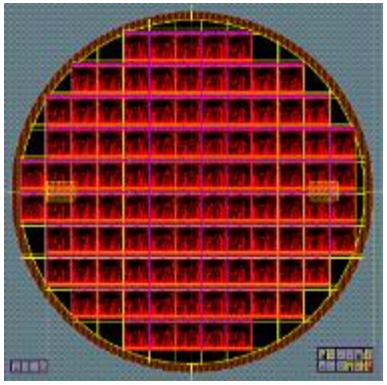
CERN Medipix TSV PROJECT – First run – 3D01

- 10 tested Medipix3.1 wafers (low-yield) were provided to CEA Leti for TSV process development. Medipix3.1 chip was designed to be compatible with the TSV last process. All chip I/Os are accessible either through wire bonding extender or TSV pad located in Metal-1 inner layer.

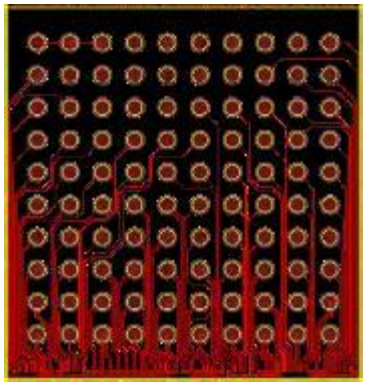
- Specific test structure requested by Leti have been implemented during ASIC development under wire bond extender area on Metal-1 inner layer of the chip. These allows TSV process monitoring without compromising the integrity of the chip. Polysilicon filling structures in TSV region were avoided

- CEA Leti has helped us to design the back side redistribution layer for every chip at the wafer level and also implemented the back side test structures (snakes, 3D-kelvin test etc.)

Wafer level back-side redistribution lines to TSV plus test structures

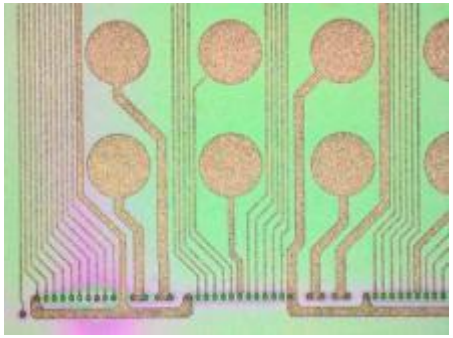


Chip level "BGA like" contacts created

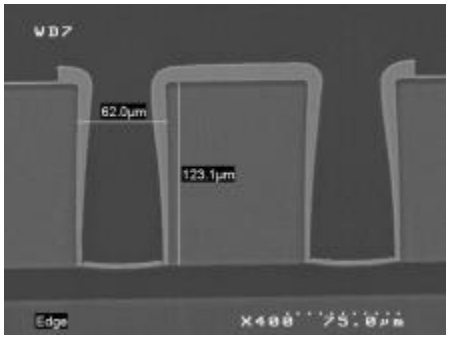


CERN Medipix TSV PROJECT – First run - Process

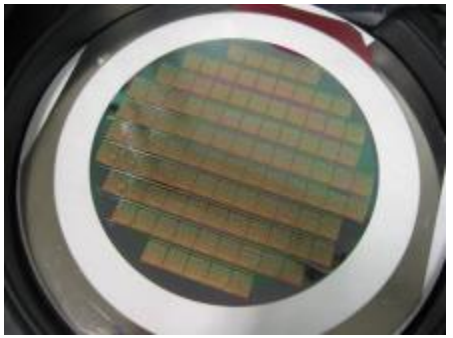
- Front Side UBM (TiNiAu) was done prior to back side processing.
- After bonding front-side to a temporary wafer carrier the back-side process starts. First with thinning from ~720µm to ~120µm (needed to limit the via aspect ratio) then TSV and RDL patterning and finally passivation and back side UBM.
- Finally the wafer is removed from temporary carrier and place on another specifically adapted for dicing and ejection.
- CEA-Leti encountered some difficulties at that time to tune the process. The non-planarized front side adhered to the support wafer differently from dummy wafers. TSV etching parameters had to be adjusted to reach the M1 inner layer and establish a good electrical contact without compromising the isolation between adjacent TSVs.



RDL microsope view



SEM cross section of TSVs

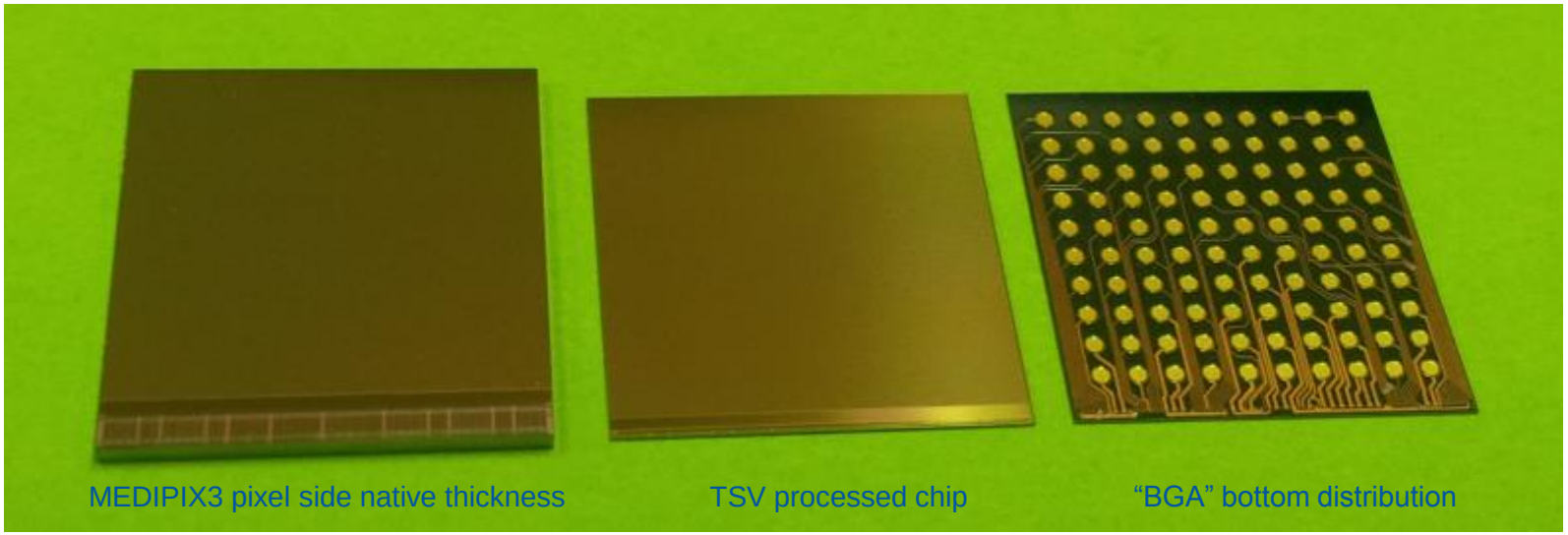


120um thinned and processed wafer on dicing tape

* Images of a TSV courtesy of CEA LETI

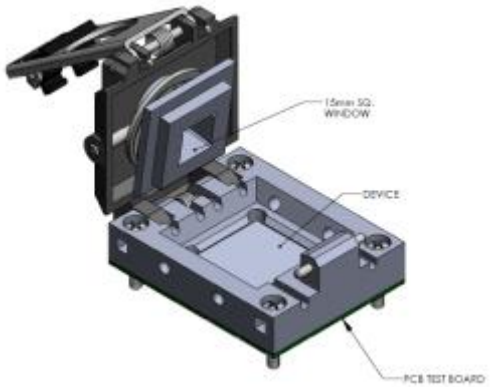
CERN Medipix TSV PROJECT – First run - Inspection

- CEA Leti provided us several diced chips in Gelpak for electrical test and visual inspection, in parallel, one TSV processed full wafer was sent to ADVACAM directly for assembly trials. Below is a direct visual comparison of a standard chip and (left side) and two TSV processed chips (middle and right side) viewed from top or bottom.



CERN Medipix TSV PROJECT – First run - Test

- A test board has been developed at CERN. It could be used with the same readout system as the one connected to probe card during original wafer tests.

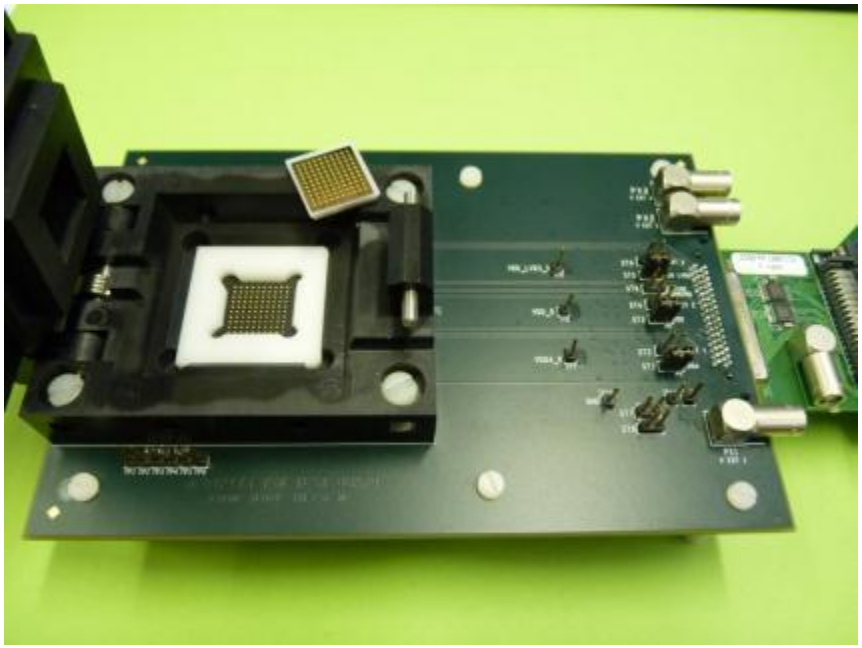


CSP style for "Ball Grid Array" chips until 3x3mm

"BGA" side

Side view of one pin

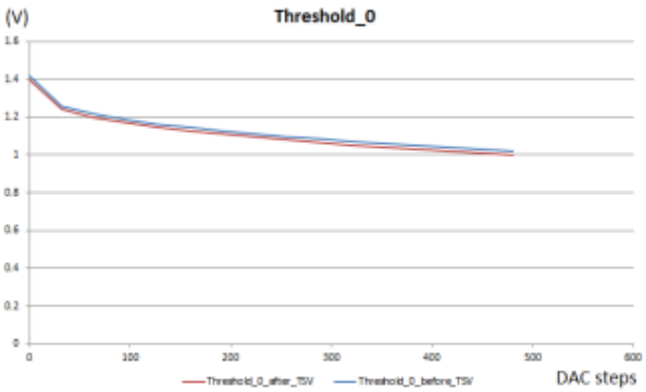
Printed Circuit Board side



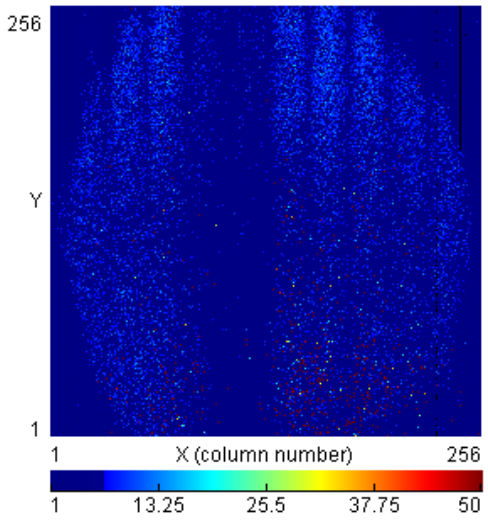
Polymer parts (in white) machined by Firscut company are used to maintain the chip aligned to pins

CERN Medipix TSV PROJECT – First run - Results

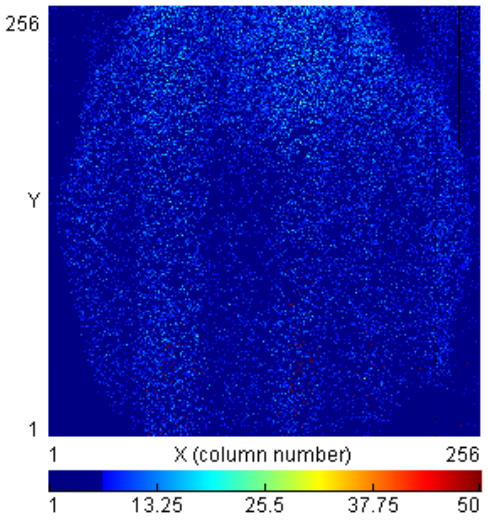
- 10 parts out of 14 received were functional and passing the test, giving a TSV yield of 71.4 % on this small lot.
- Comparison of internal DAC behaviour shown really minor drifts.
- Chips were almost all classified with low grade (one or more bad column) during original wafer test. Some of them where not so badly rated but still suffered originally from an inhomogeneous noise floor due to yield issues in that lot.



Comparison of one DAC Threshold 0 dependency before and after TSV. No significant drift are noticeable. Selected sample is W24 chip H2



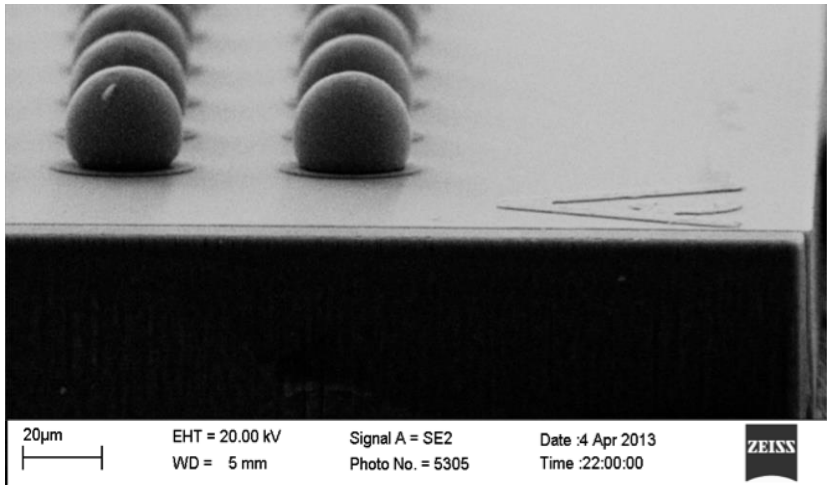
Noise floor before TSV. Selected sample is W24 chip H2



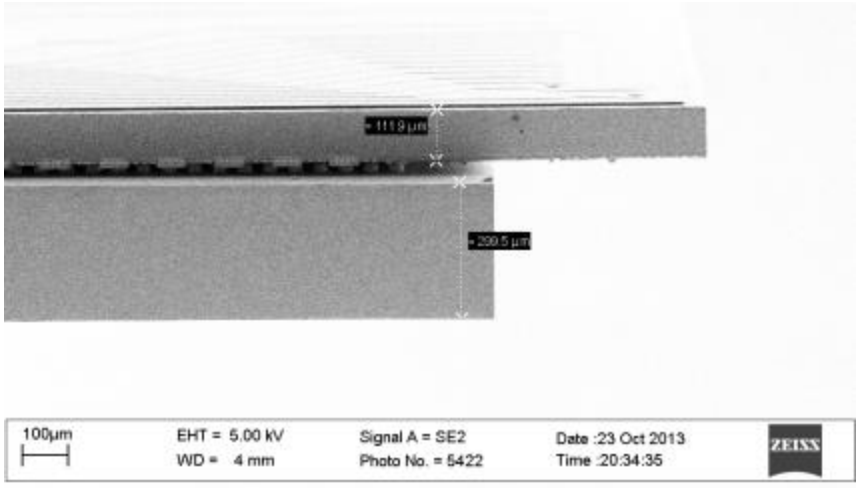
Noise floor after TSV. Selected sample is W24 chip H2

CERN Medipix TSV PROJECT – First run - Assemblies

- First assemblies with edgeless sensors were received from ADVCAM in october 2013

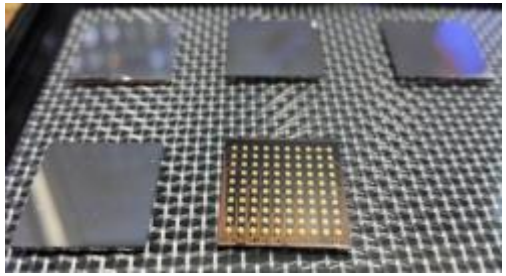


* Sensor with Sn-Pb solder bumps
After reflow process



TSV Readout Chip assembled to an
edgeless sensor (300um thick)

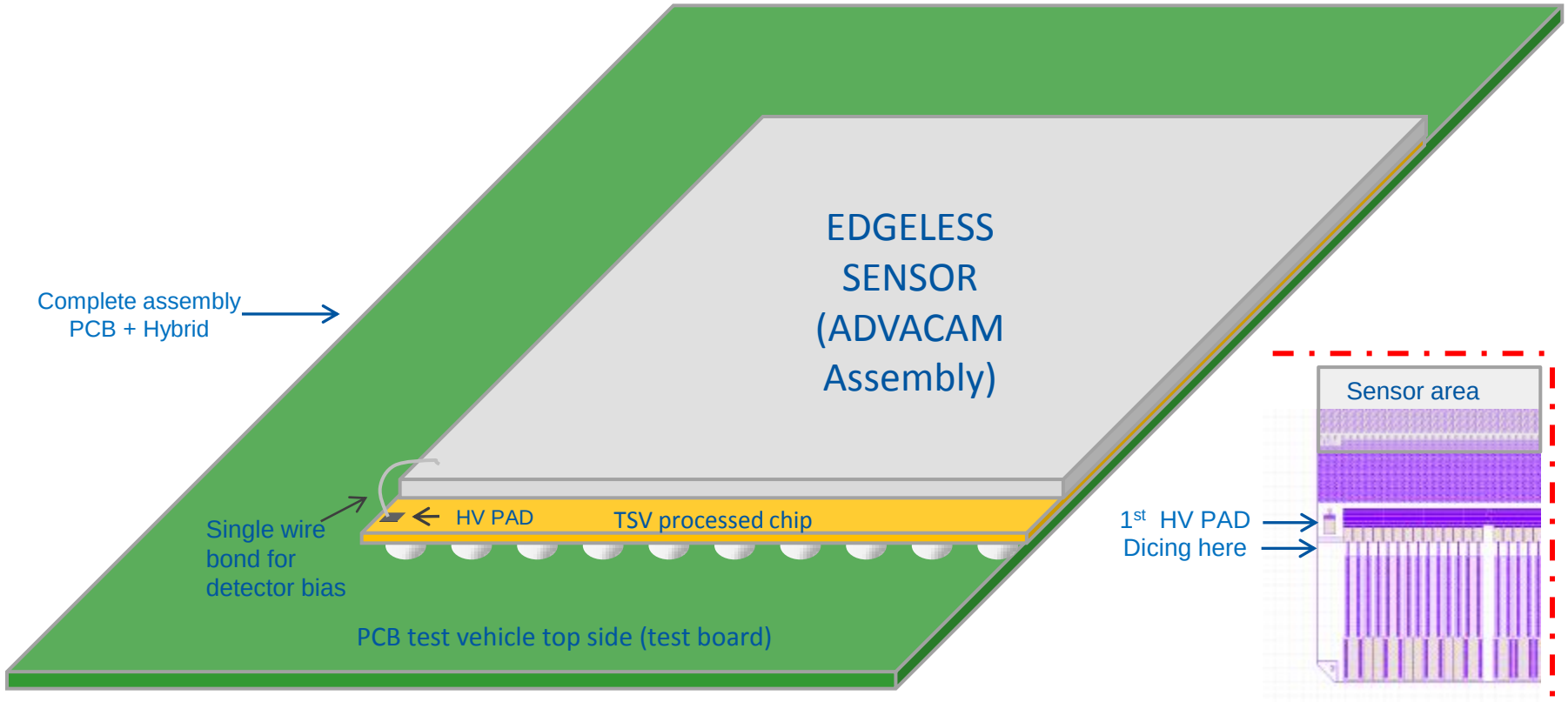
5 assemblies
ready for test



** SEM images courtesy of Advacam*

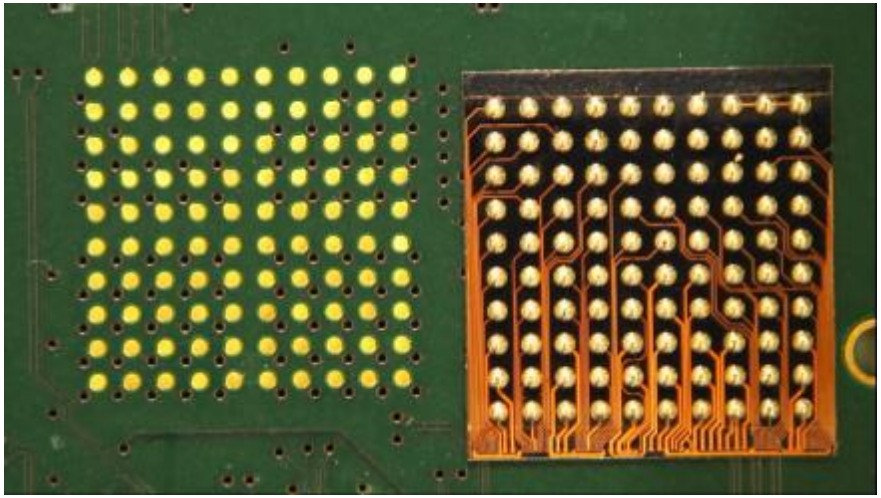
CERN Medipix TSV PROJECT – First run – Chip-on-board

- It was decided to reuse the test board without the test socket fortunately its footprint matching redistribution layer BGA footprint



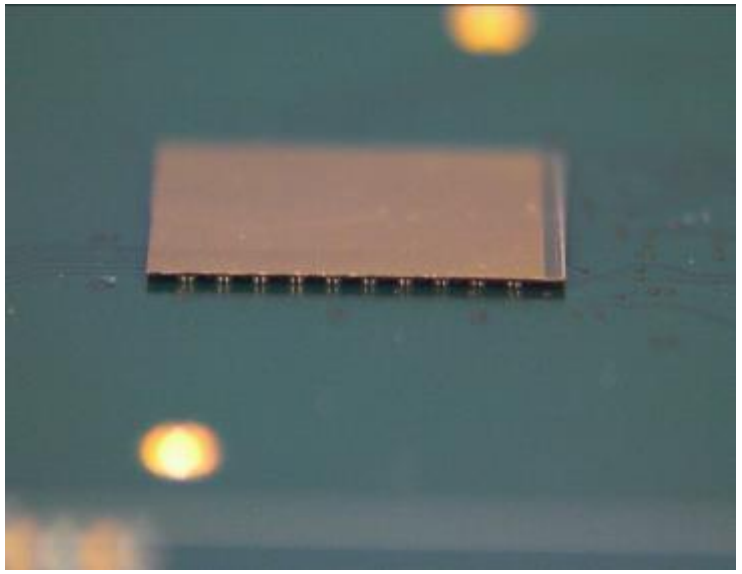
CERN Medipix TSV PROJECT – First run – Reflow

- BGA pads on the redistribution layer (back side of the chip) have been prepared with low temperature solder spheres



PCB BGA footprint

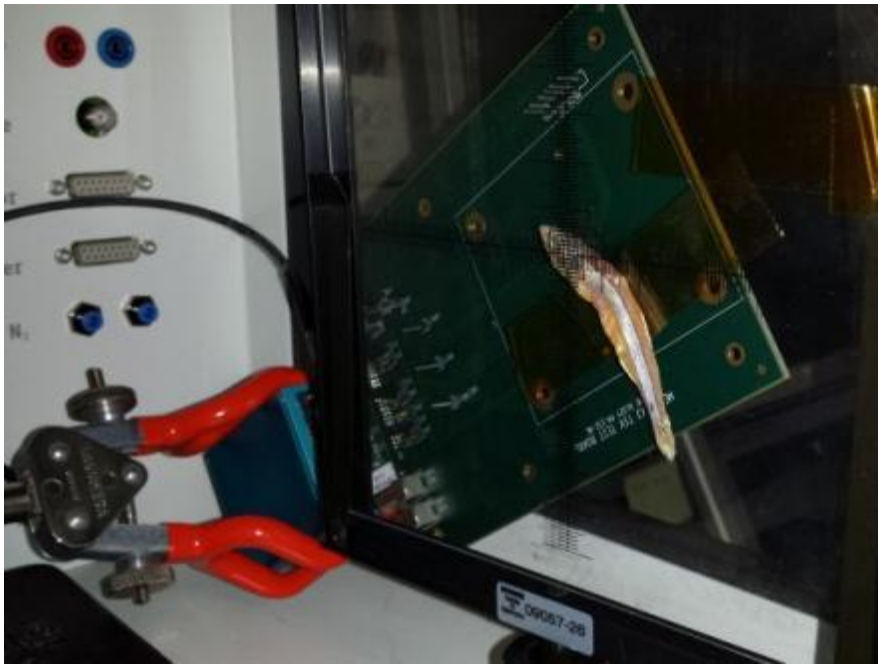
Bare chip with solder spheres
57Bi42Sn1Ag/Indalloy #282



First trial with a bare Medipix 3.1 TSV processed chip assembled on board

CERN Medipix TSV PROJECT – First run – X-Ray imaging

- Hybrid Pixel Detector was positioned in front of the X-Ray beam
- A biological sample (fish) placed before the detector
- X-Ray chamber 35kV, 1mA



First irradiation setup using a Medipix 3.1 TSV assembly

First image obtained with a TSV processed hybrid pixel detector (flat field corrected)

CERN Medipix TSV PROJECT – First run – Conclusion

- The first TSV run (3D01 in Leti) showed very encouraging results. Despite first difficulties to tune the process, last lot of wafers was delivered with a reasonable TSV yield. Unfortunately the original wafers were not so good

- A test setup has permitted to validate several lot of chip. Several candidates were selected for flip chip assemblies and on-board integration. Functionality of the whole process as been proven and had permit to achieve foreseen results

- Process validated and first electrical obtained were published and presented in :

ECTC 2013 by David Henry in Las Vegas (US)

TSV last for hybrid pixel detectors: application to particle physics and imaging experiments

D. Henry(1), J. Alozy(2), A. Berthelot(1), R. Cuchet(1), C. Chantre(1), M. Campbell(2)

(1) CEA Léti – MINATEC, 17 rue des Martyrs ; F-38054 GRENOBLE - France

(2) CERN, European Organization for Nuclear Research, 1211 Geneva 23, Switzerland

And briefly presented in TWEPP 2013 by Yann LAMY in Perugia (IT) during a more general presentation about 3D integration

3D Integration, from tool box to applications Yann LAMY *(CEA- LETI)*

CERN Medipix TSV PROJECT – Second run – 3D05

- The motivation was to reuse processing experience developed during 3D01 but this time applied to better performance MEDIPIX3RX ASIC wafers and to prove that high yield could be obtained

- Technical proposal from CEA LETI in February 2013. RDL lines have been redesigned because the distribution of TSV has slightly changed. But still the BGA footprint stay the same

- Medipix3RX TSV project started in July 2013 under supervision of Mr Gabriel Pares the new Technical manager of the project. Mr Yann LAMY is the Program Manager

- 6 Medipix3RX tested with good yield wafers supplied by Medipix collaboration to be processed

CERN Medipix TSV PROJECT – Second run – Status

Second run split in two lots:

<u>Lot # µSA999P of 3 wafers:</u>

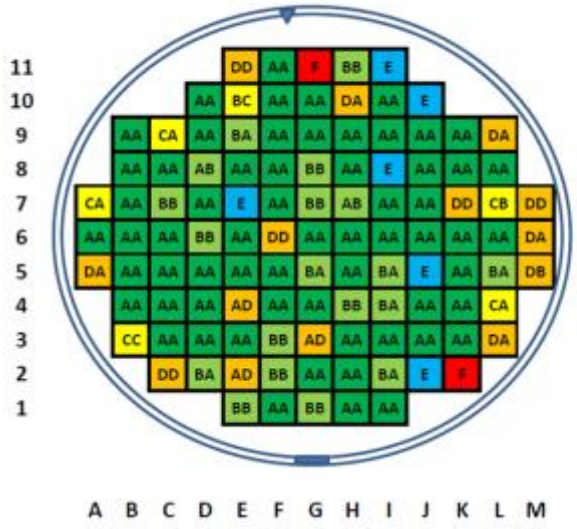
- P04 (W128-AZPGBPH) : completed, delivered to CERN and tested
- 14 chips (7 class AA + 7 with other classes) sent to ADVACAM for assembly in early august. First assemblies recently received. Test in progress.
- P05 (W127-AKPGALH) : need rework (during 3D06)
- P06 (W126-AMPG6LH) : completed, delivered to CERN and tested

<u>Lot # µSB254P of 3 wafers + 3 monitors:</u>

- P01 (W125 A3PGC2H) : completed, delivered to CERN and tested
- P02 (W124 ACPGAUH) : completed, delivered to CERN partially tested
- P03 (W123 A0PGBNH) : completed, delivered to CERN and tested

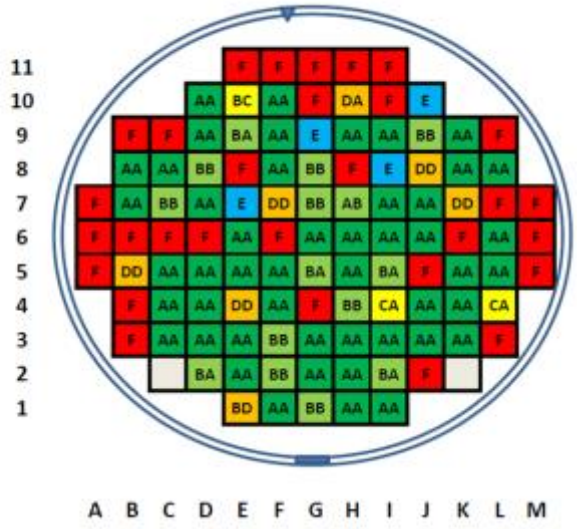
CERN Medipix TSV PROJECT – Second run – Test at CERN

W128_AZPGBPH_before_TSV



AA	62	57%
BB, BA or AB	19	17%
CC, CA, AC, BC or CB	6	6%
D	14	13%
E	6	6%
F	2	2%
Total	109	100%

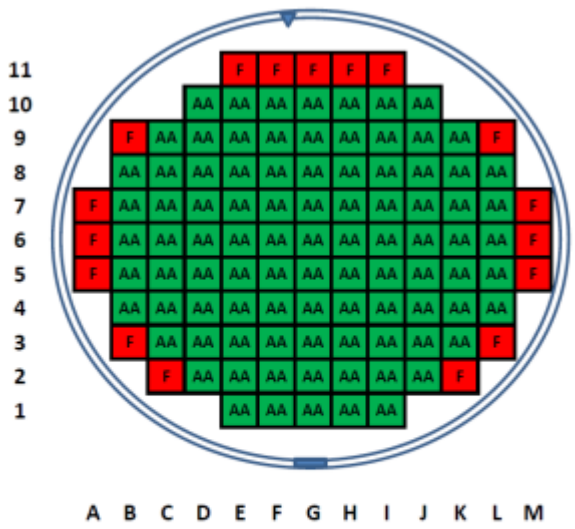
W128_AZPGBPH_after TSV



AA	48	45%
BB, BA or AB	15	14%
CC, CA, AC, BC or CB	3	3%
D	7	7%
E	4	4%
F	30	28%
Total	107	100%

C2 and K2 were not received

Bad dies due to process active area



AA	92	84%
BB, BA or AB	0	0%
CC, CA, AC, BC or CB	0	0%
D	0	0%
E	0	0%
F	17	16%
Total	109	100%

* Original wafer probing results (Foundry yield)

After foundry production and TSV added process the final yield is 45% of fully functional chips

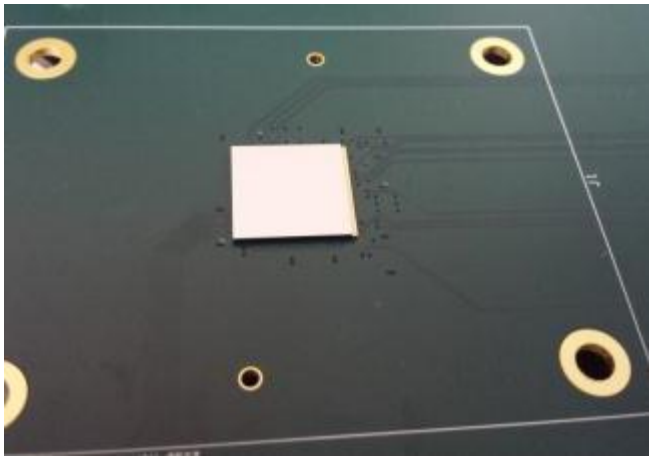
We have identified that due to equipment size limitation we are loosing some dies at the edges. Either the RDL is not completed or the TSV are not fully processed in certain region (resulting F classification)

*Class AA means perfect chip, Class Bx are with one bad column over 256, Class Cx are with two, Class Dx with more than two, Class E with bad internal DAC(s) and class F not functional (bad communication and or power failure)

CERN Medipix TSV PROJECT – Second run – Ongoing activities

- We are currently completing the electrical tests of the whole 3D05 production
- Yields obtained and performances achieved are matching our expectations
- We have received in late November several MEDIPIX3RX assemblies from ADVACAM with various sensor thicknesses.
- Testing has just been started and one of the newest assemblies has been already mounted on board

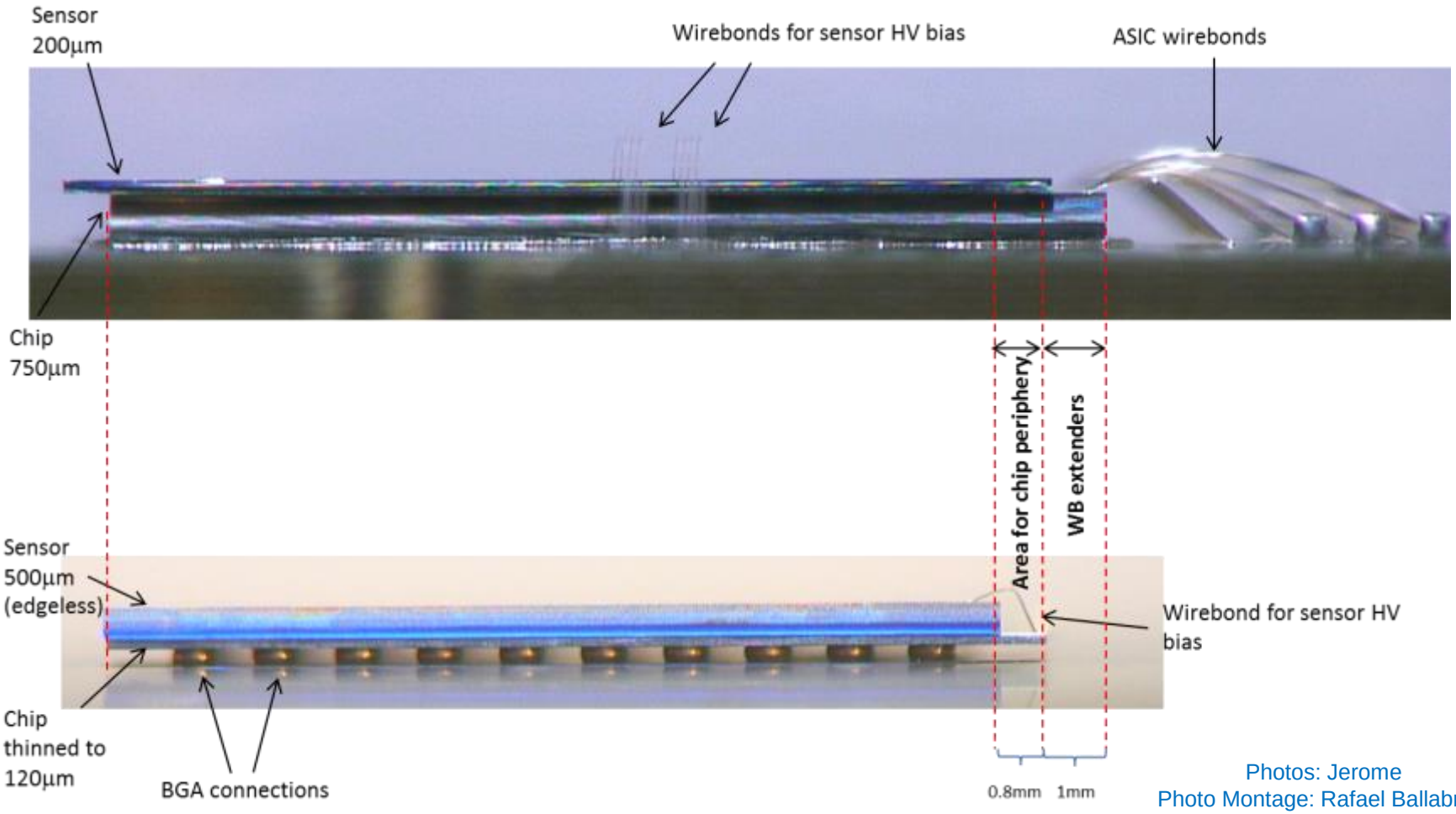
9 functional assemblies arrived



500um sensor assembly mounted on board

CERN Medipix TSV PROJECT – Second run – Integration

- Comparison between WB and TSV on board integration



Photos: Jerome
Photo Montage: Rafael Ballabriga

CERN Medipix TSV PROJECT – Third run – 3D06

- Technical proposal from CEA LETI in March 2014 (finally launched in July 2014)

- Proof of concept of TSV last with TIMEPIX3 wafer thinned to ~50µm (High Energy Physics Experiments such as CLIC would like lowest hybrid detector mass)
- Further develop the TSV process to such thickness

- First lot will be made using 2 Medipix3RX that is well known and TSV compatibility has been proven
- Second lot will ne made using only 2 Timepix3, since limited number of Timepix3 candidates are available

- Final BGA footprint with similar dimensions compared to what have been done with Medipix3 to reuse test socket probes

Ongoing process

CERN Medipix TSV PROJECT – Conclusion

- Good results with Medipix3RX TSV processed (120µm), with good number of class AA devices
- We are about to fully validate the project with recently received assemblies
- Part will be soon distributed to collaborators for integration test (ESRF – Grenoble)
- TSV processing is now available for other hybrid pixel projects

- Challenging project related to ultra-thin TIMEPIX3 TSV processed chips in progress with plenty of possibilities concerning final user
- Tiling of large area for low mass detectors (CLIC)
- Timepix3 with TSV interconnects would be perfect inside Hybrid Photon Detector or GEM detectors were wire bonding are limiting the performances

Thanks you!

Do not hesitate to contact me for more details

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