WP3

Microelectronics and interconnection technology

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The goals of AIDA WP3

- AIDA WorkPackage3 had the goal of facilitating the access of our community to advanced semiconductor technologies, from nanoscale CMOS to innovative interconnection processes.

- **WP3.2:** 3D integration for novel tracking and vertexing detector systems and photon imagers based on high-granularity pixel sensors.

- **WP3.3:** 65 nm CMOS and 180 nm SOI CMOS for new mixed-signal integrated circuits with high density and high performance readout functions

WP3 Tasks and Objectives

3.2. 3D Interconnection

- Creation and coordination of a framework to make 3D interconnection technology available for HEP detectors
- Organisation of dedicated fabrication of sensors and electronics optimized for 3D interconnection
- Construction of demonstrator detectors using 3D technology

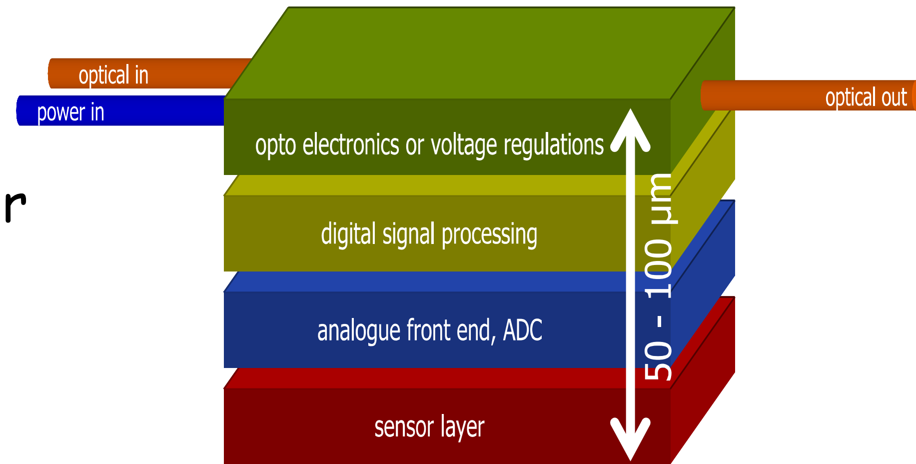
3.3. Shareable IP Blocks for HEP

- Creation and coordination of a framework for the design of low and medium complexity microelectronics libraries and blocks in advanced submicron technologies to be made available to the community of users in HEP
- Organization of the design and qualification of a set of blocks using selected and qualified technologies
- Distribution and documentation of a shared library of functional blocks

3D Interconnection

Vertical integration of thinned and bonded silicon active layers with through silicon vias (TSV) for interconnection

3D integration has the potential to address the extreme performance requirements of future pixel detector applications (smaller pixels, 4-side buttability, integration of dissimilar technologies)



WP3.3 organized itself in subprojects exploring different approaches to 3D integration in terms of the minimum allowed pitch of bonding pads between layers and of TSVs across the silicon substrate.

Some of the initial goals changed during the course of AIDA. The evolving landscape of viable 3D technologies and of available CMOS processes led some groups to redefine their scope and to pursue alternative paths.

Even not fully achieving their individual goals, WP3.3 subprojects widely explored the current status of 3D integration, providing valuable information to our community in view of future detector projects.

WP3.2: 3D interconnection Sub-Projects

1) Bonn/CPPM:
Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).

2) CERN:
Interconnection of MEDIPIX3 chips using the CEA-LETI process

3) INFN/IPHC-IRFU:
Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others)

4) LAL/LAPP/LPNHE/MPP:
Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.

5) MPP/GLA/LAL/LIV/LPNHE:
Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.

6) Barcelona
use a 2-tier approach to increase the fill factor of APD-sensors (based on Tezzaron/Chartered)

7) RAL/UPPSALA
Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV, including redistribution of I/O connections to the backside for a 4-side buttable device.

3D integration in WP3.2

- 3D integration of heterogeneous layers: interconnection of layers fabricated in different technologies, "via last" technique for Through-Silicon Vias (via fabrication in fully processed CMOS wafers).

- The subprojects planned to explore different options for the pixel sensors (high resistivity fully-depleted detectors and CMOS sensors) and for the readout electronics (130 nm and 65 nm CMOS, 3D integrated circuits)

- Different specifications for the interconnection technologies:

  relatively mature 3D processes for peripheral TSVs and for interconnection:

  as expected, they were the most effective in allowing subprojects to fabricate demonstrators and successfully test them.

  more aggressive 3D processes, low pitch (< 50 μm) for TSVs and interconnections as required to fully exploit 3D potential

  higher level of risk, clear added value in view of future designs of advanced pixels; work done in the 3.2 subprojects shows that there still are issues in terms of reliability, yield, turnaround time

WP3.3: Shareable IP blocks for HEP

Goal : provide IP blocks for analog and digital needs in HEP with full documentation and laboratory tests.

1st set organized by CERN in 65 nm CMOS

Lot of interest in the community triggered by the design of pixel readout integrated circuits for HI_LHC and CLIC; plan to benefit from modern nanoscale technologies by obtaining smaller and more intelligent pixels, more compact digital logic and lower power in front-end chips.

2nd set organized by OMEGA in 180 nm SOI CMOS

for needs in calorimetry, TPC, high speed applications…

65 nm CMOS IP blocks

- CERN signed a contract with IMEC and TSMC for accessing the 65 nm Low Power CMOS process. This allows us to have a free exchange of information between users in the HEP community. A special NDA was distributed by IMEC to interested Institutes and signed. CERN distributed to the community a 65nm design kit tailored to the majority of the typical projects.
- Contract negotiations took a lot of work and a long time, and were concluded in the final year of AIDA. However, WP3 groups started their design work in 65 nm CMOS, and IP blocks were designed and submitted, providing the basis for a common shared library. Test results should be available by the end of AIDA.

CERN:

Pseudo-dual-port SRAM generator

1.2V CMOS I/O pad library

32-channel 12-bit ADC for monitoring (1MS/s)

Bandgap voltage reference circuit

Bonn:

LVDS transmitter with programmable output current (S-LVDS)

LVDS receiver with rail-to-rail input stage

CPPM:

General purpose ADC

Bandgap voltage reference

SEU-tolerant latches

Temperature sensor

INFN:

“DICE” SRAM cell

Bandgap voltage reference

Low-voltage low-power differential link

LPNHE:

Per-pixel FIFO buffer with timestamping

AGH:

Power and frequency scalable 6-bit SAR ADC

Power and frequency scalable PLL

(these AGH blocks were fabricated in a 130 nm technology, with the goal of validating design concepts in view of their implementation on the 65 nm CMOS process)

180 nm SOI CMOS IP blocks

- Electronics needs in calorimeters and TPCs :
  - large dynamic range,
  - high speed,
  - low noise,
  - low offset,
  - need of precise capacitors and resistors, …

- Blocks :

  ADC, TDC, DAC, Bandgap, OTA, Rad-tol memory, SEU resistant flipflop …

- Technology : SiGe or HV SOI
- SiGe still moving a lot => shift to AIDA2
- Choose XFAB SOI 180 nm (SOI --> fast, low substrate noise, low cost, HV capability, latchup free)

WP3 session in the final AIDA meeting

WP3.3 (library of IP blocks)

- Sandro Bonacini (CERN) and Gisele Martin-Chassard (OMEGA) will report about 65 nm CMOS and 180 nm SOI CMOS

WP3.2 (3D interconnection)

- We will hear reports about the activity performed by the subprojects.
- Hans-Günther will give an assessment of the status of the final WP3 deliverable D3.10, which will provide an overview of the results of WP3 work on vertical integration for advanced pixel systems.

Backup slides