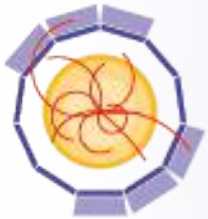

AIDA

Advanced European Infrastructures for Detectors at Accelerators

Timepix readout

Michael Lupberger

University of Bonn

AIDA Final Meeting

December 10 2014, CERN

AIDA is co-funded by the European Commission within the Framework Programme 7 Capacities Specific Programme, Grant Agreement 262025

universitätbonn

Introduction

Subtask 9.2.3 (CEA, Bonn, NIKHEF):
Common **readout systems** for gaseous detectors.
Auxiliary electronics for the read-out of
pixellated front-end chips, aimed at highly granular pixel read-out of **gas detectors**, are to be developed.

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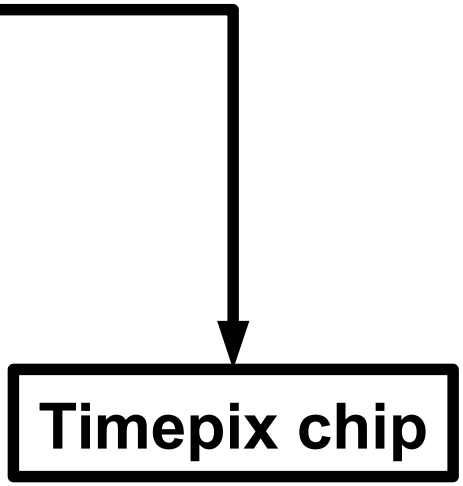

Introduction

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Scalable Readout System (SRS)

Introduction

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Timepix3 chip

Introduction

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Common **readout systems** for gaseous detectors.
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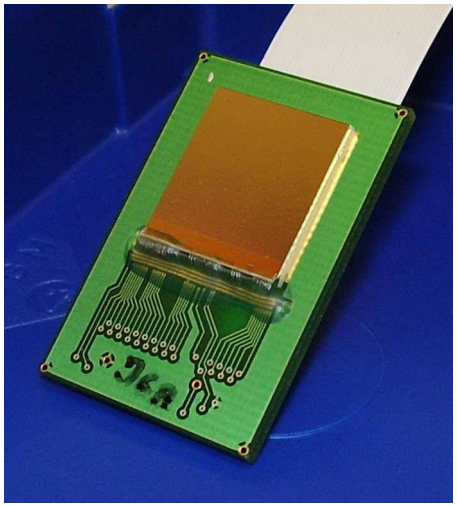
Speedy PIxel Detector Readout (SPIDR)

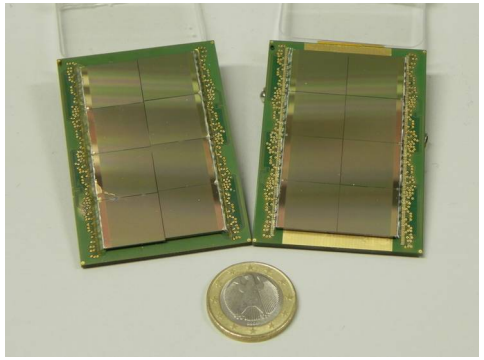
Outline

- *Introduction*
- Timepix Readout
  - Chip
  - SRS
  - Implementation
- Timepix3 Readout
  - Chip
  - SPIDR
  - Implementation
- Summary and Outlook

Timepix

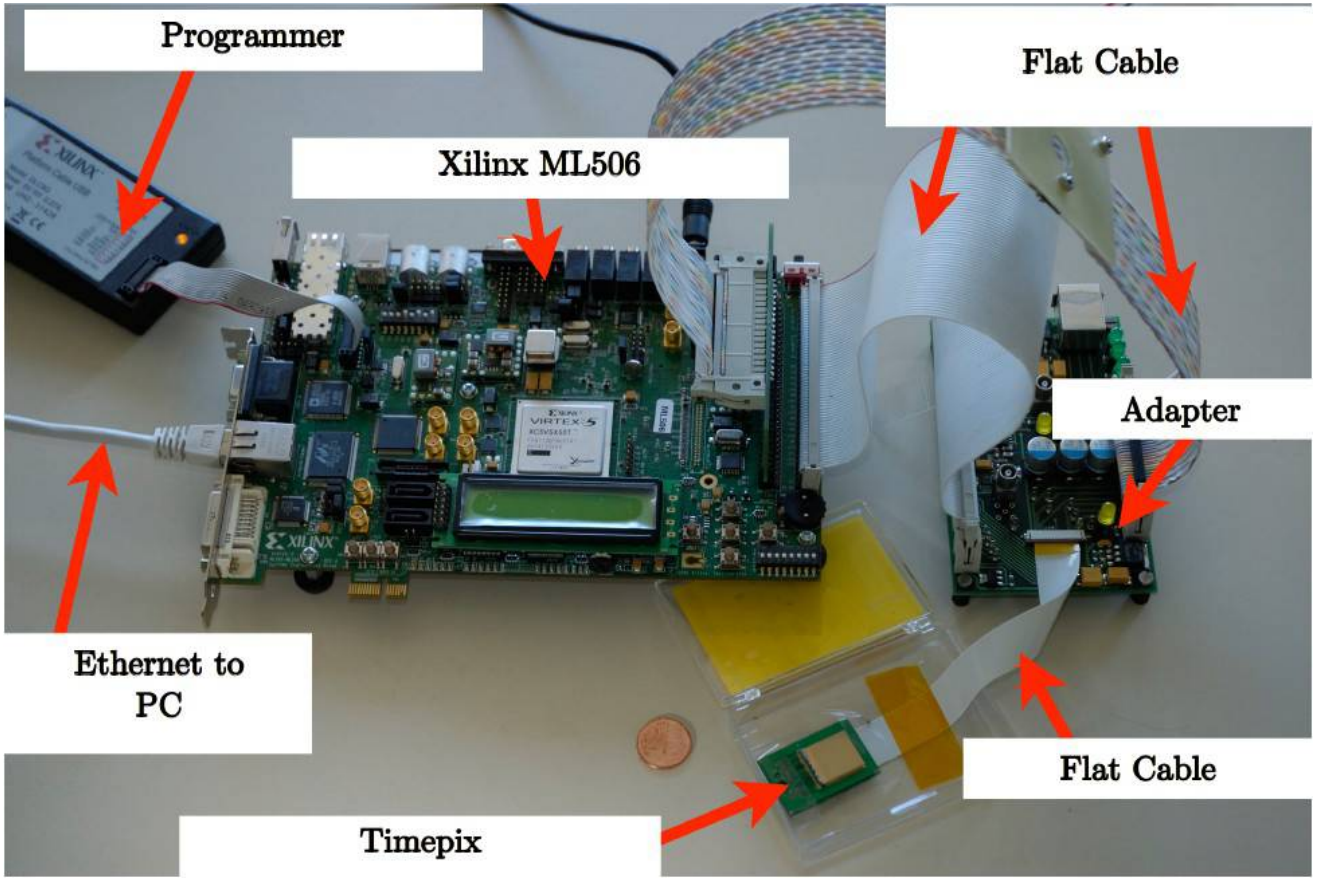


- Universal readout chip
- Properties:
  - Active surface: 1.4 x 1.4 cm²
  - Pixel size 55 x 55 µm² on 256 x 256 array
  - 14 bit counter in each pixel (ToA or ToT)
  - Noise threshold ~500e^- (ENC ≈ 90e^-)
  - Frame based readout (1 Mbit of data)



- Challenges for the readout (2011):
  - (Available) for only up to 8 chips, no scalability
  - Slow readout speed

Starting point 2011

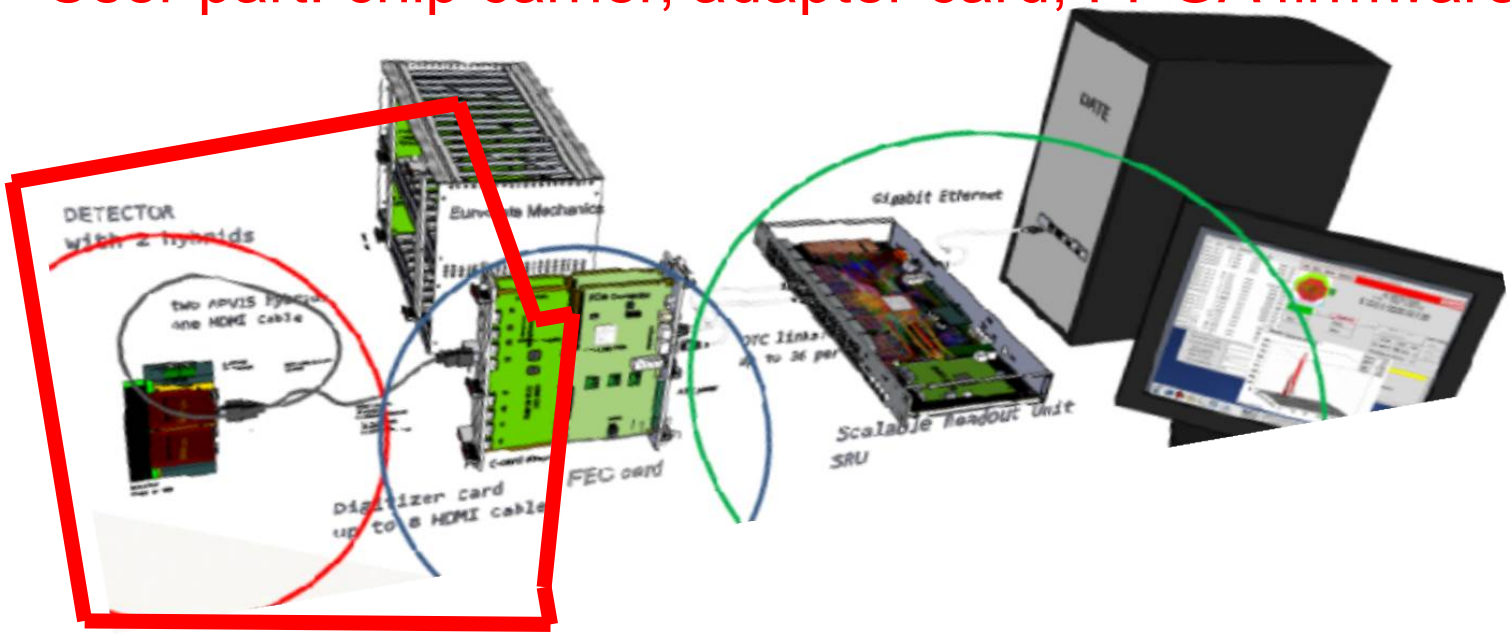


Prototpye system from Mainz

Goal: SRS

Developed within RD51 (OpenSource)

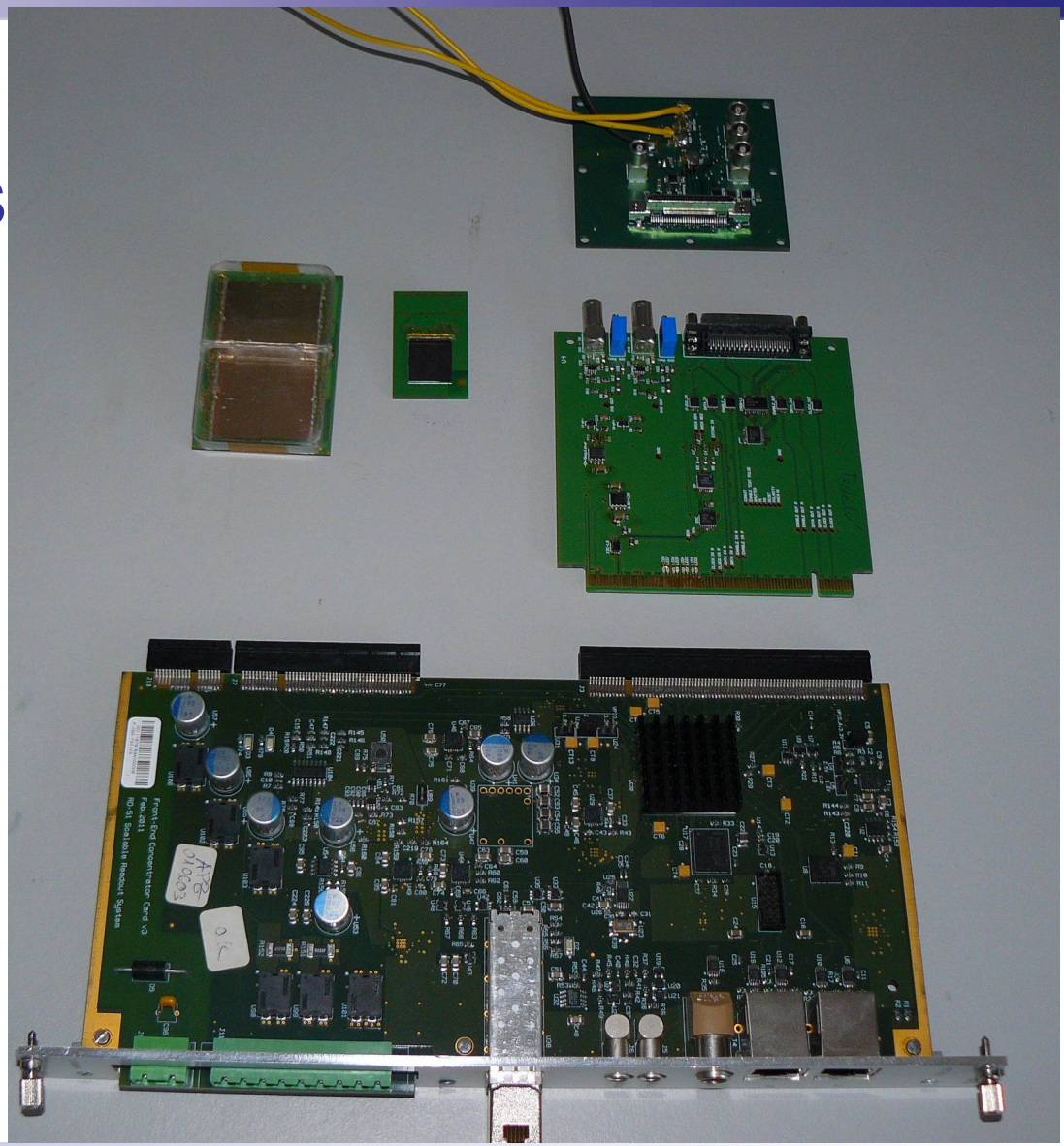
- Provides common hard- and firmware
- Uses cheap standard components
- User part: chip carrier, adapter card, FPGA firmware



SRS

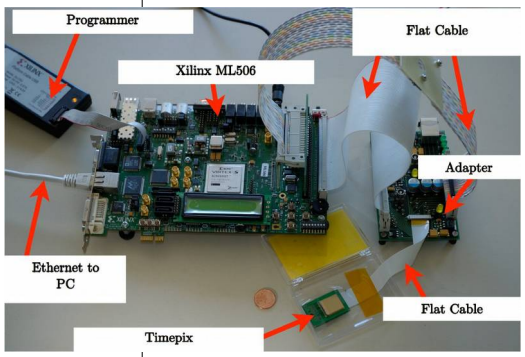
Implementation in SRS

- Single Timepix or Octoboard
- Intermediate board
- A type adapter card
- SRS FEC with Virtex5/6 FPGA
- Ethernet to PC

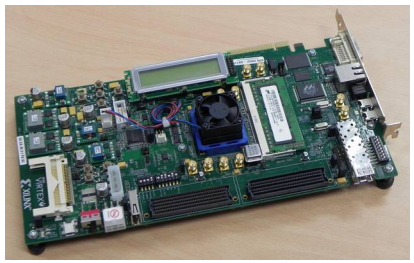


System evolution

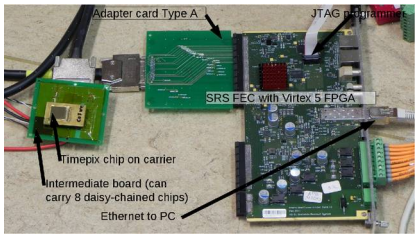
ML506 from Mainz



ML605 evaluation board +VHDCI V1



SRS + VHDCI V1



Testbeam

ML605 evaluation board +VHDCI

√

CAST

SRS + VHDCI

√

Bonn, Helsinki, DESY, Saclay

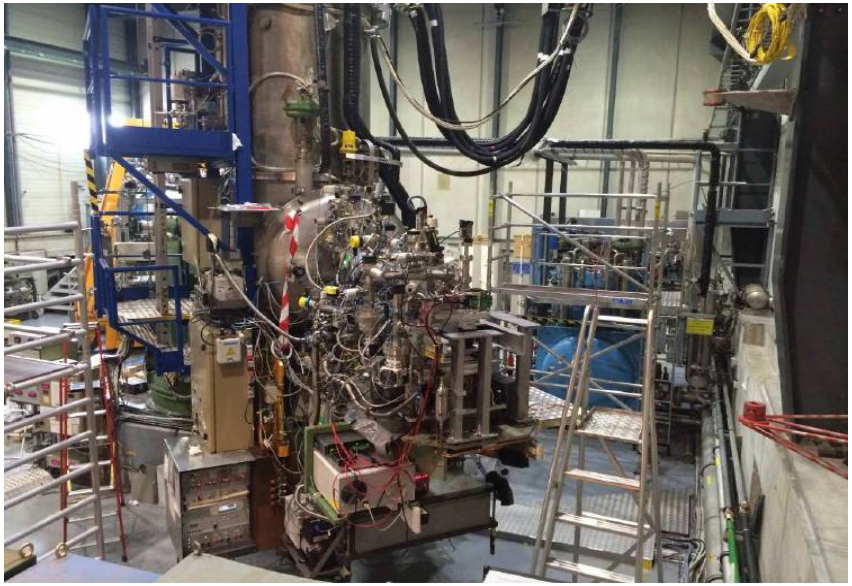
√

SRS V5/6 + HDMI

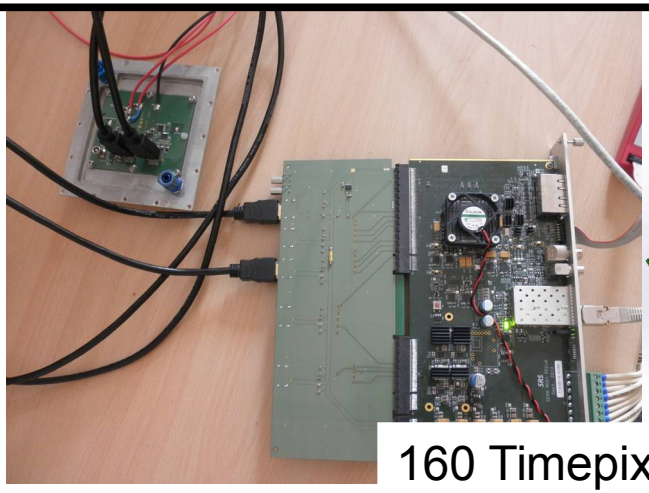
2010 2011 2012 2013 2014

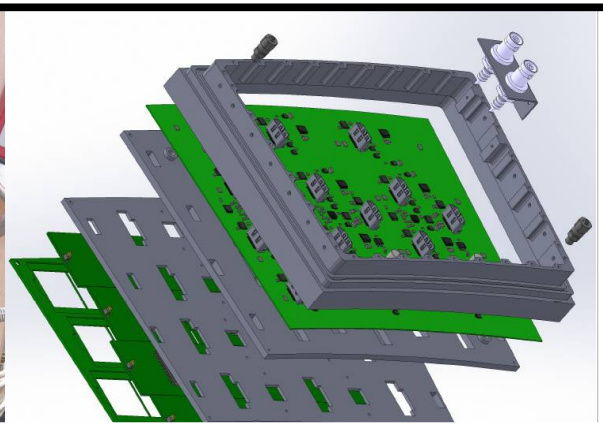
Highlights

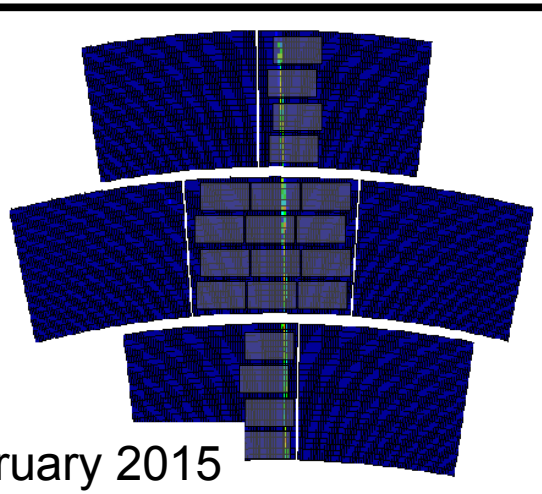
System verification at DESY testbeam 2013



Timepix readout at CAST 2014 run period







160 Timepix chip detector testbeam in February 2015

Timepix3

- Available since September 2013

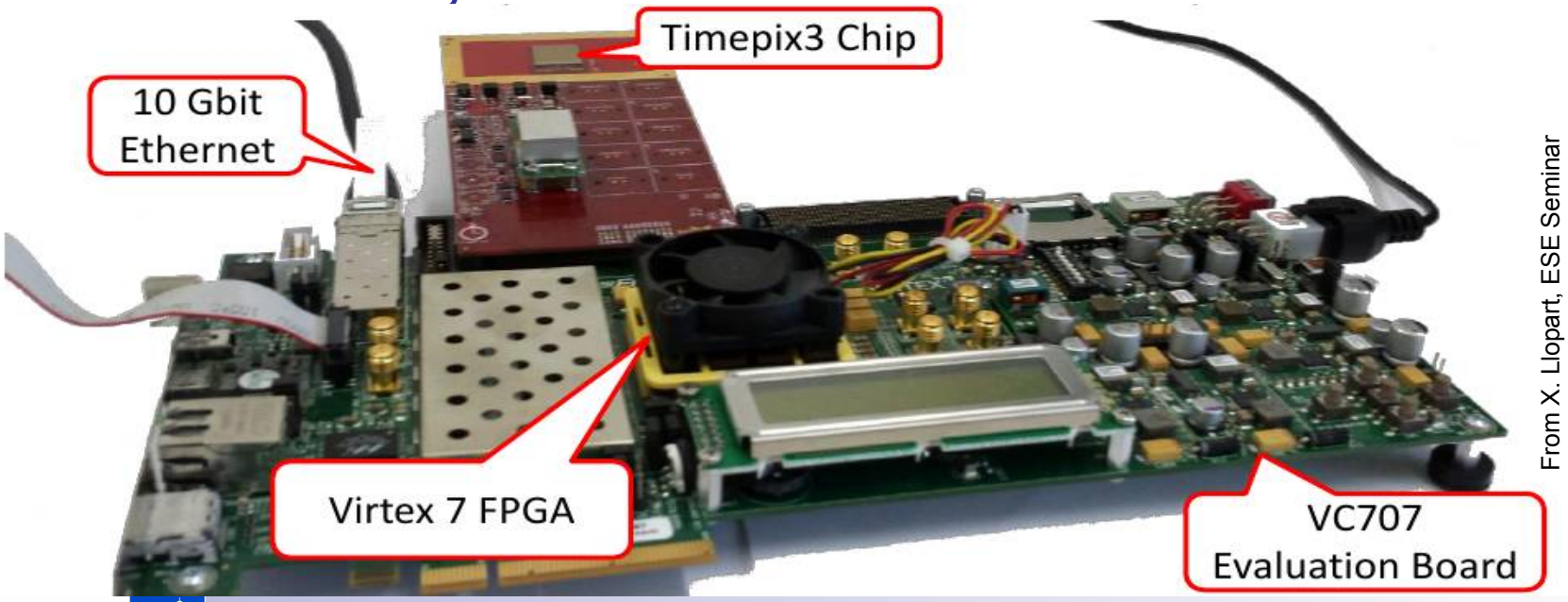
	Timepix	Timepix3
Pixel matrix	256 x 256	
Pixel size	55 µm x 55 µm	
Technology	250 nm CMOS	130nm CMOS
Readout	1. Frame based	1. Data driven 2. Frame based
Zero suppression	no	yes
Acquisition modes	1. Charge (TOT) 2. Time (TOA) 3. Event counting	1. TOT and TOA 2. TOA 3. Event counting and TOT

- Challenges for readout
  - Not available
  - High data rate: 5.12 Gbit/s

SPIDR

NIKHEF

- Speedy PIxel Detector Readout
- Based on Xilinx evaluation board (Virtex7 FPGA)
- 10 Gbit/s Ethernet
- Timepix3/Medipix3 adapter card on FMC connector
- Software library



From X. Llopart, ESE Seminar

SPIDR

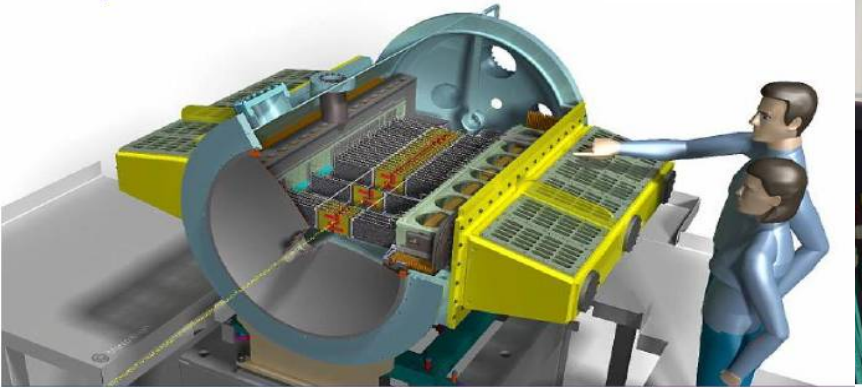
NIKHEF

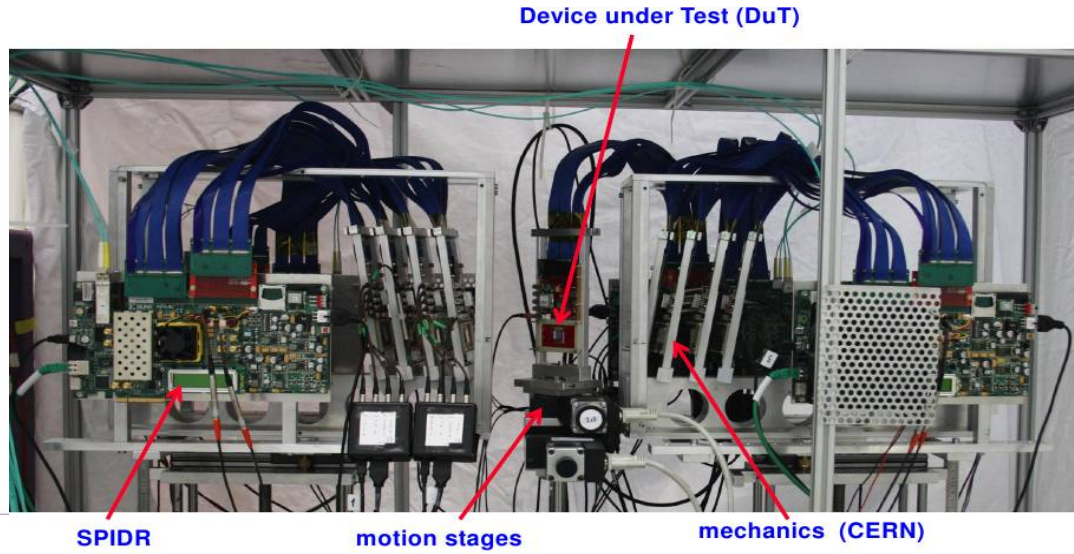
- NIKHEF Timepix3 adapter board
- CERN Timepix3 chip carrier and adapter board to FMC

From X. Llopart, ESE Seminar

Highlights

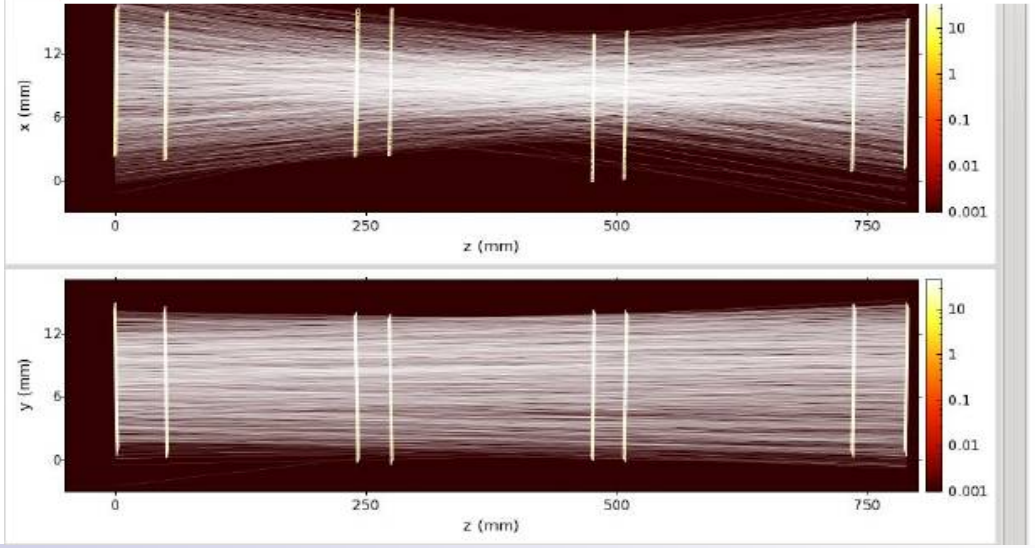
Timepix3 → LHCb VeloPix





July 2014: testbeam at PS

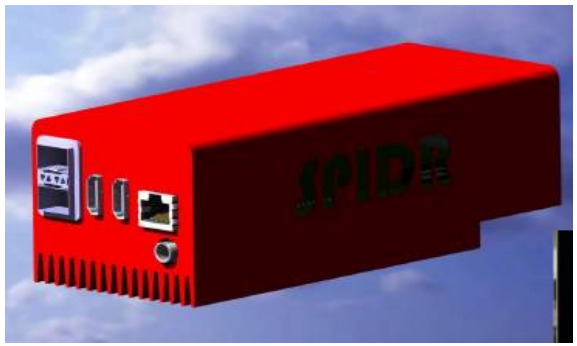
Timepix3 telescope, Timepix3 as DUT, 4 SPIDR readouts

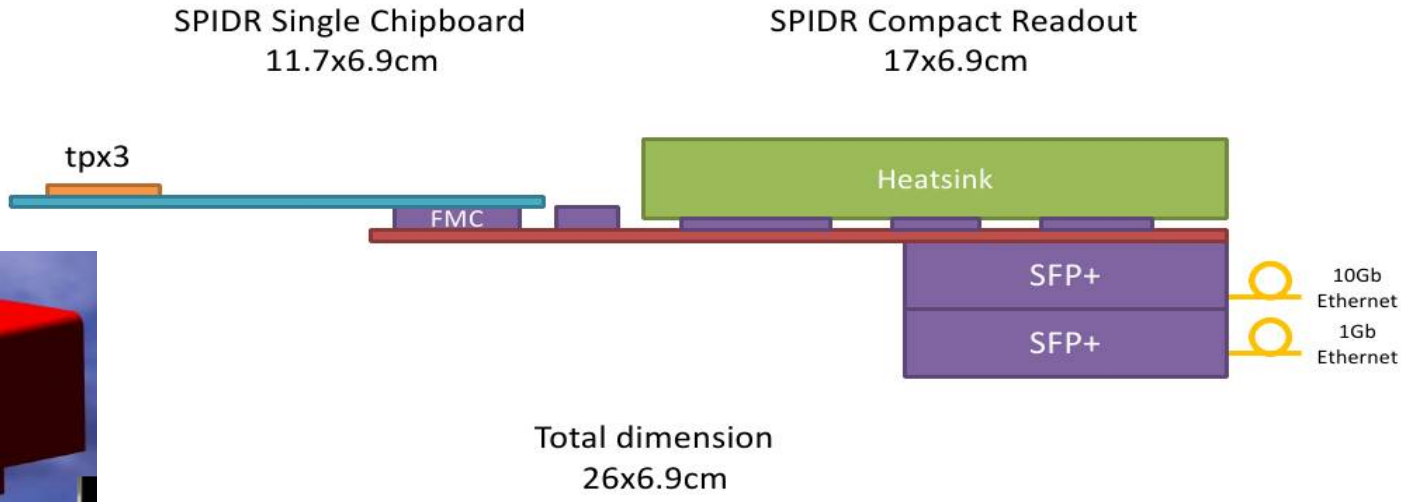


Compact SPIDR

NIKHEF

- Dedicated board with FPGA, FMC plug, 10Git/s and 1 Gbit/s Ethernet
- Prototype finished, 3 boards in production





AIDA contribution

- MS 41: Intermediate state (Month 23) √
- D9: Deliverable (Month 40) √

- Estimated indicative person-months: 27 √
- AIDA financial contribution as requested √
- Financial contribution from institutes as required √

Summary

- Subtask 9.2.3 successfully finished

- Readout for two pixellated front-end chips:
  - Timepix: small system on Xilinx evaluation board
    integration in SRS for larger systems
  - Timepix3: SPIDR on Xilinx evaluation board
    compact SPIDR on small dedicated PCB
- Demonstration of readout in testbeam
- Systems are used in experiments
- Advancements ongoing

Thanks

People in Subtask 9.2.3:

- NIKHEF: Nigel Hessey, Martin van Beuzekom, Jan Visser, Bas van der Heijden
- CEA Saclay: David Attié, Paul Colas
- Uni Bonn: Klaus Desch, Jochen Kaminski, Michael Lupberger