Remaining Projects

1) CERN (M. Campbell)

2) RAL/Uppsala (R. Brenner)

3) INFN/IPHC-IRFU (M. Kachel)

4) Bonn/CPPM

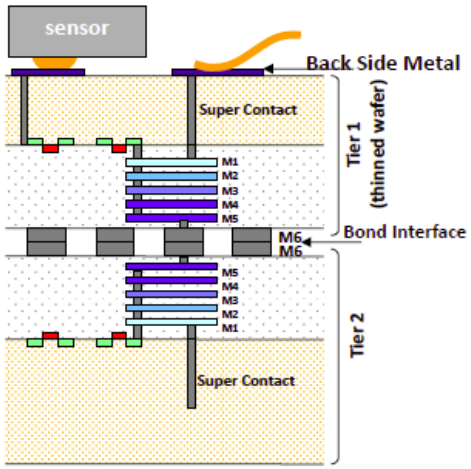
5) LAL/LAPP/LPNHE/MPP

6) MPP/GLA/LAL/LIV/LPNHE

7) UB

Bonn/CPPM

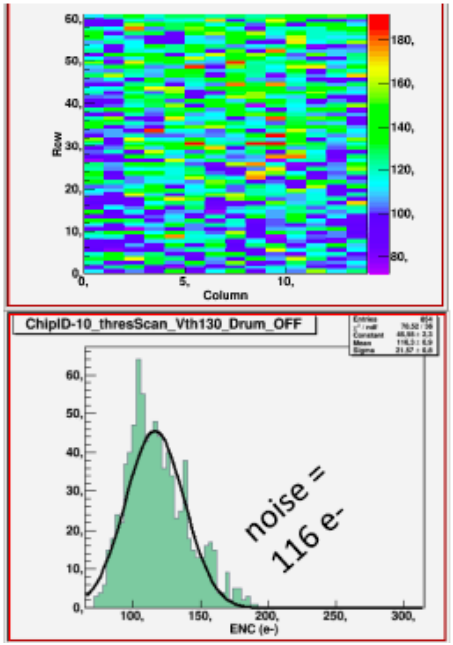
Test of a 3D version of the ATLAS FEI4 ASIC
Tezzaron via middle (first) technology
High density low diameter vias



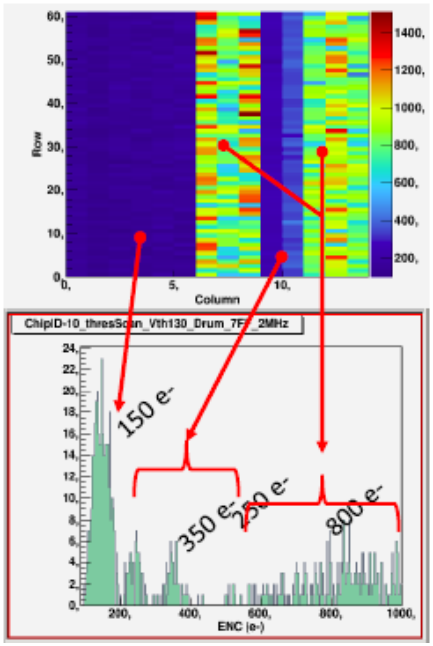
Chip works with a performance similar to the original FEI4

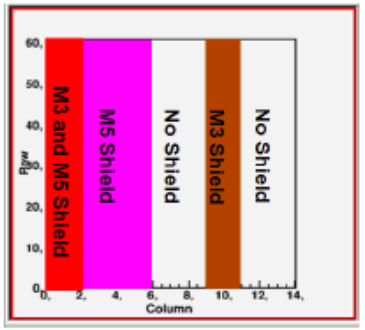
- 11 noise generators to inject noise in the analog pixel
- Different shielding configurations implemented column wise

Noise map - Drums OFF



Noise map - Drums ON





- A shielding is necessary.
- Shielding with only M3 is not enough efficient.
- Shielding with Metal 5 appears to be the best solution.

Bonn/CPPM

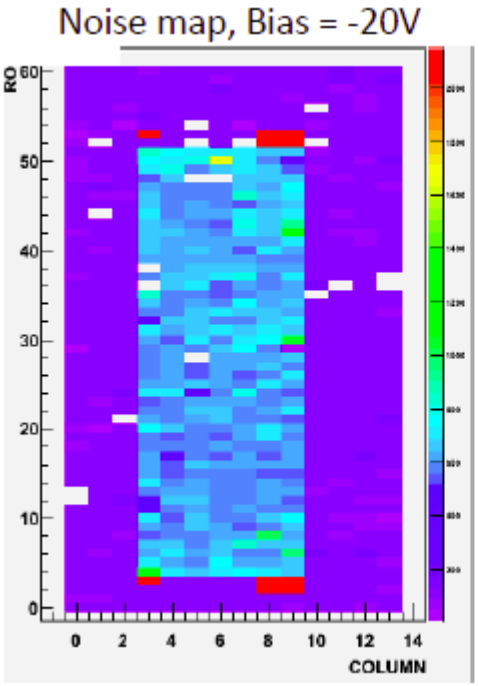
Assemblies with sensors under study

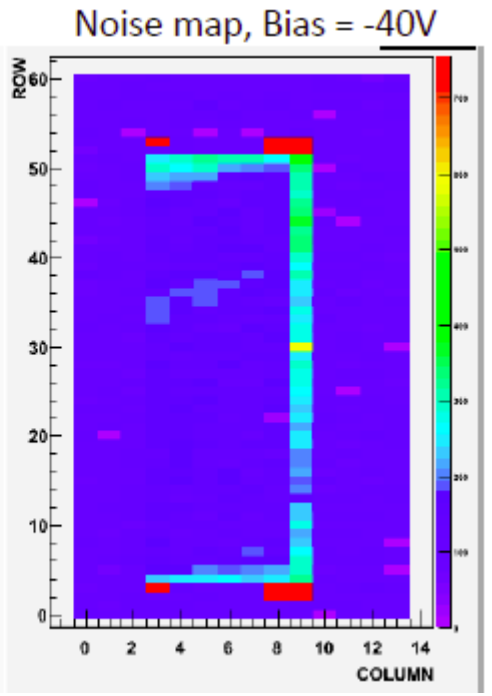
First results:
Connection to sensor successful (noise decreases with increasing bias voltage)

Conclusion:

Tezzaron 3D technology works

However:
Long production time (5 years)
Low yield





Bonn/CPPM

Pre-study:
Via last TSV in thinned (90µm) ATLAS FEI2/3 chip
TSVs in periphery for backside connectivity

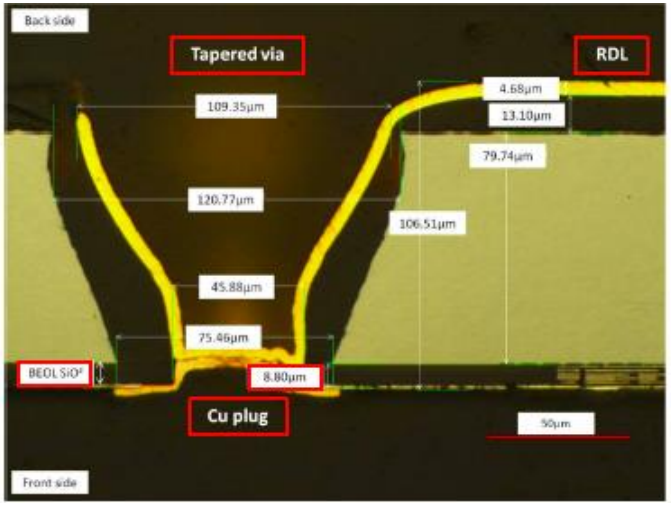
Tapered vias of 100µm diameter & RDL
(redistribution layer on backside)
Processed by IZM, Berlin

Successful connection to sensors (standard flip chip to planar sensor)

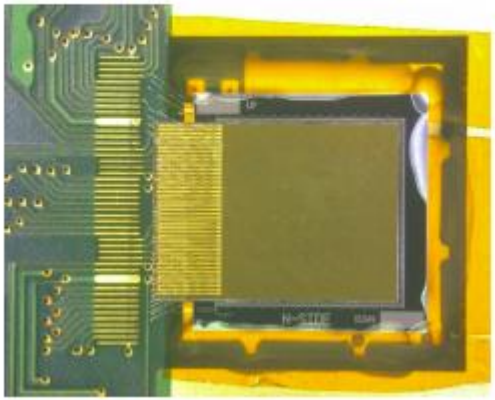
No loss in performance compared to modules without TSV

Problems with bonding of thinned ASICs
(chips bowed => corners lift off)

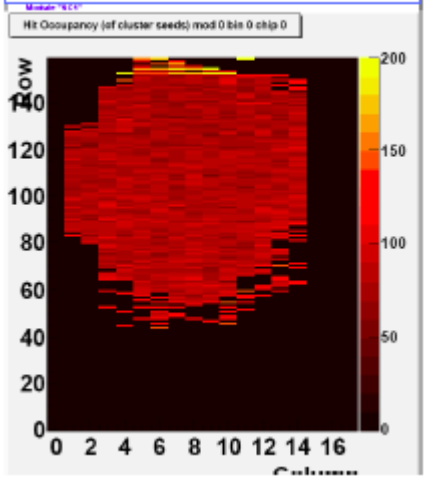
Frontside processing needed



Module on board



Am-241 source



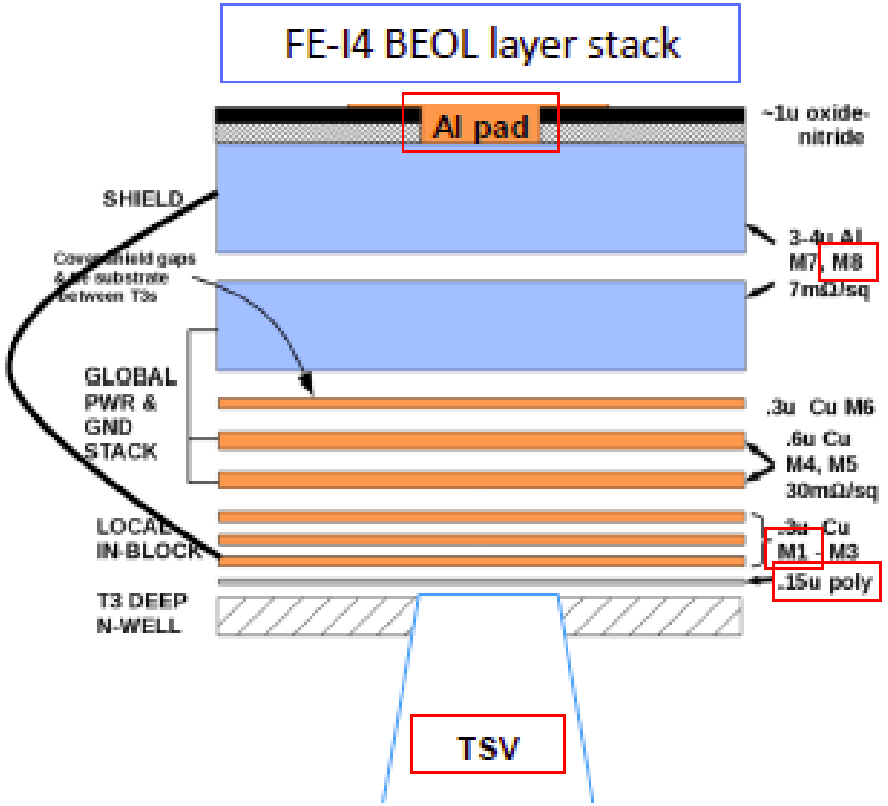
Bonn/CPPM

Extension to FEI4
Modification to avoid frontside processing: Metal 1 connected to I/O pad
Sufficient to etch TSV from backside to metal 1

Three wafers are at IZM for processing

Thinning to 150-200 µm (avoid bowing) &
Improved flip chip bonding (handle wafer)

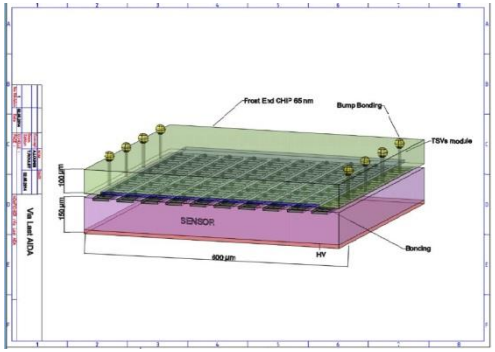
In work, first results till February?



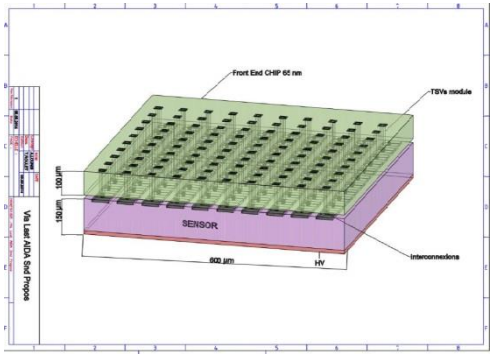
LAL/LAPP/LPNHE/MPP

Initial goal: 3D interconnection of 65nm ASICs at CEA-LETI

Conservative:
I/O vias at periphery



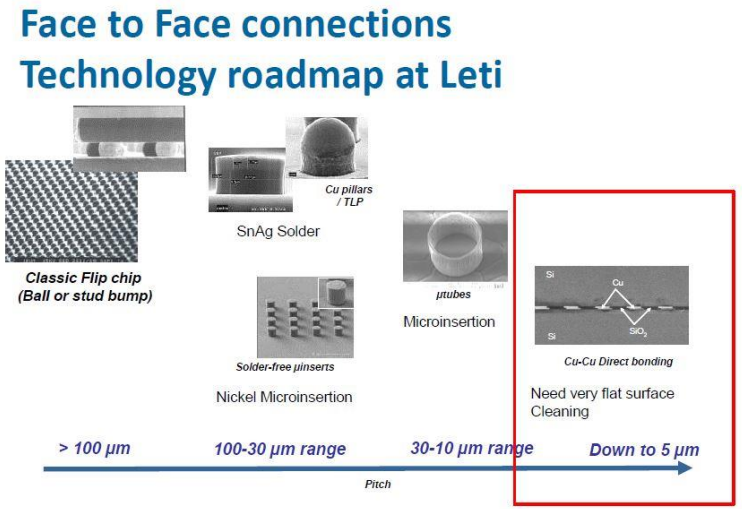
More challenging:
High density pixel
by pixel TSVx



Sensors available for the project
5 x 5 mm² with 35 x 200 µm² pixel

Slim edge/edgless from CIS and VTT

Delayed due to late contracting of 65nm process at CERN



LAL/LAPP/LPNHE/MPP

Alternative project:

Interconnection of TEZZARON version 3D of OMEGAPIX with CEA-LETI solder bumps

Expected end of December

The context of this proposal is to realize a flip chip assembly of a novel ASIC chip (OMEGAPIX) on a silicon chip detector (IBL) for evaluating the performances of this new device for high energy particles detection at CERN. The ASIC OMEGAPIX technology is based on a 2 tiers partitioned 3D chip made by Tezzaron. The already singulated ASIC chips are not prepared to perform flip chip assembly at this stage and are terminated with standard aluminum pads. In this configuration the flip chip assembly is not possible and requires the realization of a solder interface at the die level on the ASIC chips.

The objectives of the proposal are:

- To form a solder interface on top of the OMEGAPIX chip
- To supply two flip-chip stacked assemblies of OMEGAPIX ROIC on IBL sensor dies.

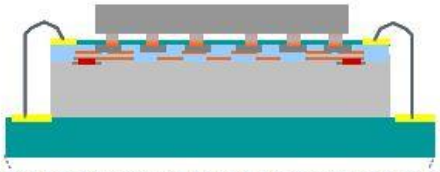


Figure 1 : schematic of the flic chip assemby of the ASIC OMEGAPIX chip on the IBL sensor chip

The specifications and the requirements for this project are detailed below:

- Project requirements :
  - 8 OMEGAPIX test chips with Alu pad, chip thickness = 300 µm (tbc)
  - 2 OMEGAPIX functional chips with Alu pad, chip thickness = 300 µm (tbc)
  - 2 IBL functional chips with UBM Ti/Ni/Ag pads, chip thickness = 280 µm
- OMEGAPIX solder interface realization
  - Electroless selective deposition of UBM Ni/Pd/ Au layer on Al pad
  - Single chip solder balling compatible with fine pitch placement (< 60 µm)
- Flip chip technology
  - Flux dipping of top die (omegapix)
  - Pick and Place with high precision automated equipment (datacon or equivalent)
  - In Situ soldering by thermo-compression
  - Reflow of the solder

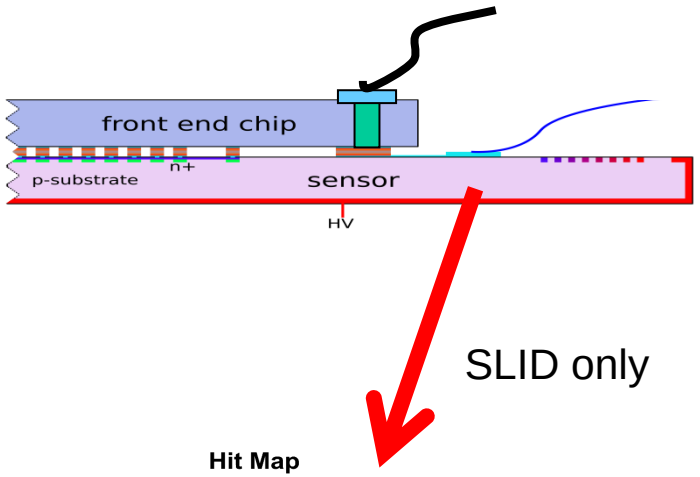
MPP/GLA/LAL/LIV/LPNHE

Pre-study:

Via last TSVs in periphery of FEI3 for backside connectivity
Similar to Bonn/CPPM
However:

- Small vias (3 x 10 µm)
- SLID interconnection (bumpless)

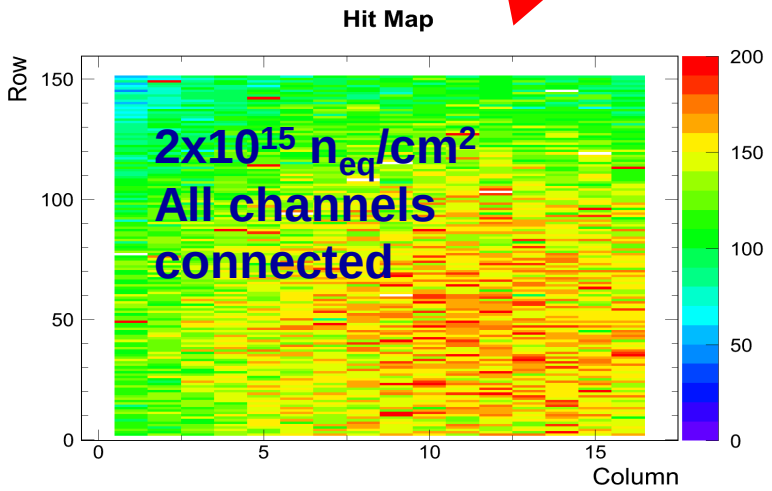
⇒ Potential for high density interconnection (20µm pitch)



Processed by Fraunhofer EMFT, Munich

❑ Good Charge Collection efficiency after irradiation up to 10^{16} n_{eq}/cm^2

❑ Number of unconnected channels stable after irradiation and multiple thermal cycles (+20°C → -50°C)



SLID interconnection is radiation hard and withstands thermal cycling

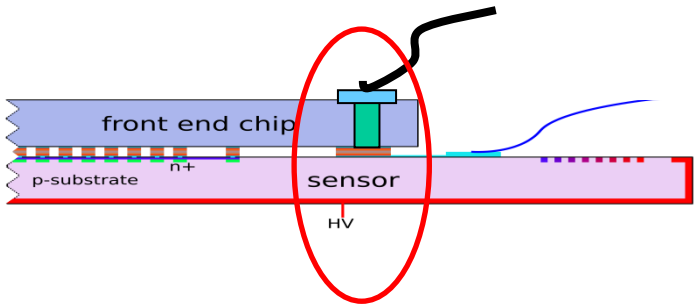
MPP/GLA/LAL/LIV/LPNHE

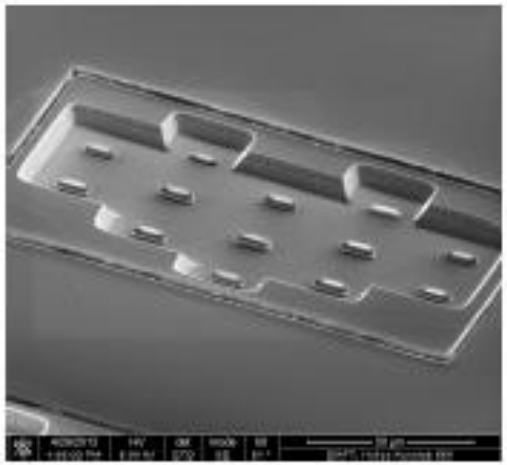
SLID interconnection works fine

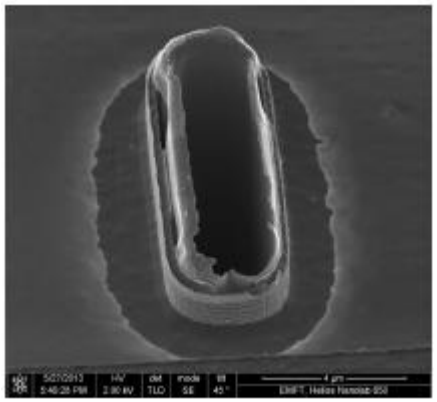
⇒ Next step TSV etching

1) Tungsten filling of vias failed (no connectivity)

2) ASIC damaged by via processing (too high currents)







MPP/GLA/LAL/LIV/LPNHE

Extension to FEI4: narrow vias

Unlike in FEI3 no etching from frontside possible
Etching from backside to metal 1

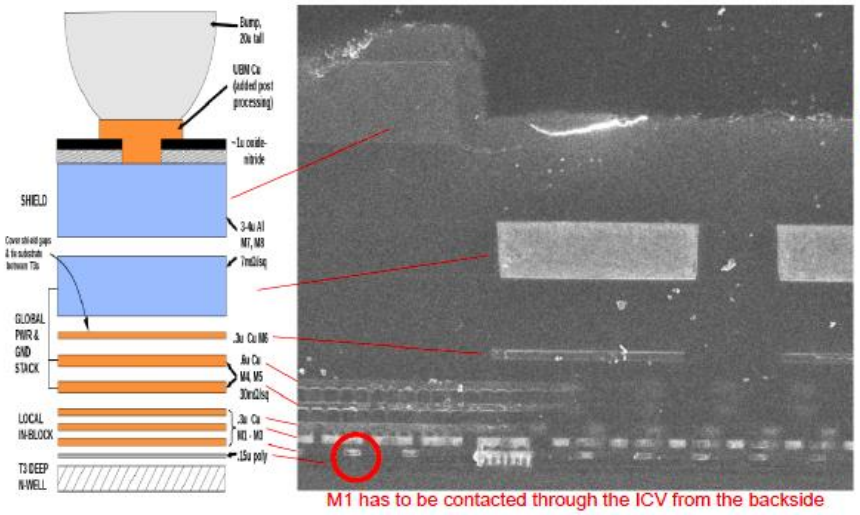
Unlike in the similar Bonn/CPPM it is nor easy to etch to metal 1 in narrow, cylindrical TSVs:
Problems to remove SiO2 and poly layer under metal 1.

Solution: local thinning to reduce aspect ratio.

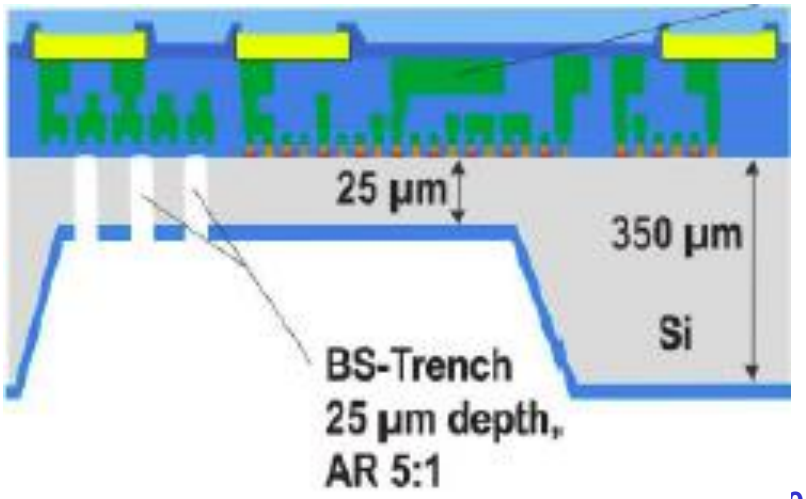
The project hast started and masks are produced, but no results yet (in work).

Conclusions:

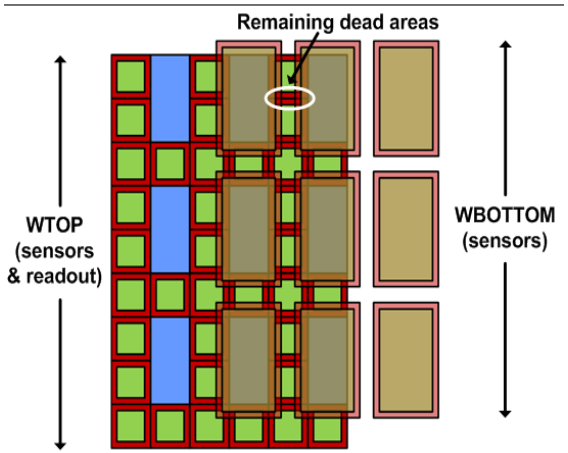
Processing of via last high aspect ratio vias is difficult. technical problems encountered at EMFT lead to considerable delays.

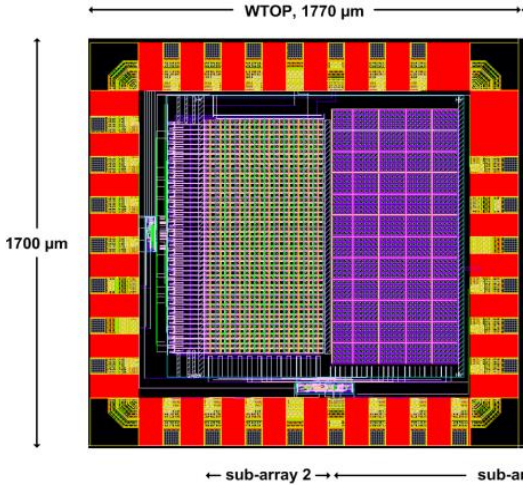


M1 has to be contacted through the ICV from the backside



UB





Geiger APDs in CMOS have been demonstrated by UB
Normal pixel arrays with Geiger APDs have considerable dead area
Can be overcome using a double layer (need for high density interconnection)
UB designed an array of 48 rows x 48 columns with 96% of fill-factor
The array is operated in the time-gated mode with passive quenching and active recharge

Unfortunately there has been no opportunity to submit with Tezzaron

Status of D3.10

AIDA

CAPACITIES

Grant Agreement No: 262025

AIDA

Advanced European Infrastructures for Detectors at Accelerators

Seventh Framework Programme, Capacities Specific Programme, Research Infrastructures, Combination of Collaborative Project and Coordination and Support Action

DELIVERABLE REPORT

ASSESSMENT OF 3D INTEGRATED SENSORS

DELIVERABLE: D3.10

Assessment

The 'assessment' should not be limited to detector performance (compared to traditional devices) but also take into account the process of R&D and production:

- cost, processing time
- technological challenges
- experience with industry and vendors
- difficulties encountered
- yield
- recommendations for further R&D

Each subproject writes a report on its own project.
The report should cover the items mentioned above.

We then prepare a phone meeting about 2 weeks later to discuss the reports

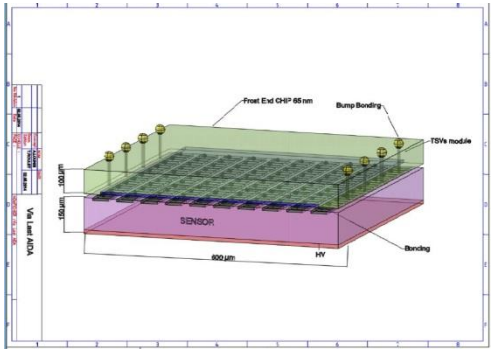
Prepare draft report. **In work, to be circulated soon**

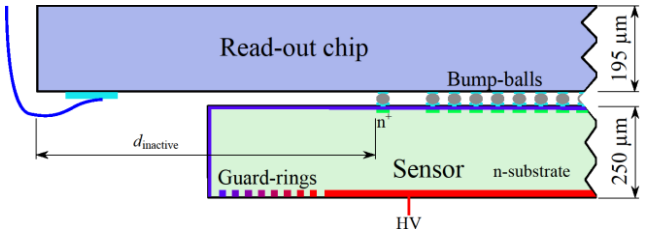
We will have a discussion in during the AIDA meeting at CERN (December 9-11).

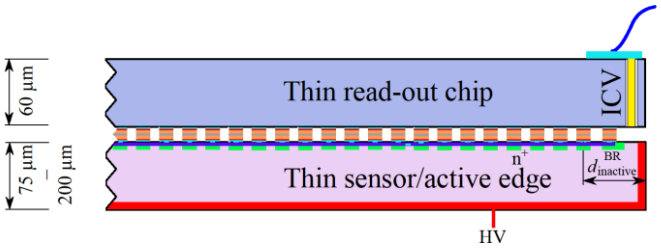
Project Overview

3D interconnection be used twofold

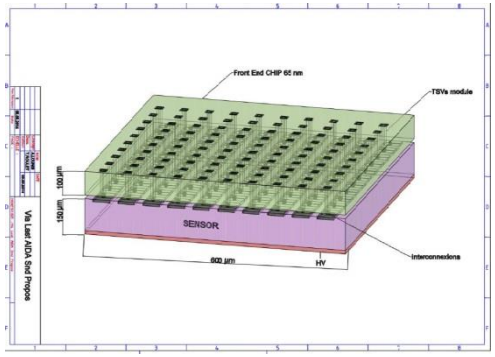
- Use TSV for backside connectivity in order to reduce dear areas
  needs few TSVs on chip periphery
  only large diameter, low aspect ratio vias needed (>50 µm, 2:1)
  Chip sensor interconnection by solder bump bonding
  (>50 µm pitch)







- Use TSVs to interconnect different ASIC layers to reduce pixel size (keeping functionality)
  needs TSVs in each pixel (many
  small diameter, large aspect ratio vias needed (<25µm, > 5:1)
  high density interconnection needed (bumpless)



Projects

project	TSV	Interconnect	Intermediate results	Final module	comment
Bonn/CPPM	Large/periphery	Solder bumps	Vias ok	In work	
CERN	Large/periphery	Solder bumps	Ok	Ok	Fully accomplished
INFN/IPHC	Small, pixel (Tezzaron process); not investigated with IMS	SLID (Fraunhofer IMS), microbumps (T-Micro)	Several	In work	Project change due to Tezzaron delay Administrative problems with IMS
LAL/….	None (high density vias in OMAGAPIX 3D)	Solder bumps		December 2014?	Originally TSMC 65nm (late). Use Tezzaron Omegapix instead
MPP/….	Small/periphery	SLID	SLID ok Vias failed	Mask designed	Delayed due to technical problems at EMFT
UB	Small, pixel	Cu-Cu (Tezzaron)	-	-	Tezzaron process unavailable
RAL/Uppsala	Small/pixel	SLID	SLID ? VIAS ?	In work	Delay due to administrative & technical problems

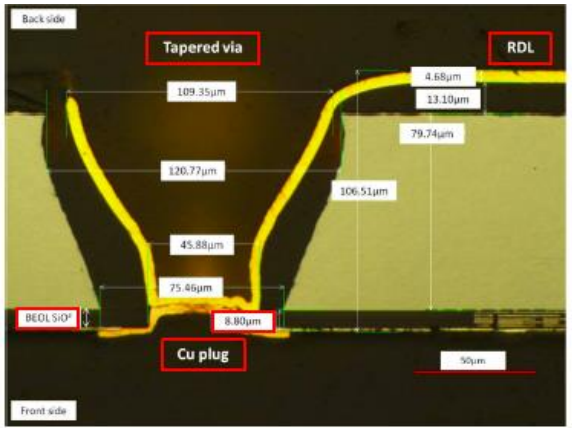
Conclusions: mature technologies

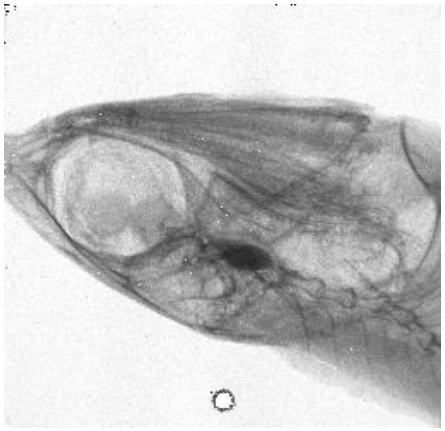
Large diameter TSVs with bump bonding interconnect (CERN, Bonn): the projects either achieved the goal (CERN) or could show successful intermediate results (Bonn).

It could be demonstrated that the goals (backside I/O) can be achieved without compromising the performance of the ASICs.

Can be used with standard ASICs (with slight modifications to allow access of via to I/O).

CEA-LETI Process openly available.





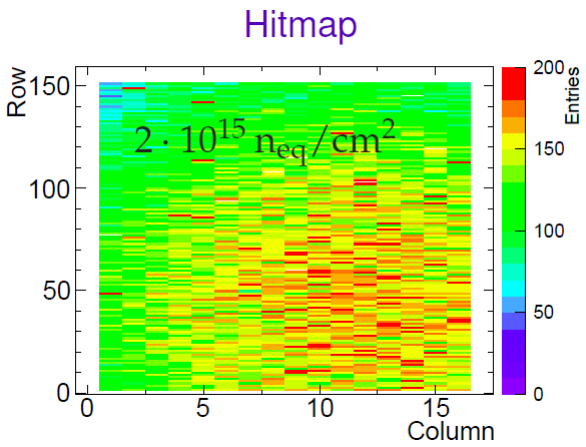
Conclusions: challenging technologies

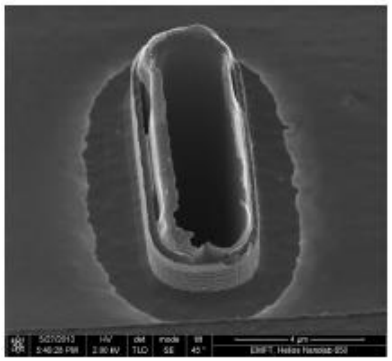
Not unexpected those projects (INFN/IPHC, MPP; LAL, RAL/Upps, UB) had more difficulties.
None achieved the final goal (yet) but some ntermediate results could be obtained:

High density interconnections (SLID, T-Micro) work

TSVs: while RAL/Uppsala seemed to have got working TSVs from EMFT, the MPP project with EMFT failed in this respect. May be bad luck, but it could tell us something on the maturity of the process.

Tezzaron: Some chips could be produced and seem to work properly (from projects started before AIDA). However, the process became virtually unavailable (and probably still is) when AIDA projects needed it. UB hat to stop completely. Others (INFN/IPHC) had to look for alternative which caused considerable delay.





Schedule for D3.10

Status

- Reports from the various subprojects exist
- Based on these reports a first draft is being drafted (90% complete)
- I first version will be circulated before X-mas.
- Final version expected end of January

Do do:

- More results should show up till January
- Need more information on the performance of the 3D assemblies compared to the 2D versions
- Direct comparison of pros & cons of the subprojects
- Shall we report on the administrative problems some subprojects had and caused delays?
  Since this is an EU project and should foster international projects within the EU I think: yes.
- Include information from outside AIDA ?