AIDA
(mini) Trigger/Timing Logic Unit
(mini TLU)

Introduction

Status

Plans

Summary

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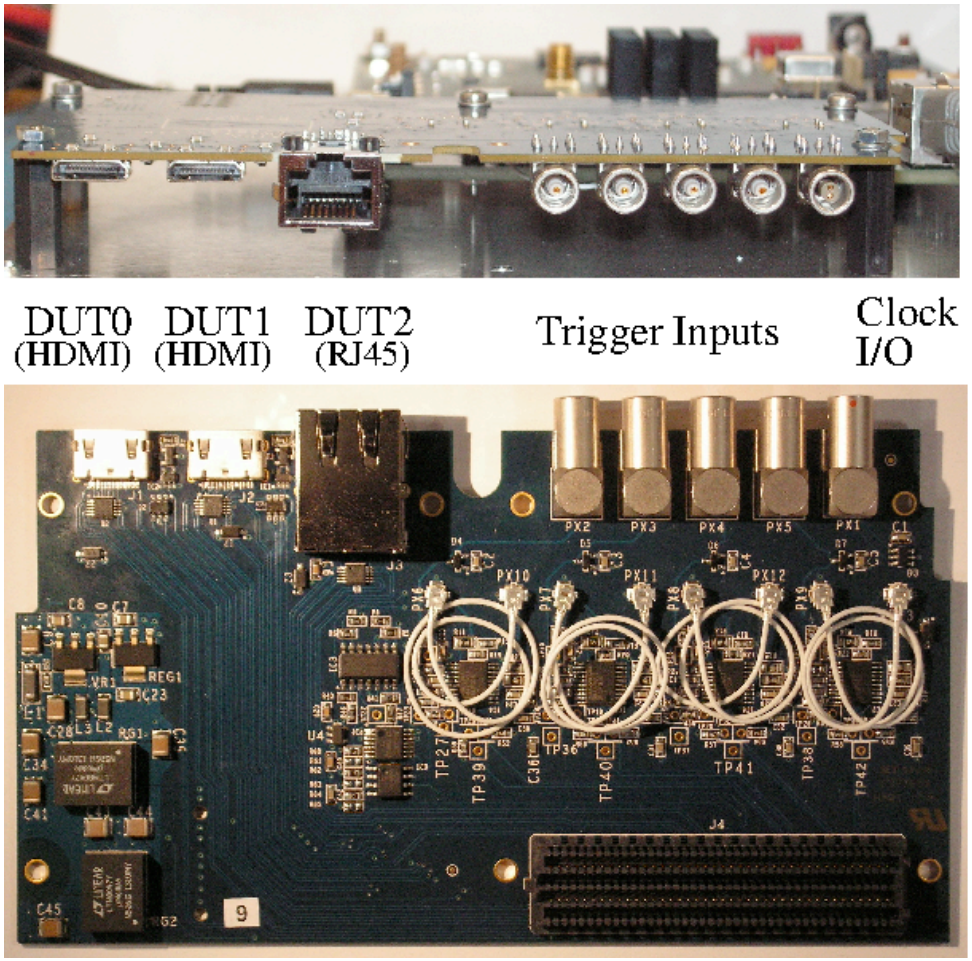
Introduction

- Provide Simple Timing/Synchronisation Interface
  - Builds on EUDET TLU
  - Linked with Deliverable D8.2.2 (specification documents for the common DAQ)
- New for AIDA – synchronous mode (clock/ trigger/busy) for high trigger rate
- Better performance than EUDET TLU
  - Trigger rate > 1MHz sustained , > 10MHz instantaneous

Hardware

- Implemented as FPGA Mezzanine Card (FMC).
- Plugs into off-the-shelf FPGA carrier
- Four trigger inputs
  - Software adjustable threshold
  - Threshold and CFD
- Three Device Under Test interfaces
  - Can be fanned out to up to 30 DUT interfaces in synchronous mode with external fanout.
- Open Hardware, Open Firmware: http://www.ohwr.org/projects/fmc-mtlu/wiki



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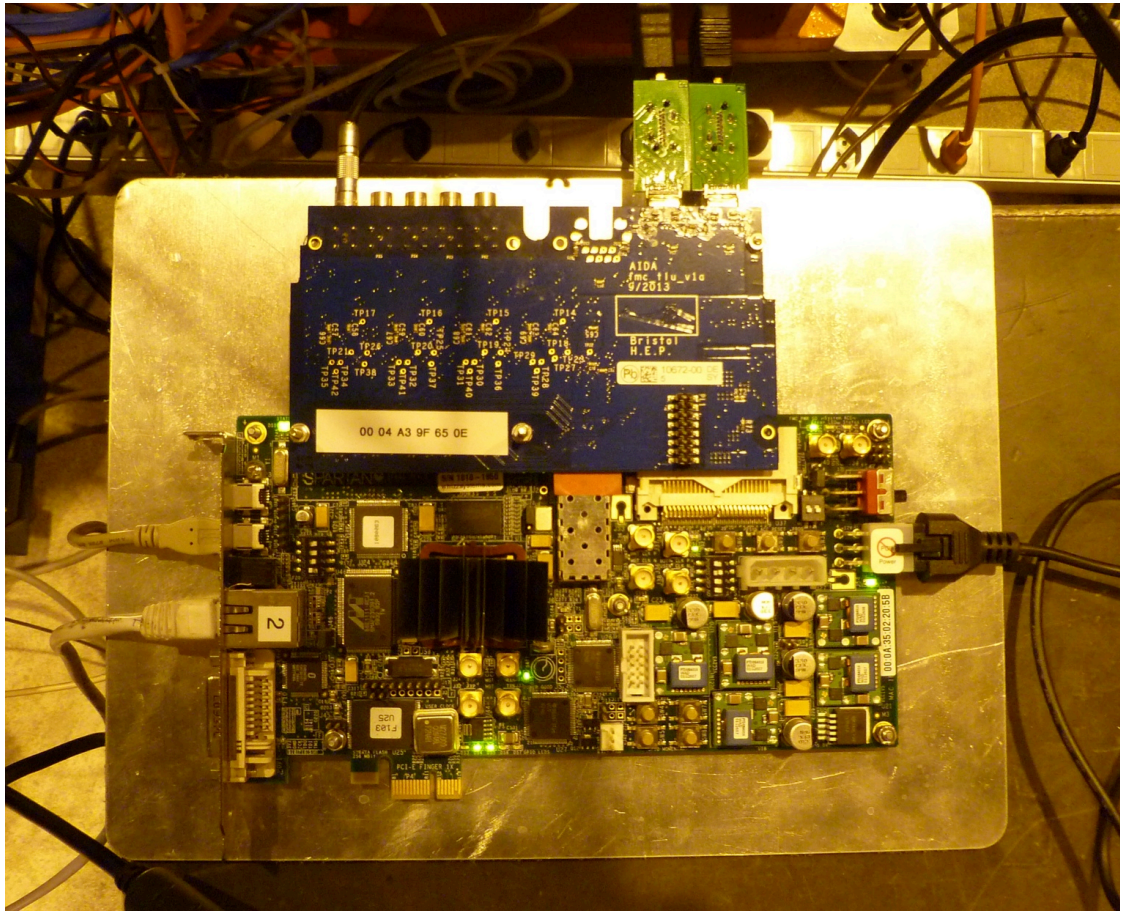
Hardware

- Currently only as boards bolted to plate
- Design for box in progress



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Hardware

- LVDS → TTL converters exist.
- This example from NIKHEF

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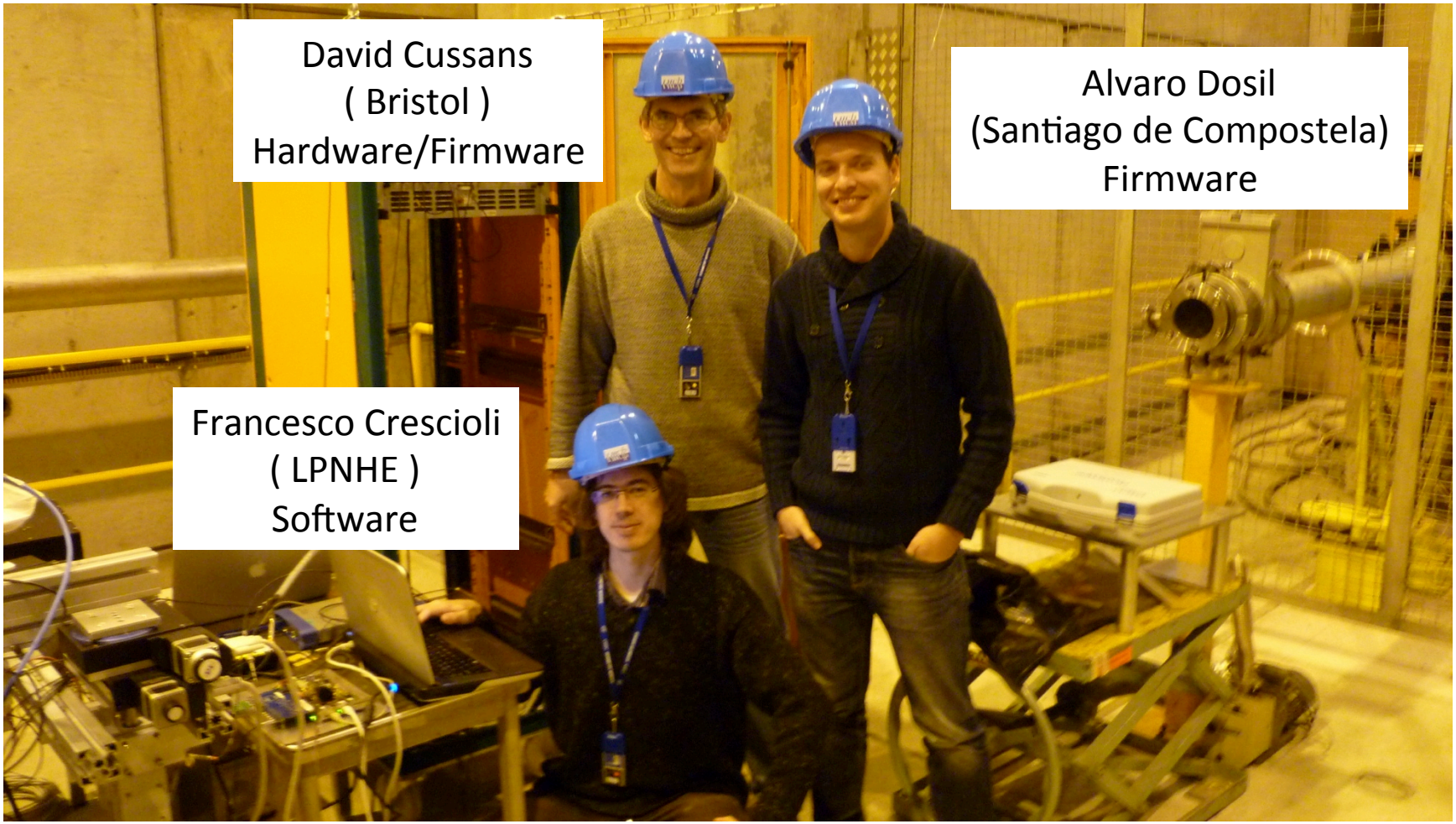
Development Team



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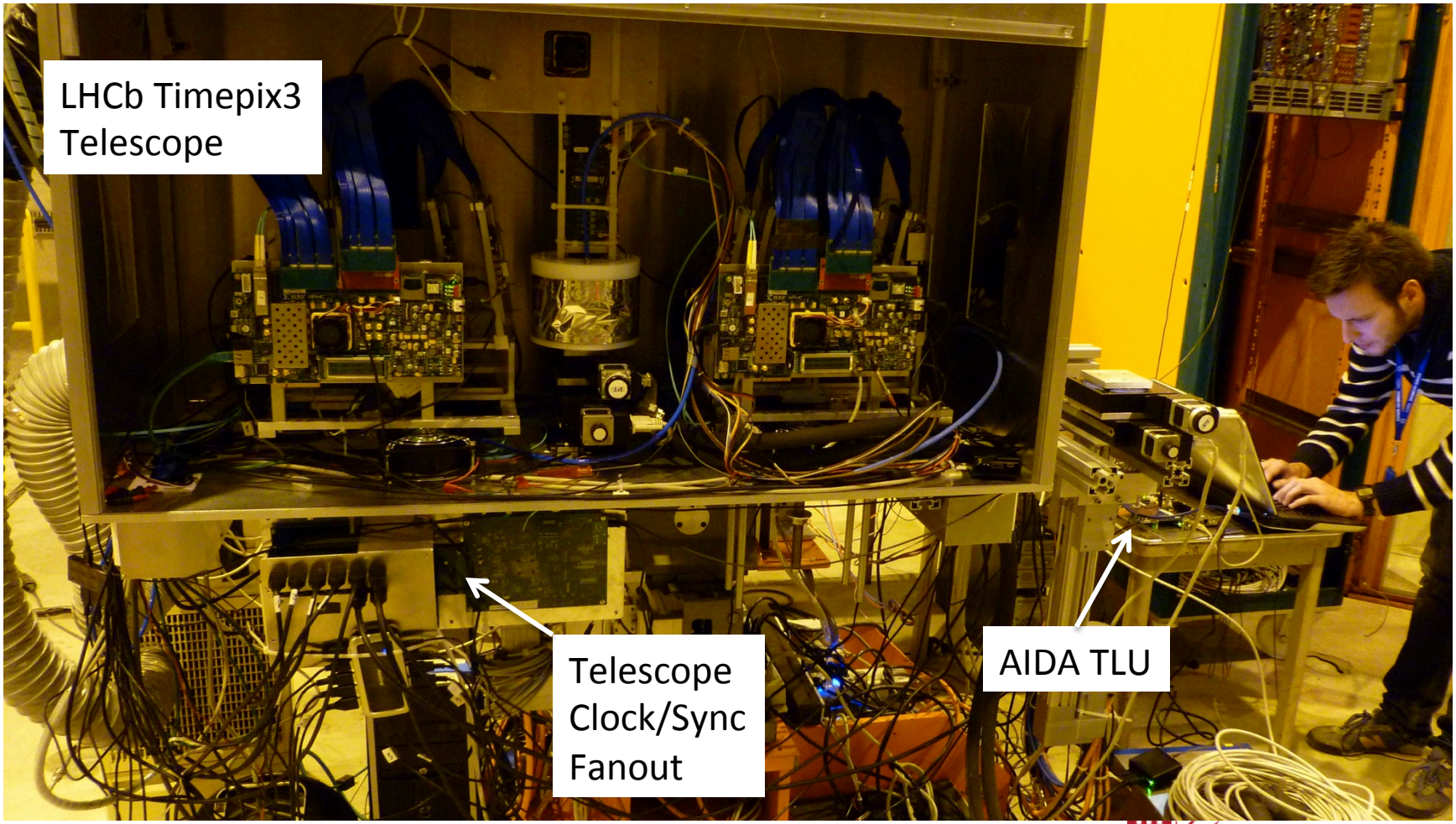
TLU in action

- Debugging new interface with AIDA telescope
- Operation with non-AIDA telescope:
  - Interfacing TORCH (LHCb upgrade proposal) DAQ with LHCb TimePix3 telescope.
  - Accepts clock and synchronization signals from LHCb telescope
  - Provides “AIDA synchronous interface” to DUT

AIDA TLU with non-AIDA Beam-Telescope



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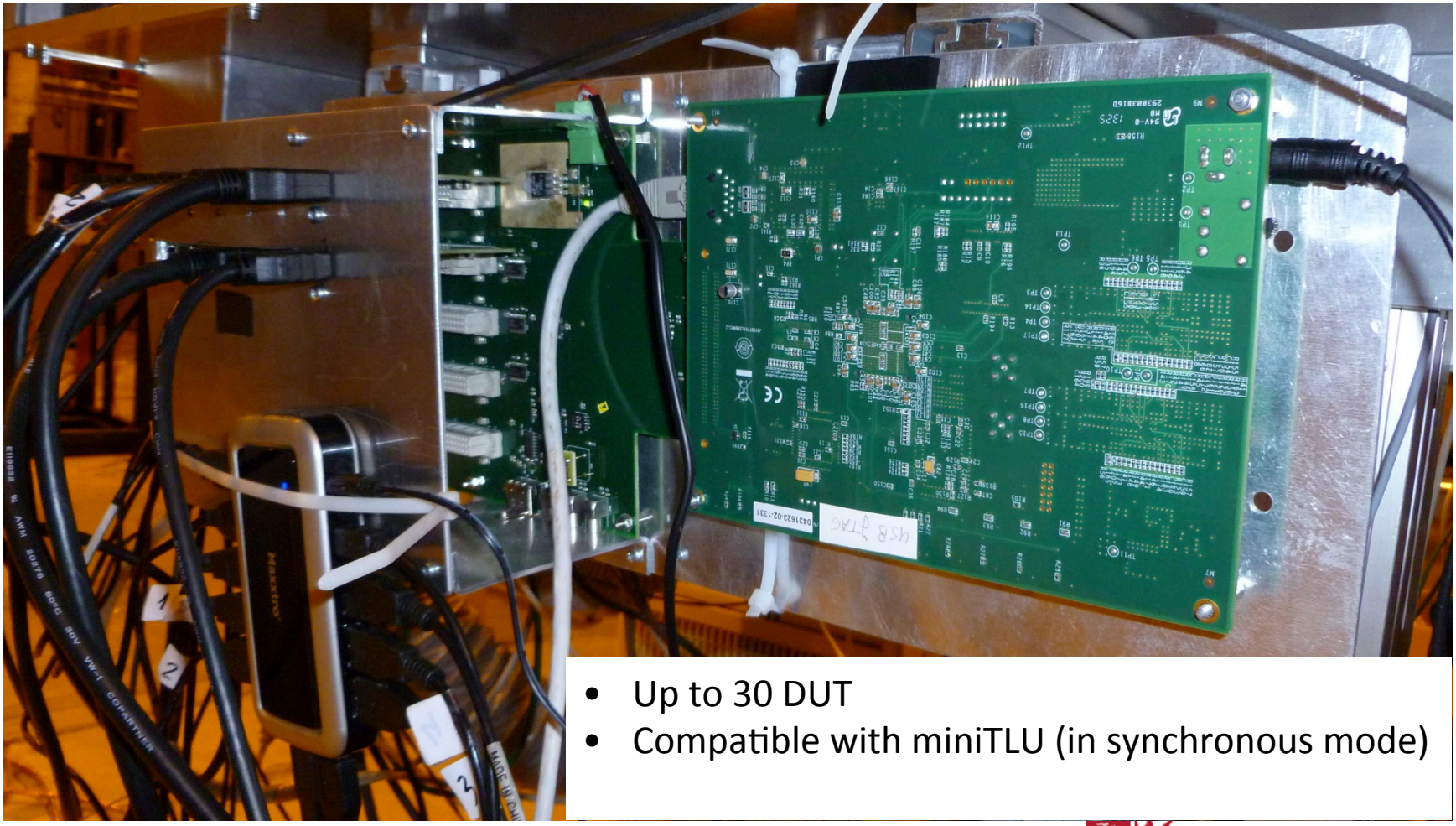
Clock/Syncronization Fanout



- Up to 30 DUT
- Compatible with miniTLU (in synchronous mode)

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Status – Hardware

- Ten AIDA miniTLU boards exist
  - Production organized and paid by DESY
- Minor hardware bugs
  - correctable by external plug-in cable converter
- Bug fixed design by end of AIDA

Status – Firmware

- Synchronous mode implemented
- EUDET mode still in development
- TDC functionality tested (and works)
  - Granularity 780ps
  - Separate timestamp for each trigger input
- Basic coincidence logic exists. Being tested and improved

Status – Software

- Producer for EUDAQ-2 written
  - Basic Functionality Present
- Sustained trigger rate of 1MHz measured
- Debugging continues

Plans

- Current team available until end March 2105
- Aim to have “finished” TLU by then.
- Longer term plans depend on outcome of AIDA-2020
  - If no AIDA-2020 support on best-efforts basis
    - Hardware, Firmware, Software all freely available
    - (Modifying PCB needs access to CERN CAD libraries)

Summary

- Aim: Simple hardware unit to make common beam-tests easier.
  - Basic functionality achieved
  - Full functionality badly delayed but nearing completion
- Existing TLU specification document will be uploaded as an AIDA note.