Frontier Particle Physics with the ATLAS Detector at the Large Hadron Collider

Sub program No. 5

Title: Preparing for the LHC upgrade

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Prototyping electronics and data acquisition for sTGC

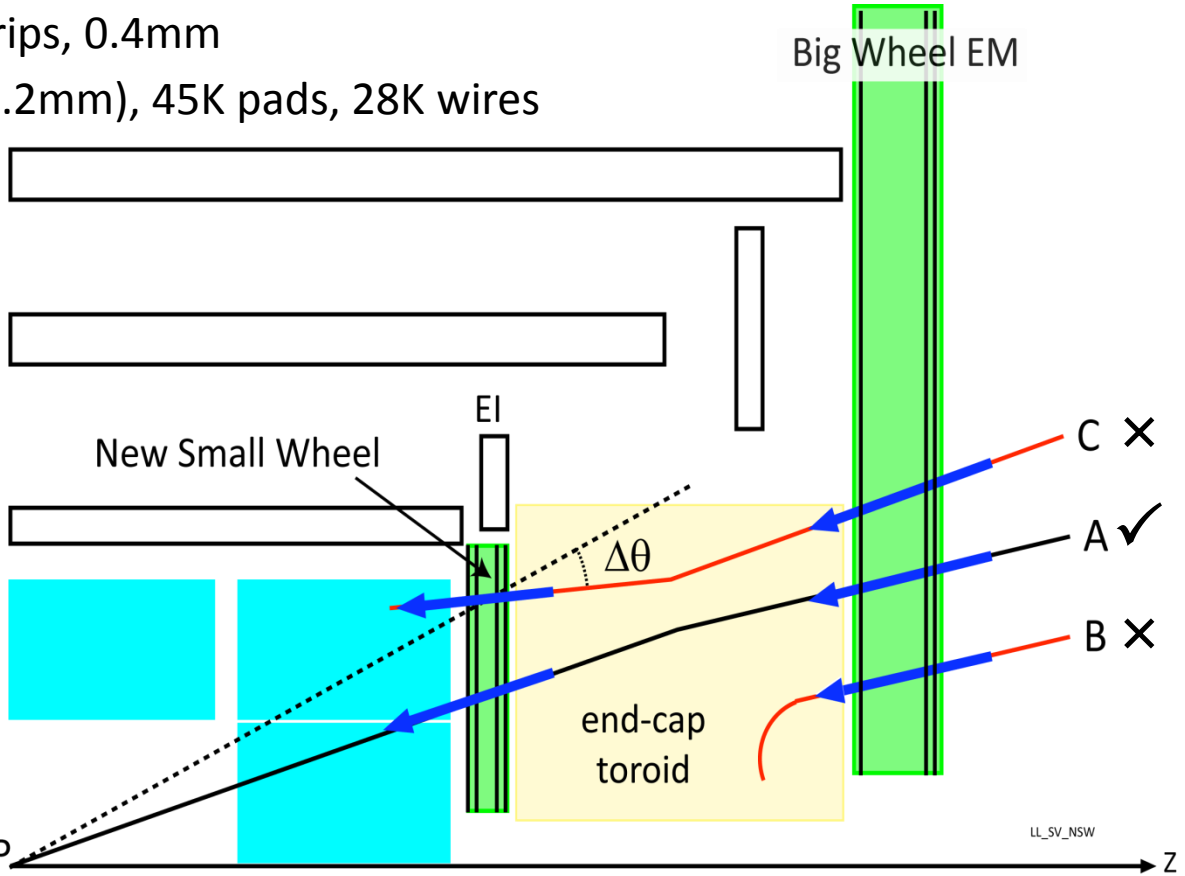
ISF Centre of Excellence Workshop, 1 October2014

NSW trigger concept

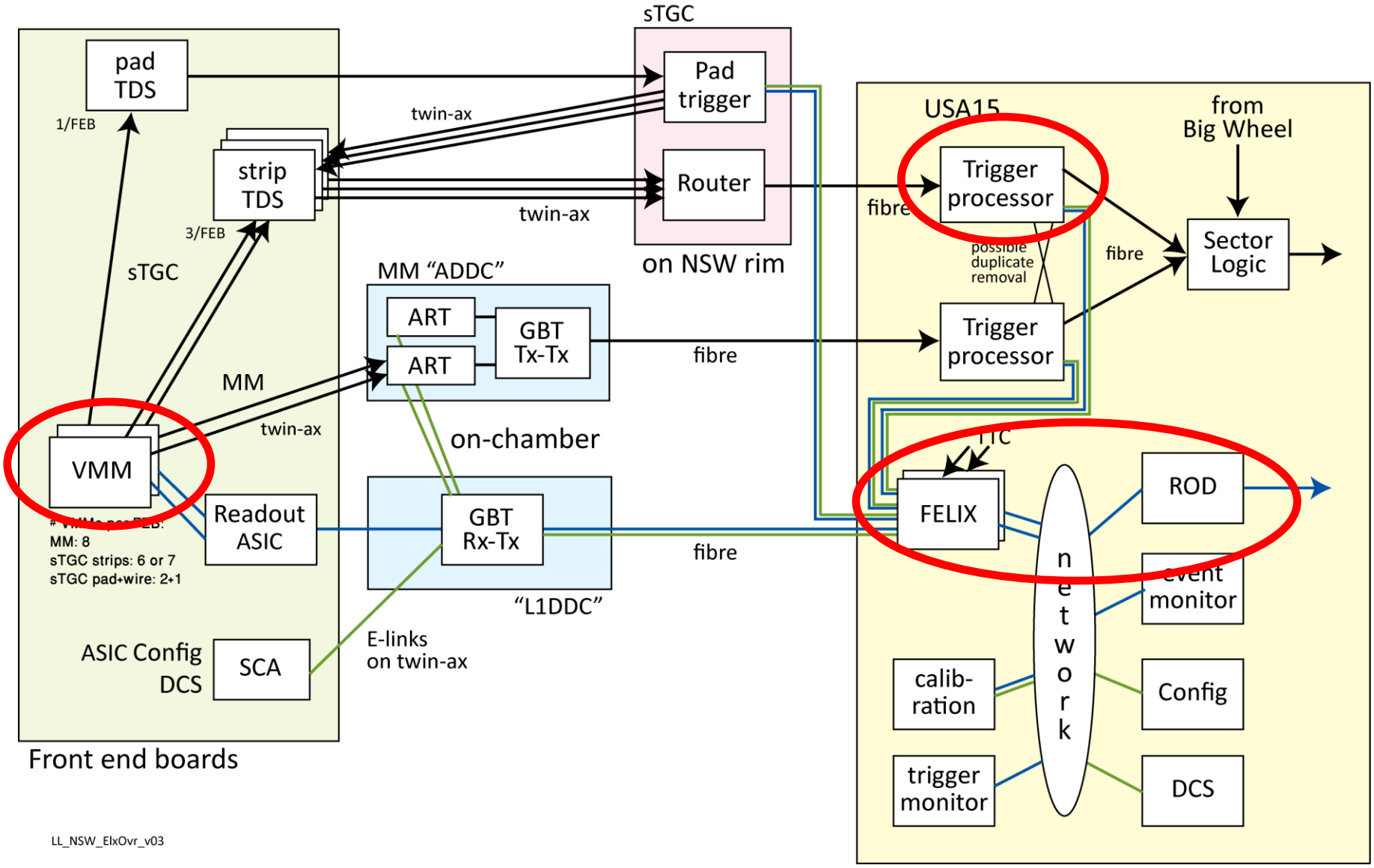
- Phase I upgrade: Increased backgrounds, but must maintain existing trigger rate
- Filter "Big Wheel" muon candidates to remove tracks that are not from the IP
  Only track "A" should be a trigger candidate: pointing: $\Delta\theta$ e.g. < ±7.5mrad
- **Challenge is latency**: 500nsec for electronics + 500ns fibres to be in time for Big Wheel
- Micromegas: 8 layers, 2M strips, 0.4mm
- sTGC: 8 layers, 280K strips (3.2mm), 45K pads, 28K wires
- sTGC, MM find candidates independently,
  list merged for Sector Logic
- Hit per layer:

  sTGC:
  hit is centroid of 3-5 strips

  Micromegas:
  hit is address of strip

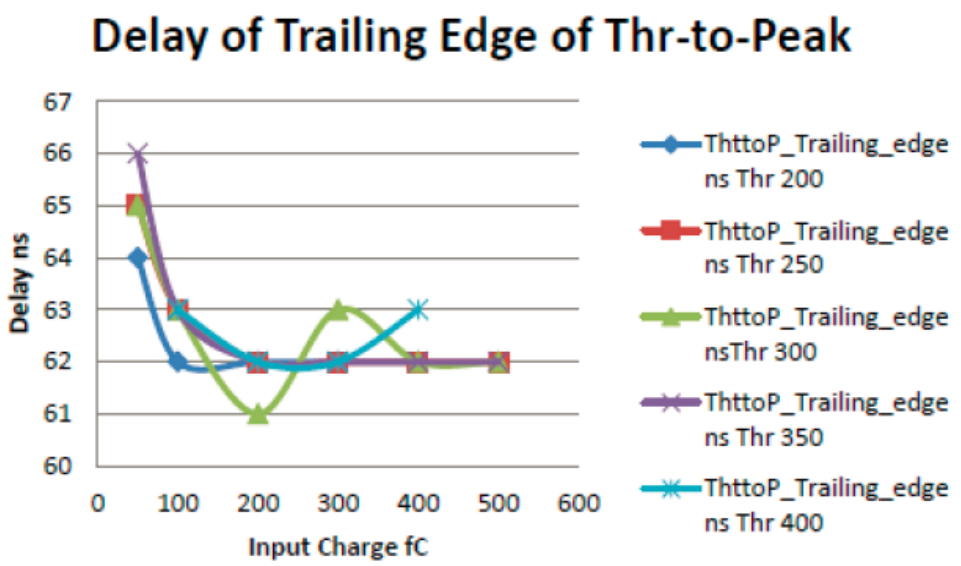


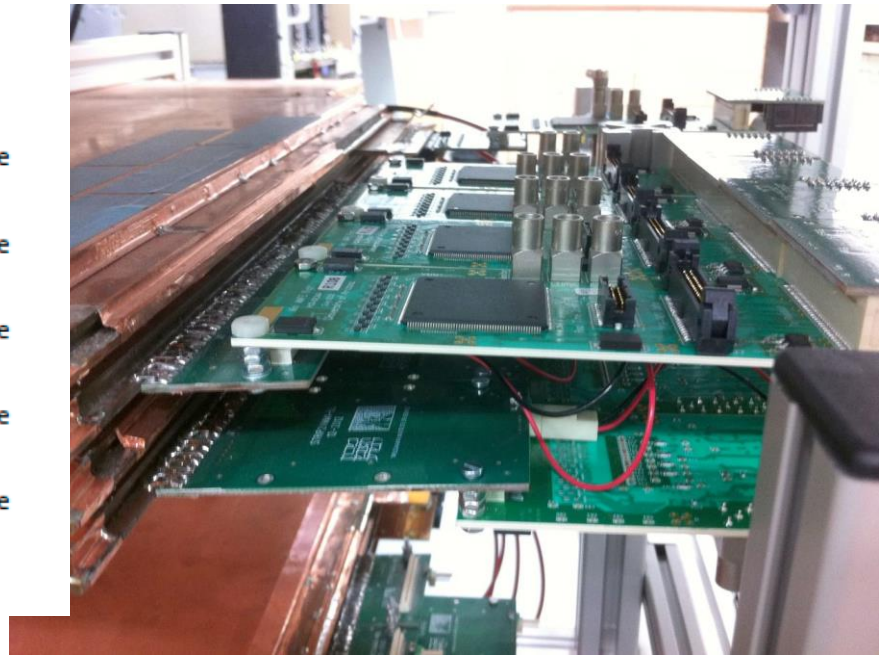
New Small Wheel Electronics and Trigger/DAQ



Front end ASIC - VMM

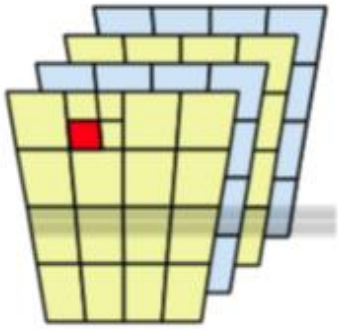
- ASIC developed by Brookhaven for both Micromegas and sTGC
- Israel groups have worked extensively on testing the first prototype (VMM1) in the lab (pulsers and cosmics) and in test beam
- Problems and requests have been fed back to the designers
  Designers not aware of all our detailed requirements



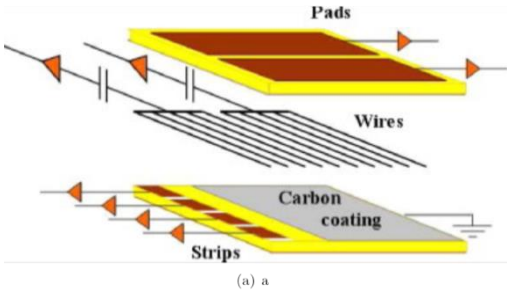


sTGC Trigger Processor for the New Small Wheel

sTGC trigger scheme



1/16th sector



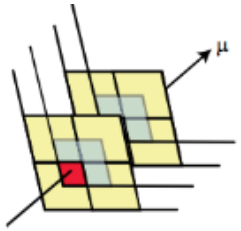
On Rim of NSW FPGAs

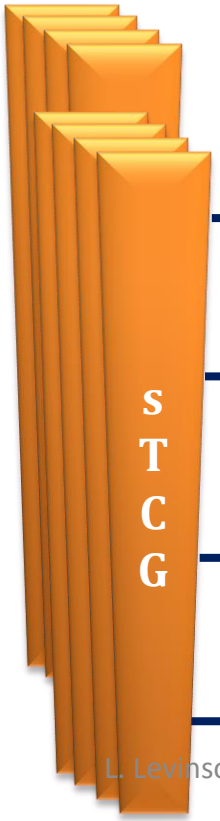
USA 15

Pad Trigger

Router

sTGC Trigger Processor





Pad VMM

Pad TDS

Strip VMM

Strip TDS

Strip VMM

Strip TDS

Only one Strip TDS chosen

On-chamber ASICS

Problem: no BW to read all strips

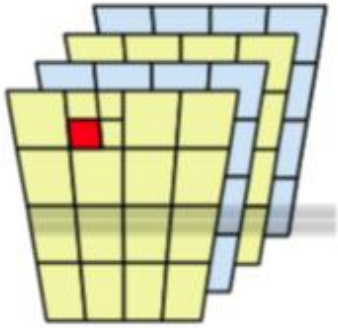
Pad trigger uses pad tower coincidence to choose ONLY the relevant band of strips.

Physical pads staggered by ½ pad in both directions

Logical pad-tower defined by projecting from 8 layers of staggered pad boundaries

Pad-tower coincidence = 2 × 3-out-4 overlapping pads

sTGC trigger scheme



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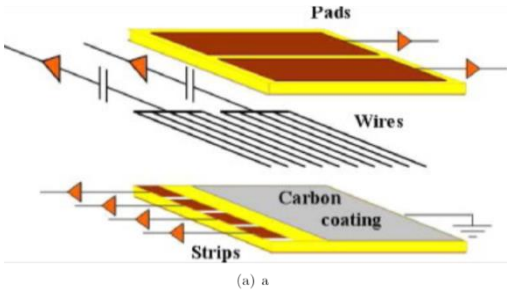

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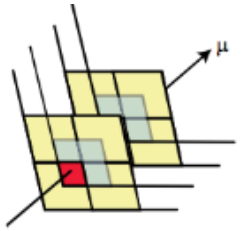

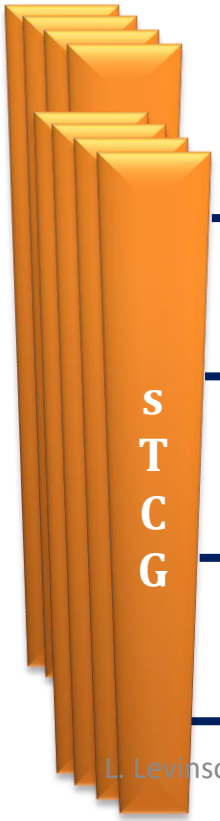

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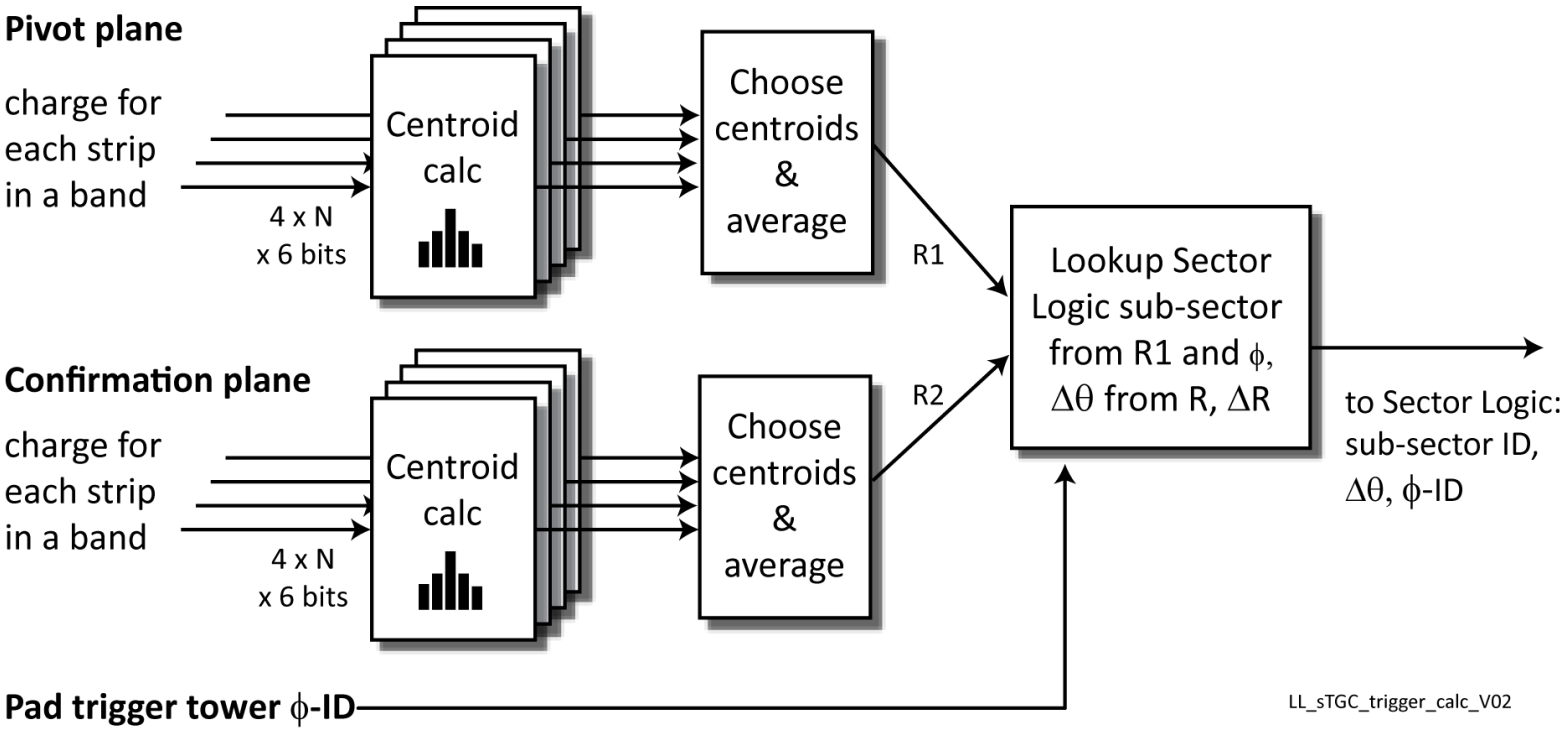
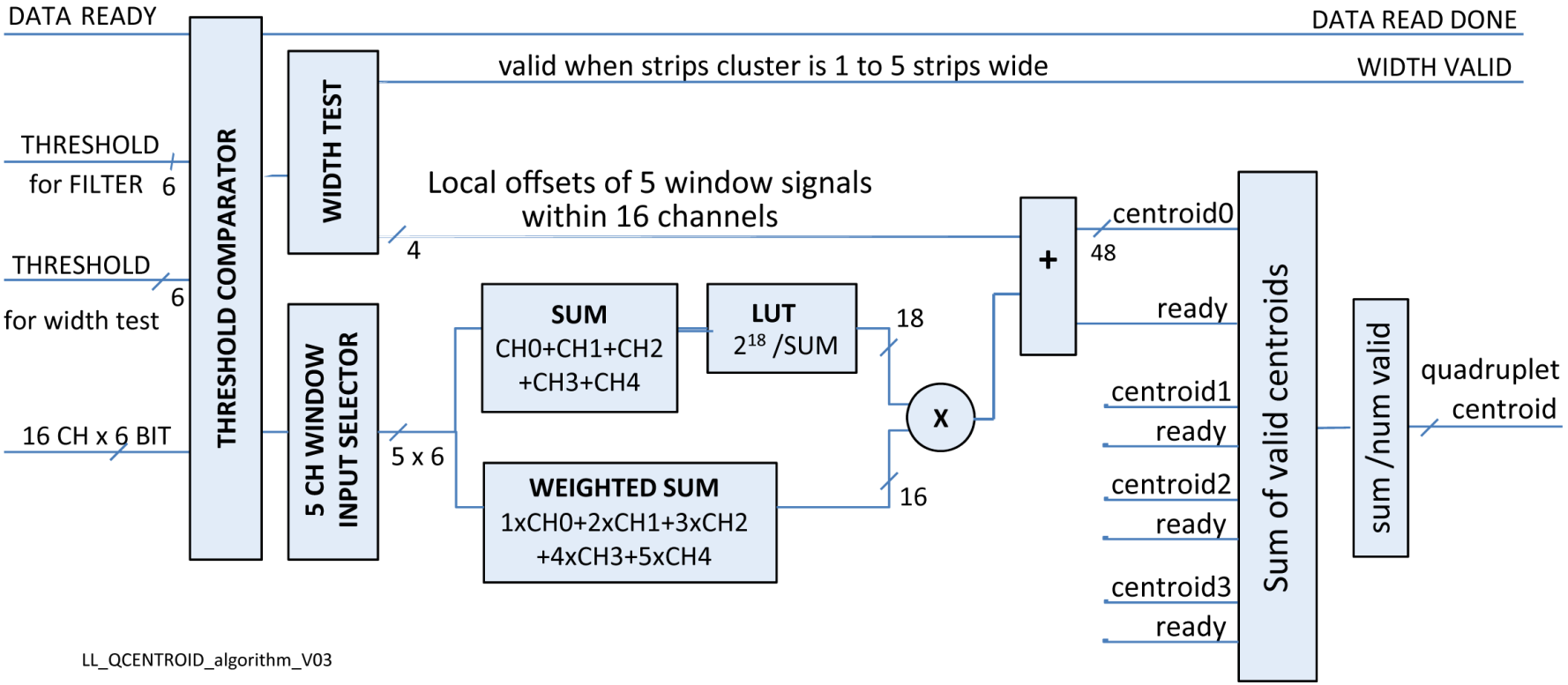
sTGC trigger algorithm



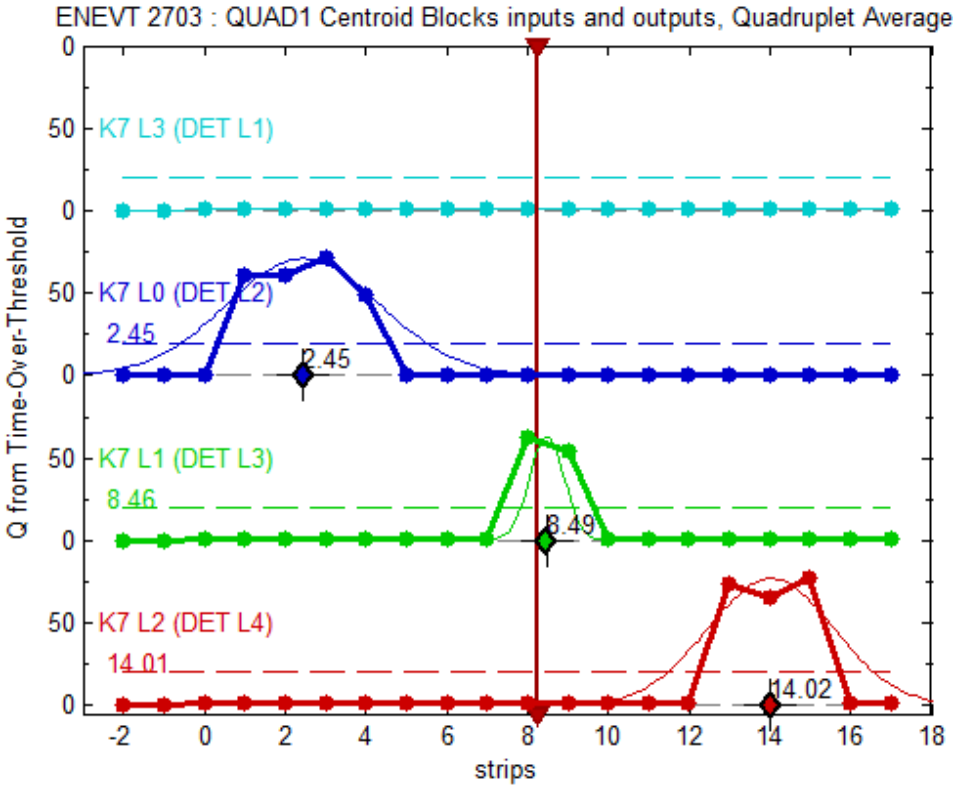
- Use average of centroids in each quad to define space points R1 & R2
- 1, 2, or even 3 of the 4 centroids of a quadruplet are omitted from averaging if:
  - δ-ray's: wide (>5 strips)
  - Neutrons: large charge or wide
  - Noise: single strip
  - Pileup, i.e. pulse in a component strip is active before the trigger

sTGC centroid calculation & averaging



sTGC centroid finder demonstrator

- Cosmic ray test of one quadruplet
- Trigger demonstrator using Xilinx Virtex-6 evaluation board
- Custom mezzanine cards to accept the ToT signals from 8 (16-chan) FE VMMs, 4 strip + 4 pad layers:
  - Triggers on 3-out-of-4 pad layers
  - Calculates Time-over-Thresholds (VMM1 does not have 6-bit FADC)
  - Finds 4 centroids
  - Selects and averages centroids
  - Sends inputs and outputs to ethernet for recording, playback
- Latency of centroid calc: ~45ns



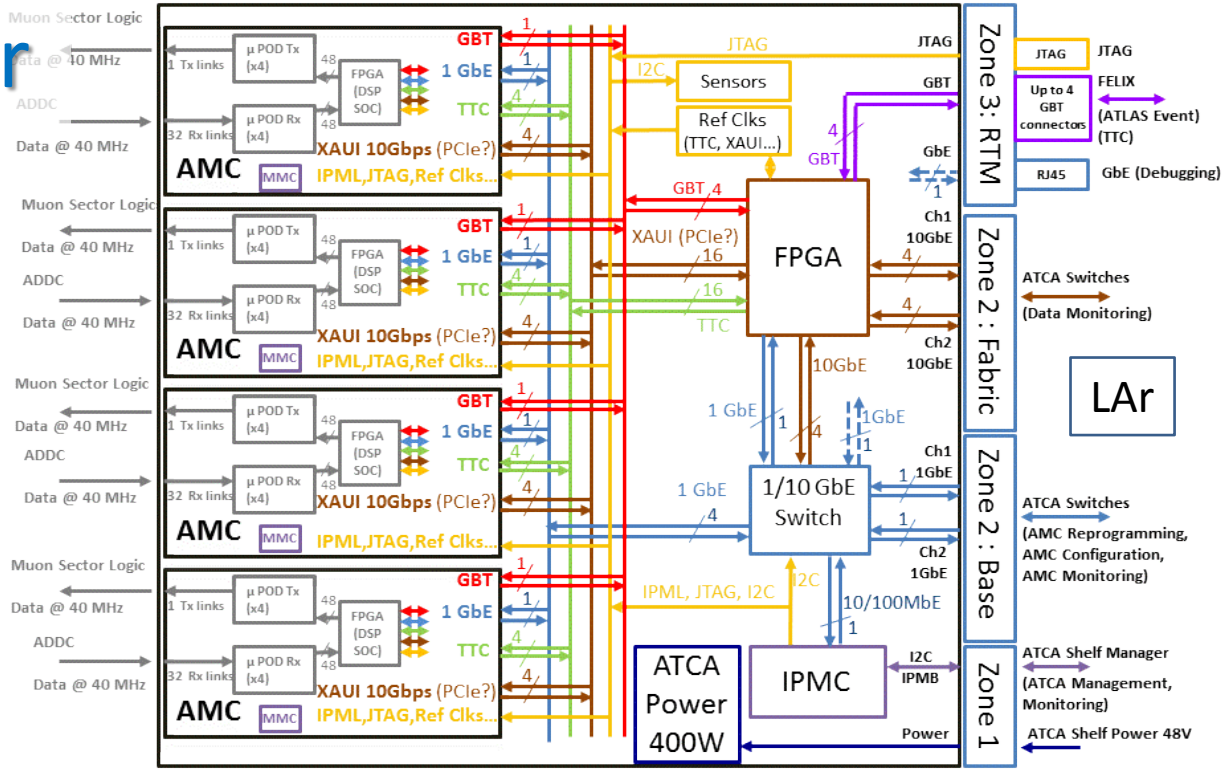
A cosmic ray passing at an angle thru' a quadruplet.

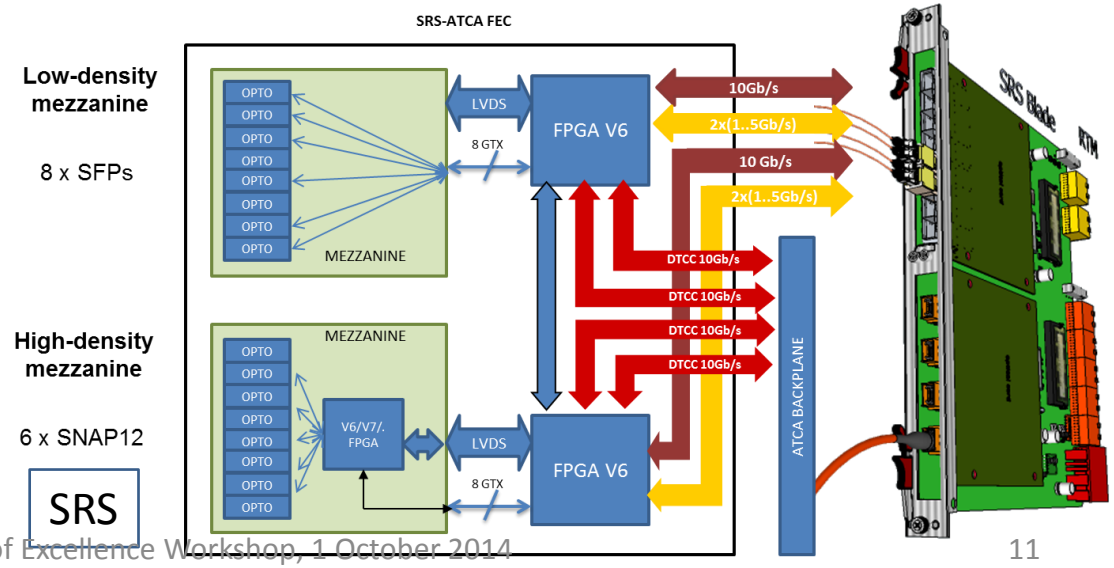
♦ are the centroids (values on the left)

Vertical line is the calculated average.

Trigger processor

- ATCA-based FPGA boards, one board per quadrant, 2 crates
- Input fibers per quadrant: MM: 128, sTGC: 96
- Separate MM & sTGC boards share candidates via ATCA backplane
- Try to avoid development of yet-another-ATCA-FPGA board
  Candidate carrier & mezz: LAr, SRS





The new readout architecture for the ATLAS upgrades

ATLAS readout architecture - it had to change

Designed in the late 1990's

- High speed optical serial links just emerging (1Gbit/s was the latest and expensive)
- Separate interconnect technologies for readout, trigger, DCS, TTC (Timing Trigger & Control)
- Every subdetector chose its own, separate interconnect technologies
- Readout bandwidths >> PC network BWs and PC memory BWs

$\Rightarrow$ Custom hardware readout processors , "RODs" (FPGAs in VME)
Custom for (almost) each subdetector
$\Rightarrow$ expensive + huge effort in design, commissioning, operating by experts
and now a headache for long term maintenance

– But they worked very well

All the assumptions have changed:

- 100Gb/s network links will be commodity in 2015
- 2014 PC memory-to-CPU BW is 80GBytes/s, peripheral-to-CPU at 128Gb/s
- 12 cores in a 3GHz CPU chip, with 128GB memory affordable
- Same 4Gb/s "GBT" interconnect used by most subdetectors -- for all traffic
  - GBT aggregates many slower (80Mb/s) links from individual front end chips
    into a single optical bi-dir link for transport to/from USA15
  - The GBT link can carry readout, trigger, DCS, TTC, calibration, configuration data on a single bi-dir link

⇒ Opportunity

  - to use industry standard commercial components
  - to do in software much of what was done in hardware
  - for all (many) subdetectors to use a common module for the part that must be hardware

FELIX: the new architecture

Born at Weizmann, for the New Small Wheel, but

FELIX was approved by the Upgrade Steering Group as the readout architecture for the ATLAS Phase-2 Upgrade

It also approved its use in Phase-1, for

- New Small Wheel
- Level-1 Calo trigger
- Liquid Argonne

Lots of discussions, hesitations, suspicions by several subdetectors and expanded functionality,
but, (after 2 years) just about all are now committed.

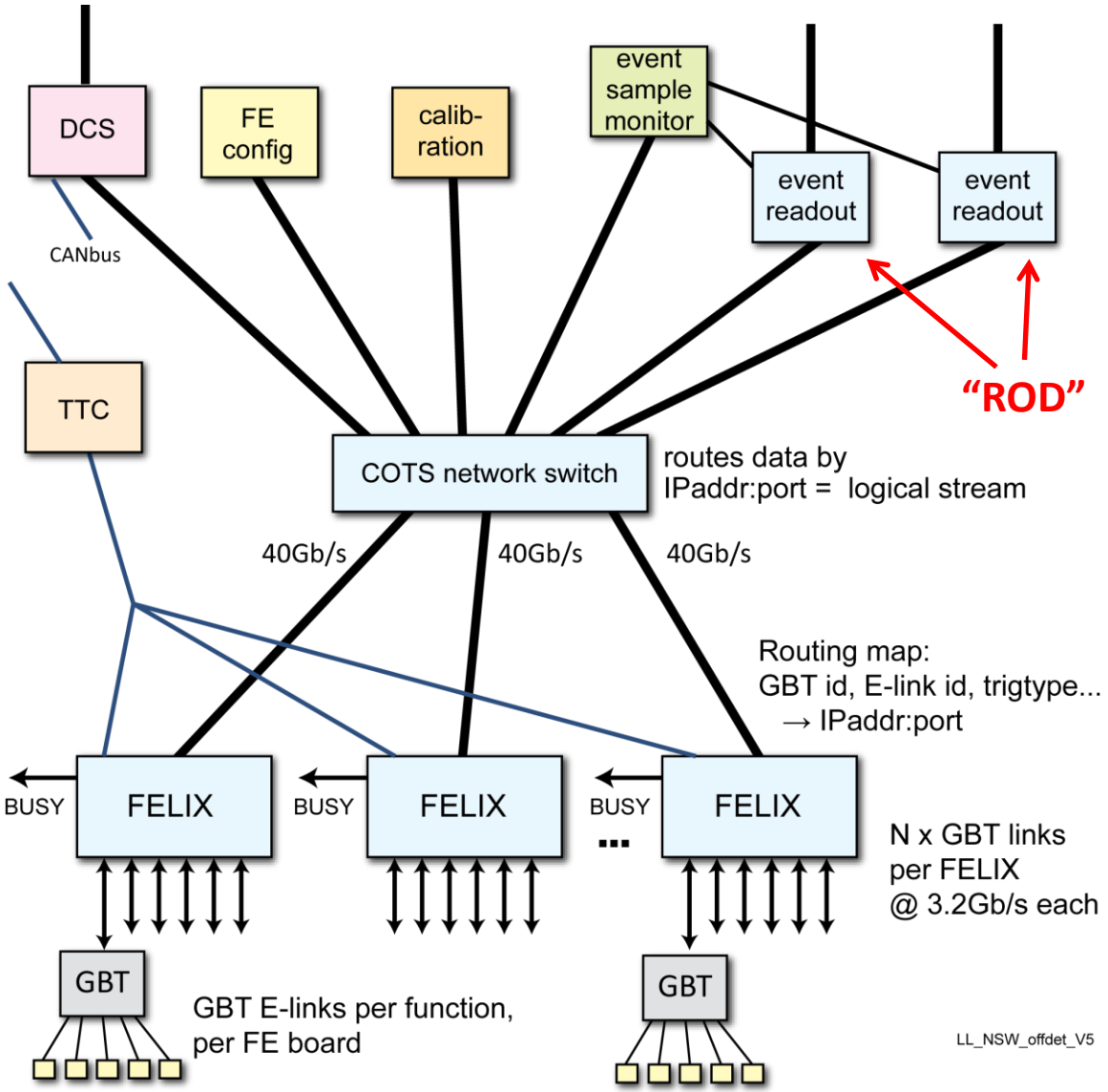
Not easy to get so many to agree on a common element.

Guiding principles

- Goal: a GBT-to-LAN “switch” as close to the Front End as possible, and with as little awareness of detector specifics as possible
  - No user code in FELIX: configuration params for options
- Separate data movement from data processing
- Configurable data paths from logical on-detector “E-links” to network endpoints
- Scalable at Front end, Back end, and switch levels
- Do as much as possible in software
- COTS FPGA PCIe board
- Readout, control and monitoring data, so latency is not important,
  but provide low latency links for trigger
- Future proof by following COTS market, separately upgradeable components:
  GBT, FPGA PCIe board, server PC, network cards
- Routing is for E-links; they are the logical connections

Off- detector architecture with FELIX

- FELIX separates data movement from data processing
  - Data movement: by common hardware
  - Data processing: software specific for each subdetector
- Processing functions can now be separated, physically, or just logically.
- "ROD" = Event fragment builder/processor for ROS



FELIX Demonstrator

No hardware development, only firmware and software development
  – COTS components; software and firmware is enough work

Collaboration: Argonne, Brookhaven, CERN, Nikhef, Weizmann

Schedule: Demo and review 1Q2015 (aggressive)

Hardware

- Commercial FPGA PCIe board
- Intel server PC
- Commercial network card: Mellanox dual 40Gb/s Ethernet or Infiniband

Reuse of firmware

- PCIe from new ATLAS ROBIN
- GBT-FPGA and TTC package from GBT group
- HDLC from LHCb

* Weizmann equipment for R&D funded by Weizmann Benozyo Center

Software ROD

- Once FELIX flows front end data into Ethernet, the ROD can be a PC, provided that it is powerful enough to absorb, check, build events, reformat, and transmit to the central ATLAS DAQ system.
- Detailed estimates of the expected data volume were made
- A “toy” SW ROD was set up by NIKHEF to measure the capability of a PC as a SW ROD:

⇒ A SW ROD based on a 2014 PC is able to do the job.

- The ROD is simplified: only processes event data
  - FELIX routes calibration and configuration data from dedicated calibration, and configuration processes
- On the basis of this test, the estimated data volume, and detailed evaluation of the ROD Use Cases:

  NSW decided that a SW ROD would be the NSW baseline.
- NSW is the first such ROD, already in Phase 1

Thank you

sTGC trigger: strip logic: one layer of one 1/16th