Trends in

MONOLITHIC DETECTORS

and

ADVANCED CMOS MANUFACTURING

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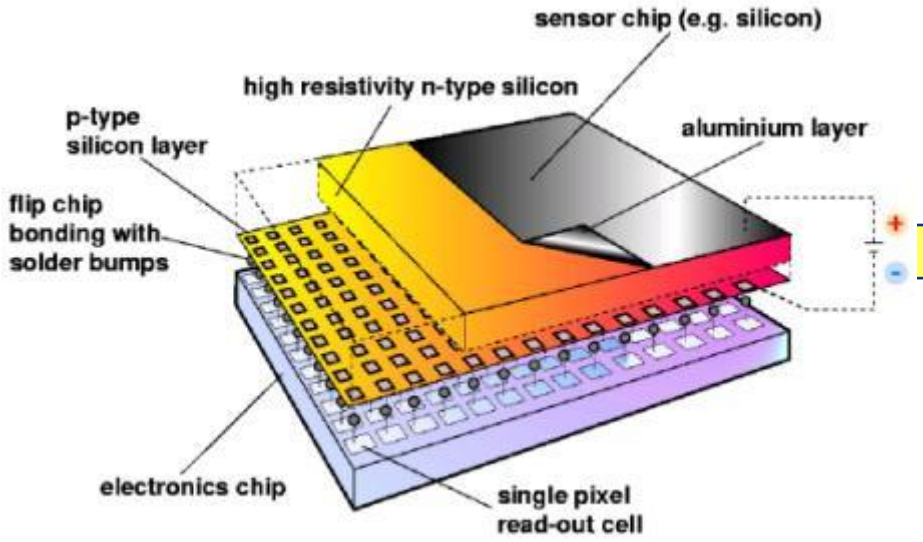
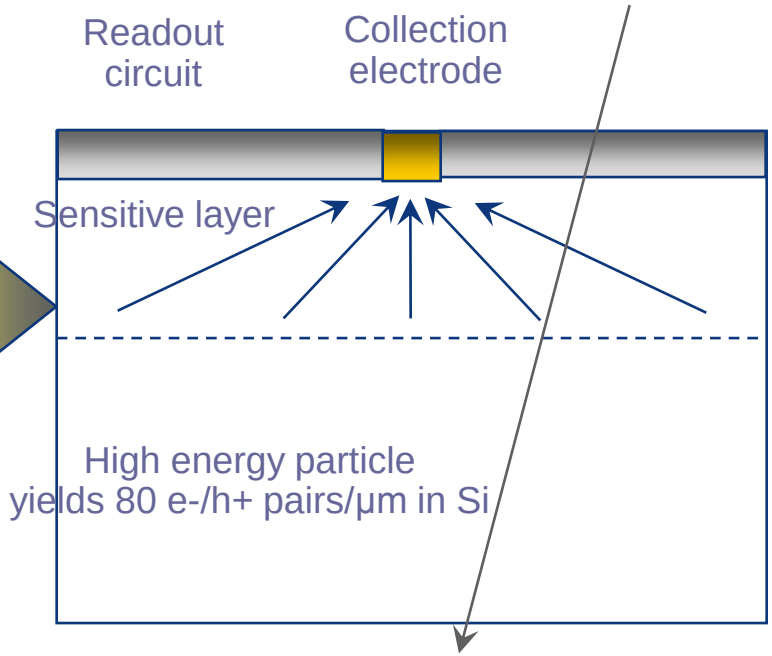
MONOLITHIC DETECTORS : definition

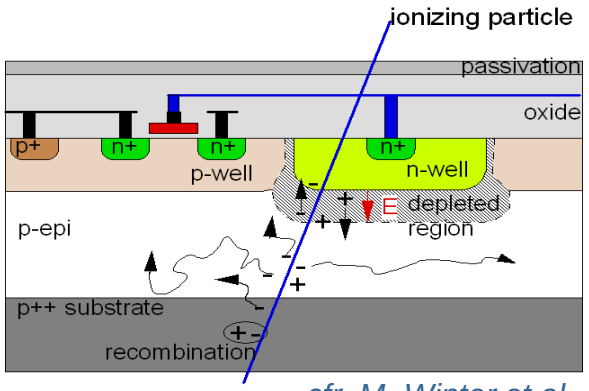




Integrate readout with the silicon sensor

- Advantages in integration, cost, potentially strong impact on power consumption and material budget
- in two experiments: DEPFET in Belle-II and MAPS in STAR
- not yet in LHC, adopted for ALICE ITS upgrade, considered for CLIC/ILC

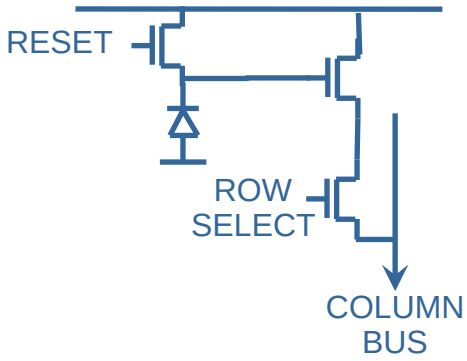
Traditional Monolithic Active Pixel Sensors



cfr. M. Winter et al

- Commercial CMOS technologies
- No reverse substrate bias:
  - Signal charge collection mainly by diffusion
  - more sensitive to displacement damage
- Only one type of transistor in pixel (twin well)
- Rolling shutter readout
  - very simple in-pixel circuit (3 or 4 transistors)
  - pixel size: 20 x 20 μm^2 or lower
  - serial, row-by-row, not very fast

Example: three transistor cell

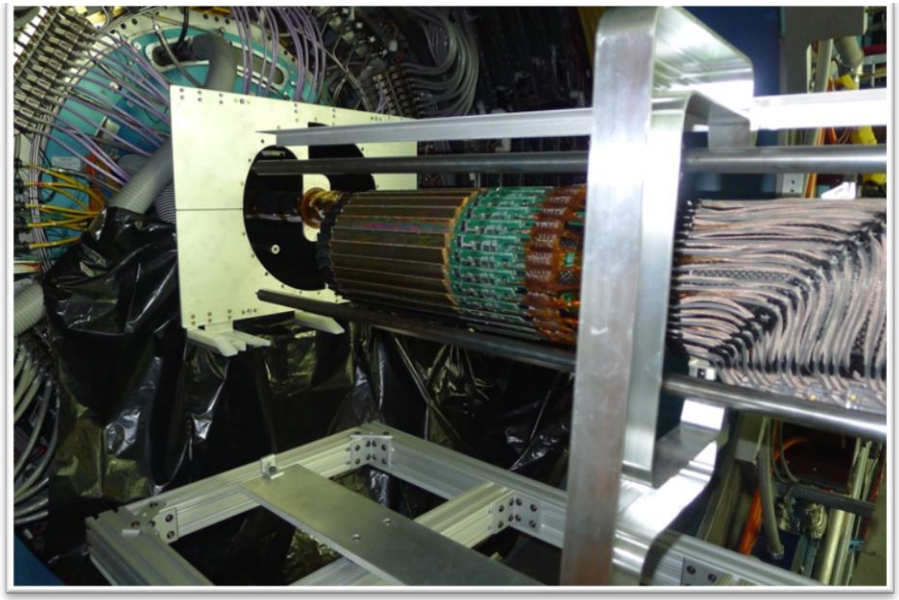


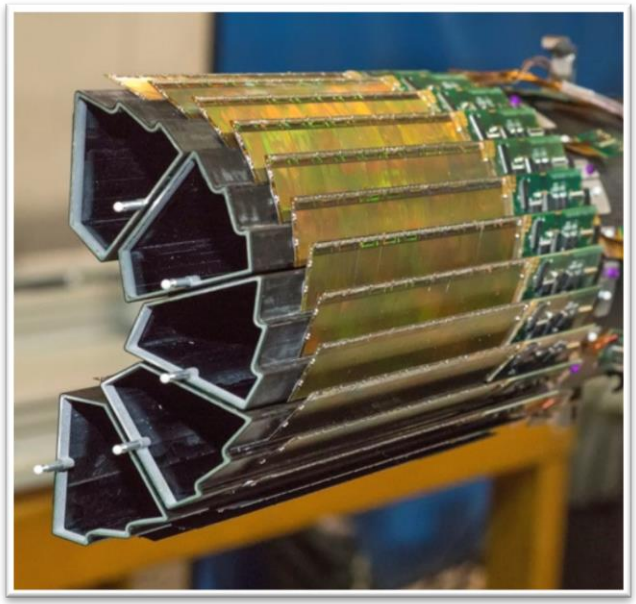
Main challenge for improvement: need combination of:

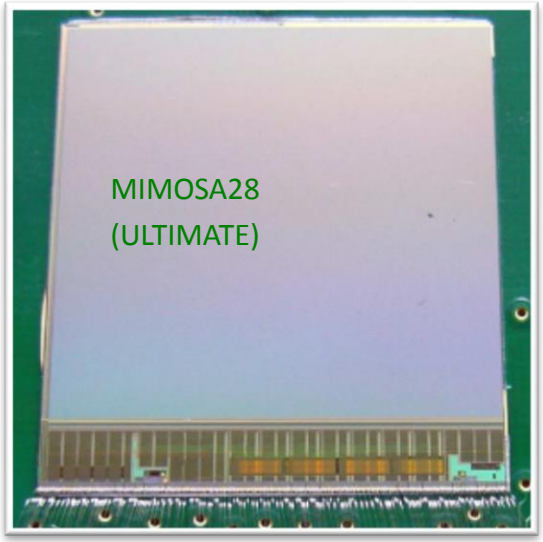
- tolerance to displacement damage (depletion)
- integration of complex circuitry without efficiency loss
- commercial technology

MAPS SENSOR CHIP in STAR experiment

Data taking March-June 2014







First MAPS system in HEP

MIMOSA28 (ULTIMATE) chip
IPHC Strasbourg :

- Twin well 0.35 µm CMOS
- High resistivity (> 400 Ωcm) 15 µm epi
- Readout time 190 µs
- TID 150 krad
- NIEL few 10^{12} 1 MeV n_{eq}/cm^2

THE ALICE ITS UPGRADE PROJECT

Replace the inner tracking system with an entirely new detector in 2017-2018

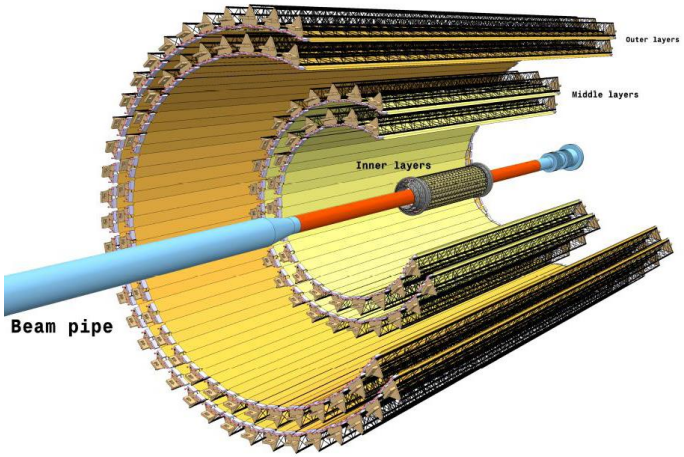
ALICE-TDR-17/CERN-LHCC-2013-024

Improve

- impact parameter resolution by a factor 3 in rφ, 5 in z
- standalone tracking resolution and p_T resolution at low p_T

New Layout 7 layers, 12.5 Gpixels in ~ 10 m^2

- X/X_0 0.3 %
- Pixel size: O(30x30) μm^2
- Inner layer radius 22 mm



Parameters

- Chip: 15 mm x 30 mm x 50 µm
- Spatial resolution ~ 5 µm
- Power density < 100 mW/cm^2
- Integration time < 30 µs
- Max required radiation tolerance : TID 700 krad & NIEL10^{13} 1 MeV n_{eq}/cm^2

Thin sensors, high granularity, large area, moderate radiation

➔ Monolithic silicon pixel sensors

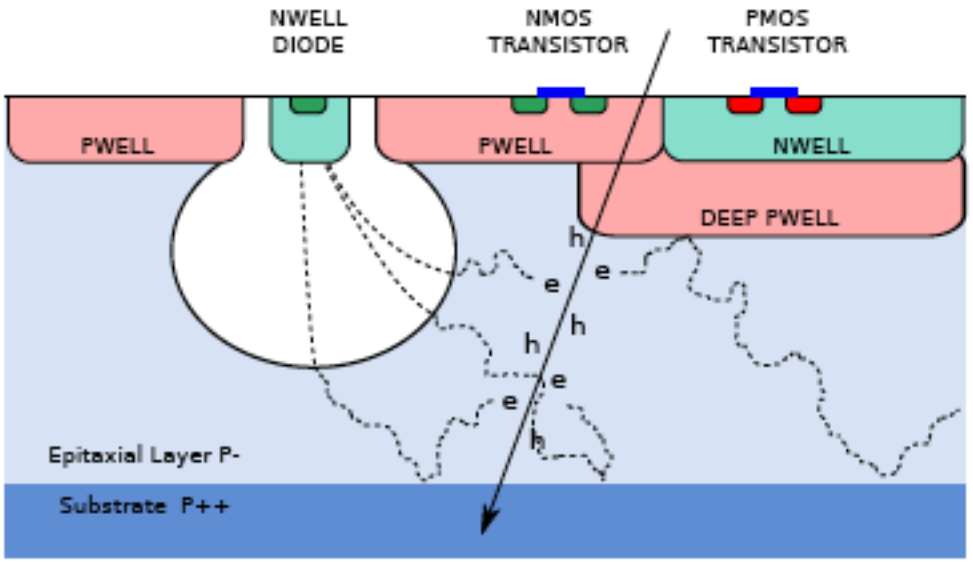
ALICE MONOLITHIC ACTIVE PIXEL SENSOR

Technology choice

TJ 180 nm CMOS imaging process

- Deep Pwell
- Gate oxide < 4 nm good for TID
- 6 metal layers
- 15…40 µm 1…8 kΩcm epitaxial layer
- Epi not fully depleted unless …

(AC coupling, high fields, Dulinski, Kachel et al)



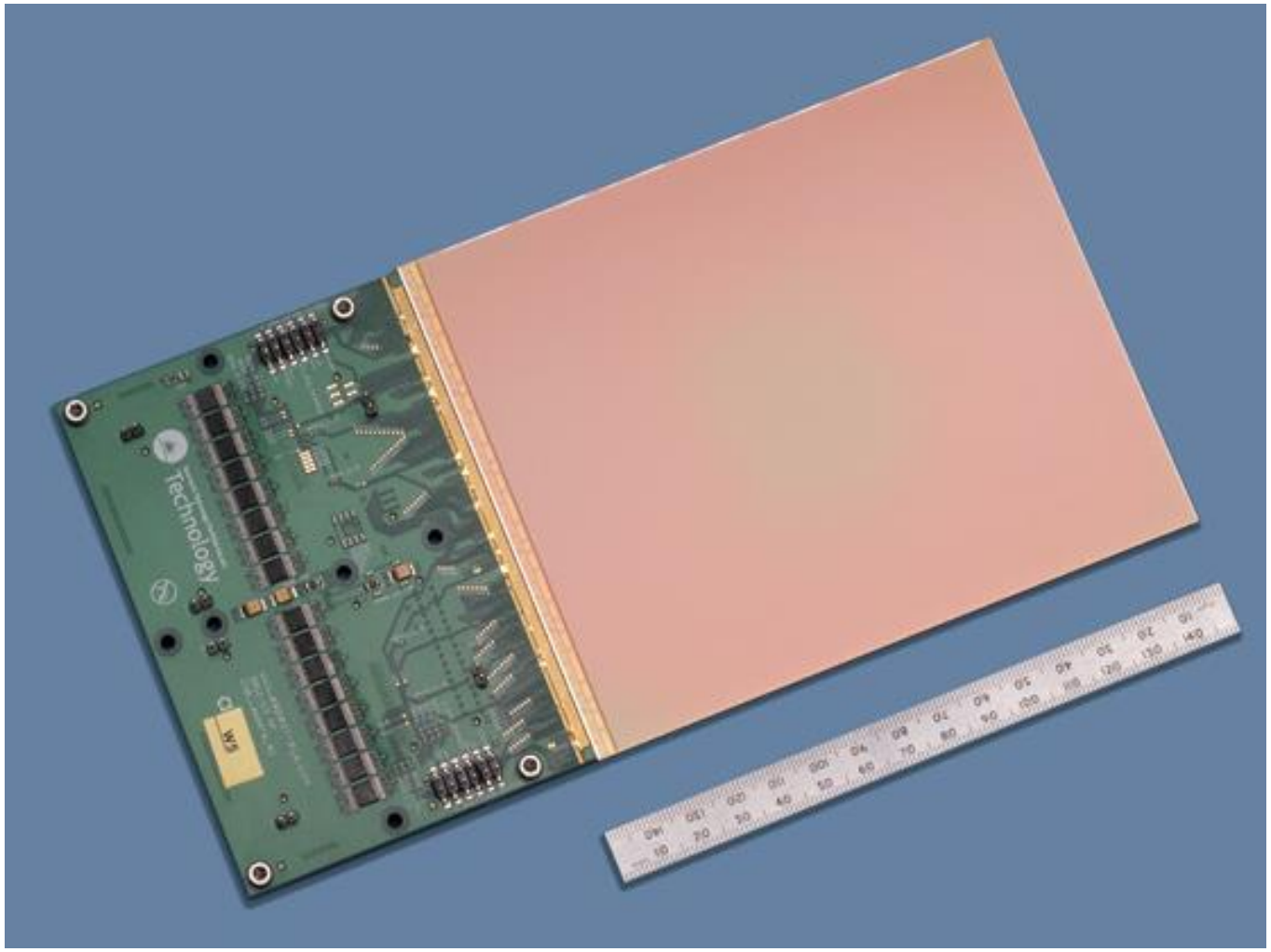
Chip development

- Since end 2011, 4 MPWs and 3 engineering runs, 4th submitted now.
- Two internal pixel chip architectures: ALPIDE and MISTRAL
- Small scale prototypes for sensor optimization and radiation tolerance verification

Full scale prototypes recently fabricated: lab and beam tests ongoing also on:

- irradiated
- thinned (50 µm) devices
- thinned devices mounted on flex

NOTE: WAFER SCALE INTEGRATION by STITCHING

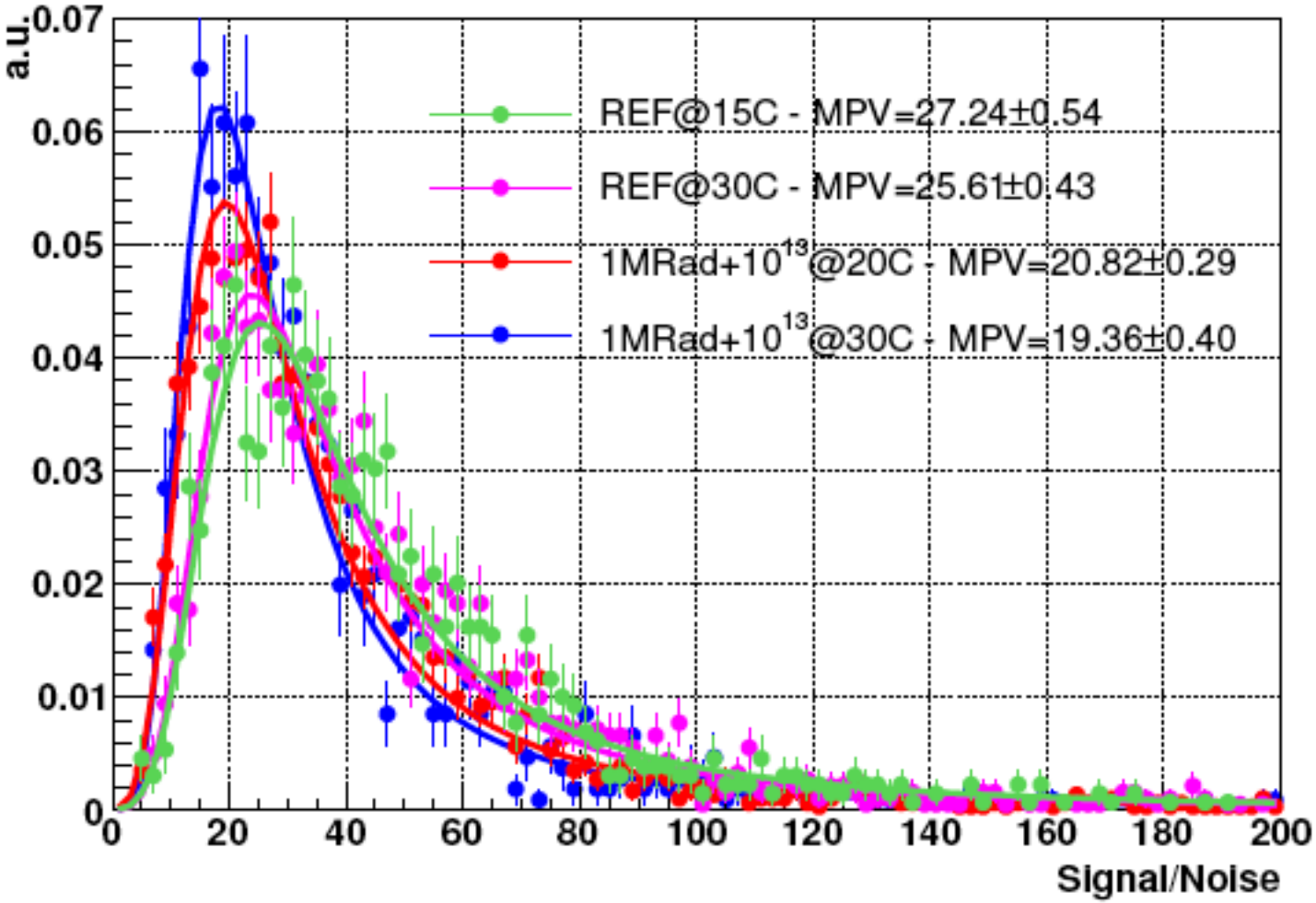


Courtesy: N. Guerrini & R. Turchetta, Rutherford Appleton Laboratory

RAL group designed many sensors in this technology

For the moment stitching not exploited for the ALICE ITS upgrade

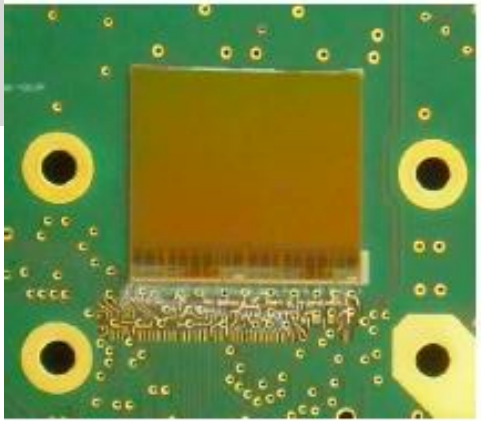
RADIATION TOLERANCE



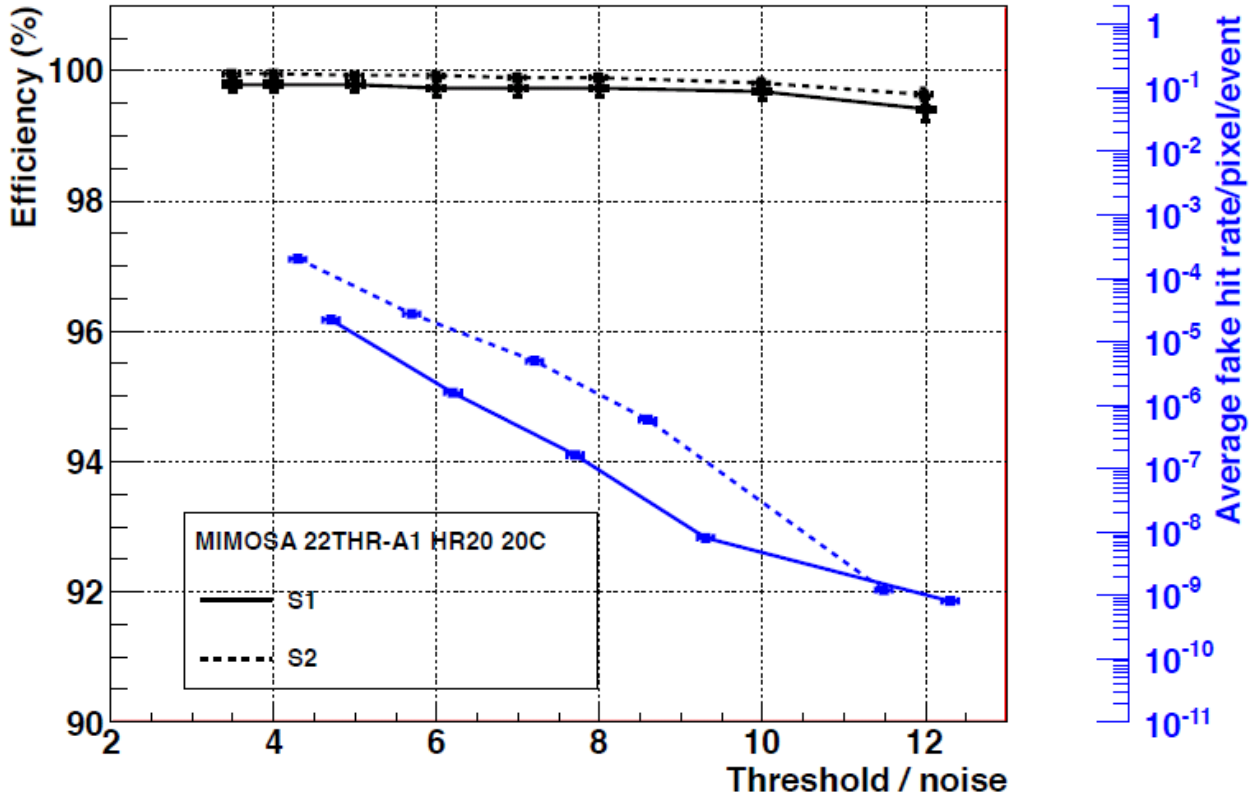
Example: SNR of seed pixel measured with MIMOSA-32 ter at the CERN-SPS at two operating temperatures, before and after irradiation with the combined load of 1 Mrad and 10^{13} 1 MeV n_{eq}/cm^2

MISTRAL

- Rolling shutter: evolution of STAR like development
- FSBB/MISTRAL functional
  - lab tests promising, ENC 15-20e
  - preparing for test beam
- Beam test results from smaller scale prototype:



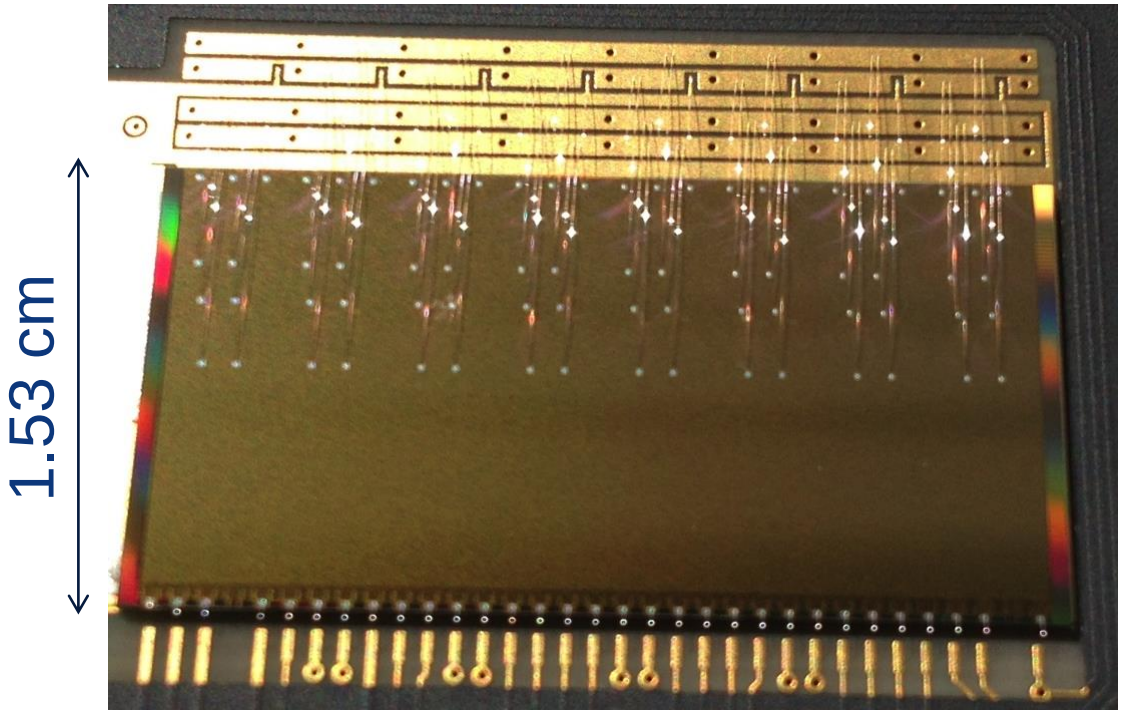
FSBB/MISTRAL



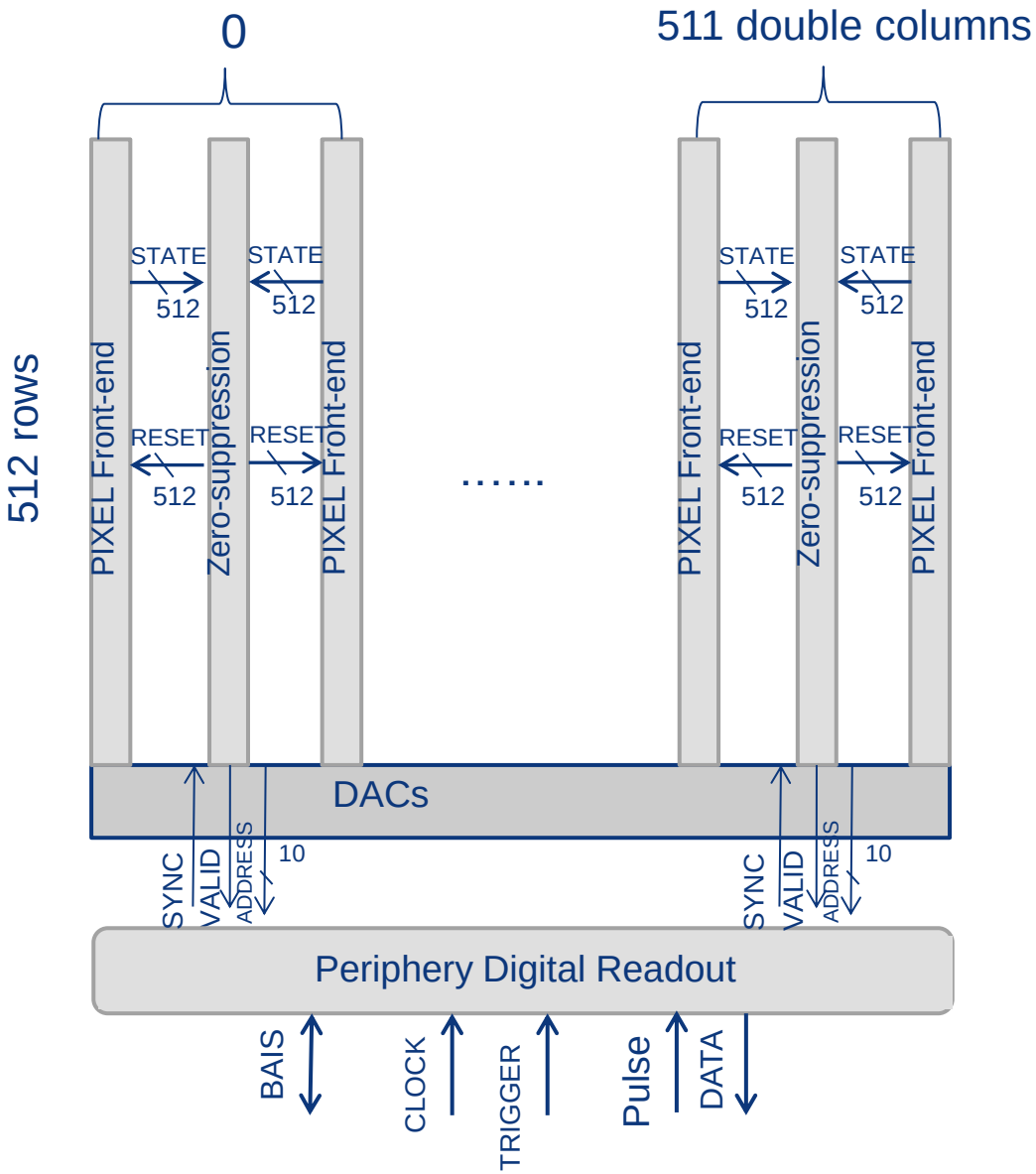
Efficiency above 99 % with fake hit rate below 10^{-5} achievable

ALPIDE

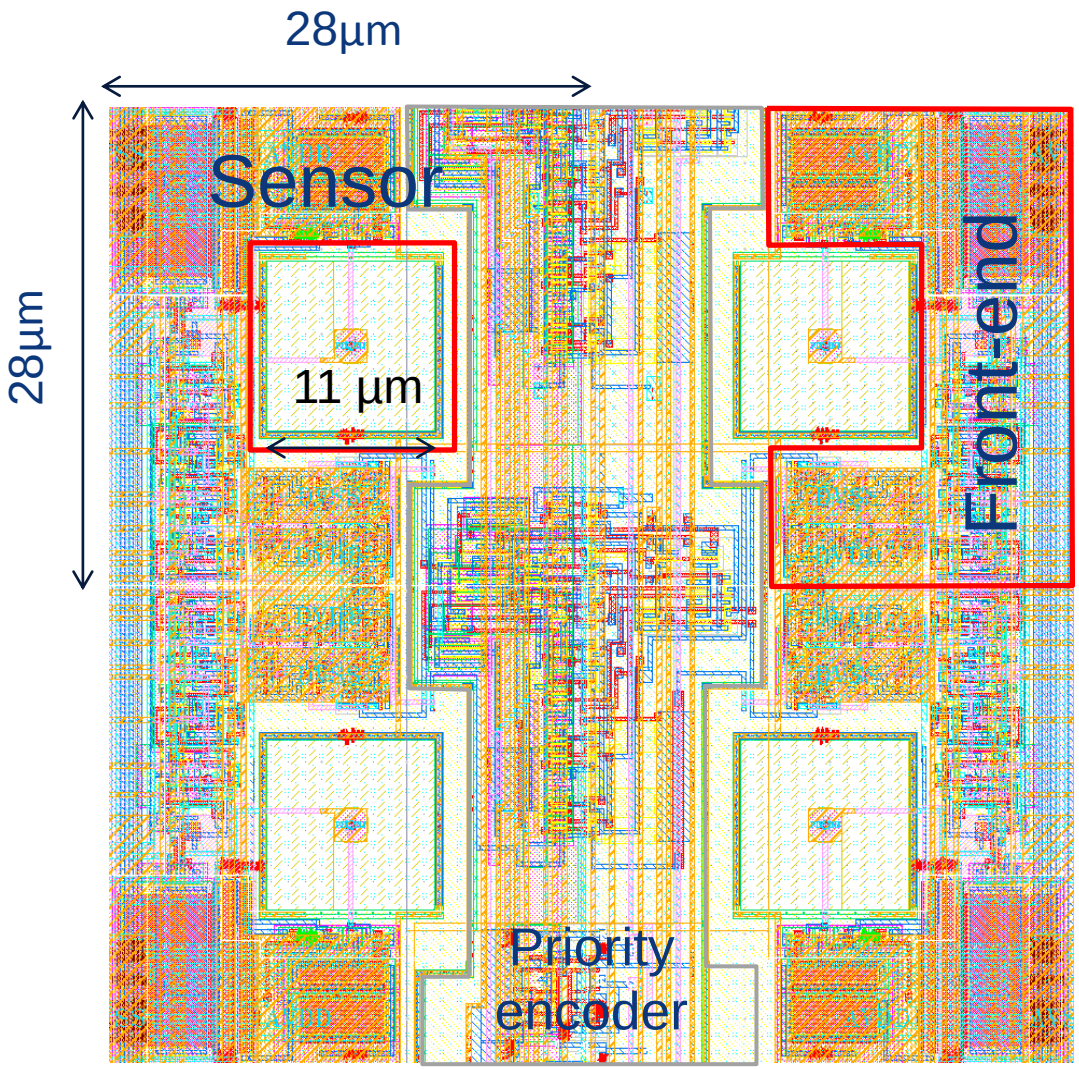
- In-pixel amplifier/comparator ~ 40nW (~5mW/cm^2) allows architectures other than rolling shutter
- Hit driven readout (priority encoder)
- Full scale prototype for the ALICE ITS: chip size: 3 x 1.53 cm^2
  ~ 500 000 pixels of 28 x 28 µm^2



ALPIDE: priority encoder



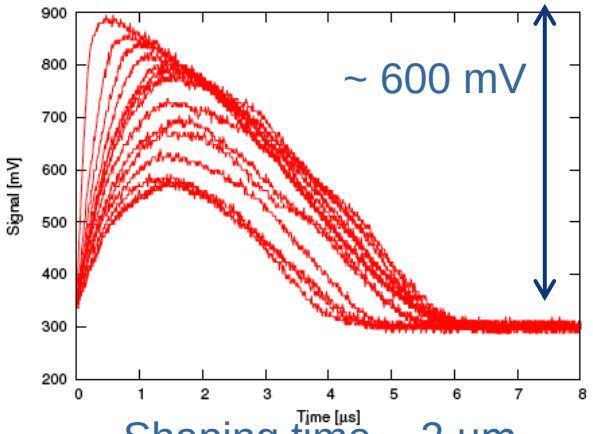
ALPIDE pixel



Pixel layout

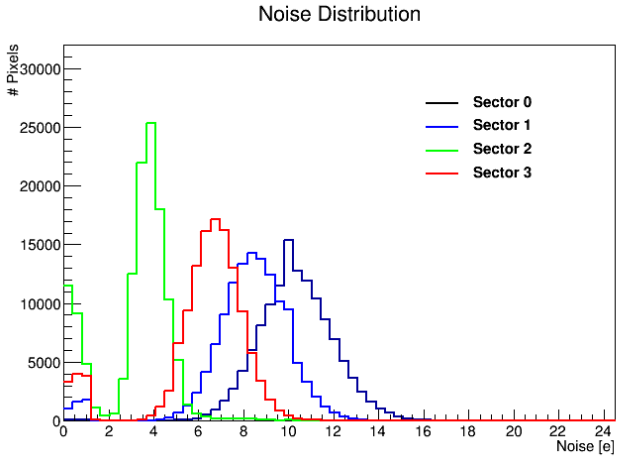
Analogue output of one pixel under ^{55}Fe

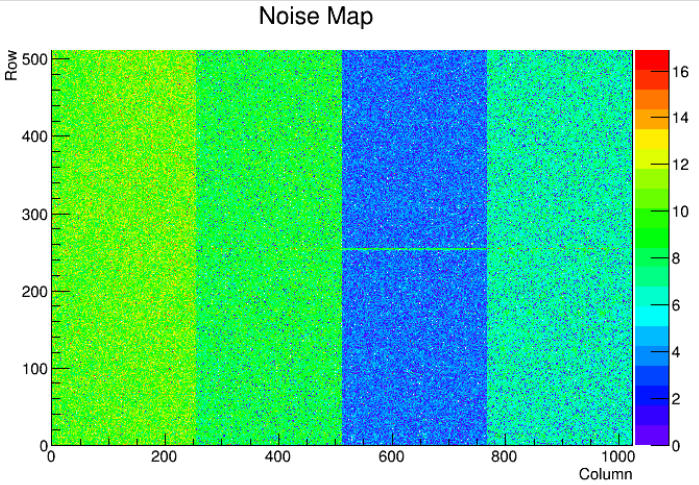
(result from small scale prototype)

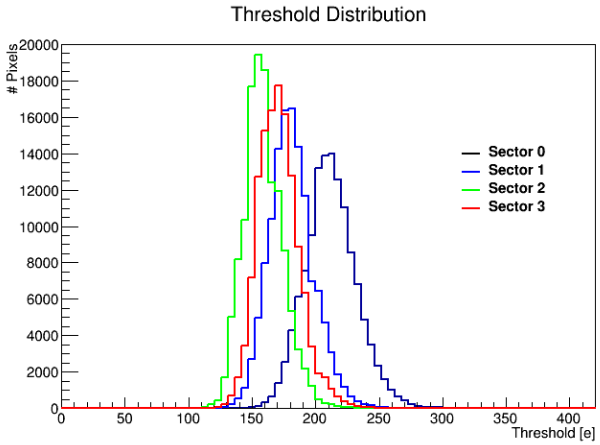


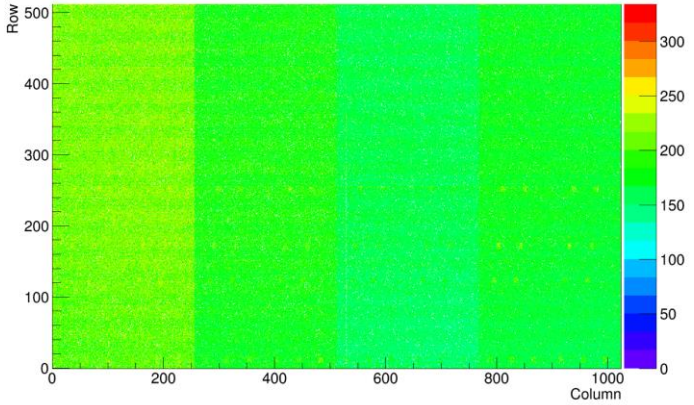
Shaping time ~ 2 µm

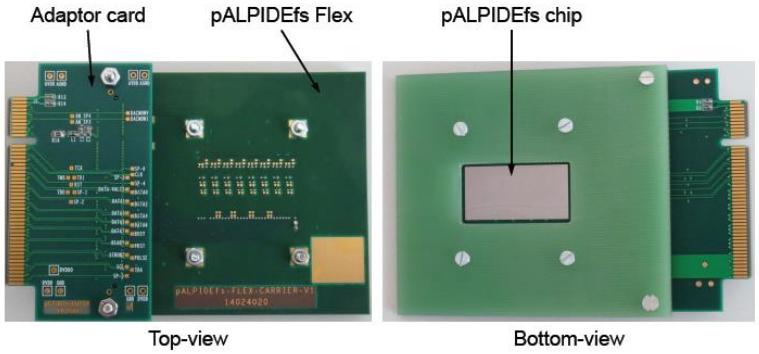
THINNED ALPIDE SOLDERED ON FLEX







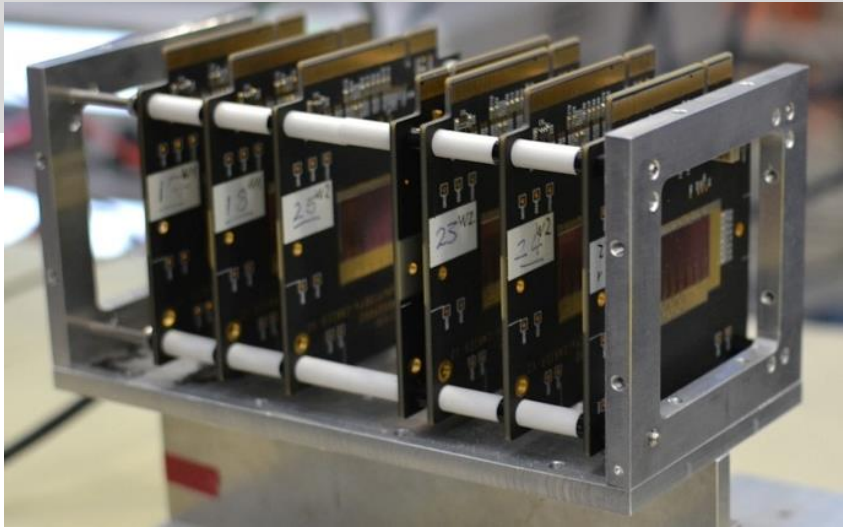


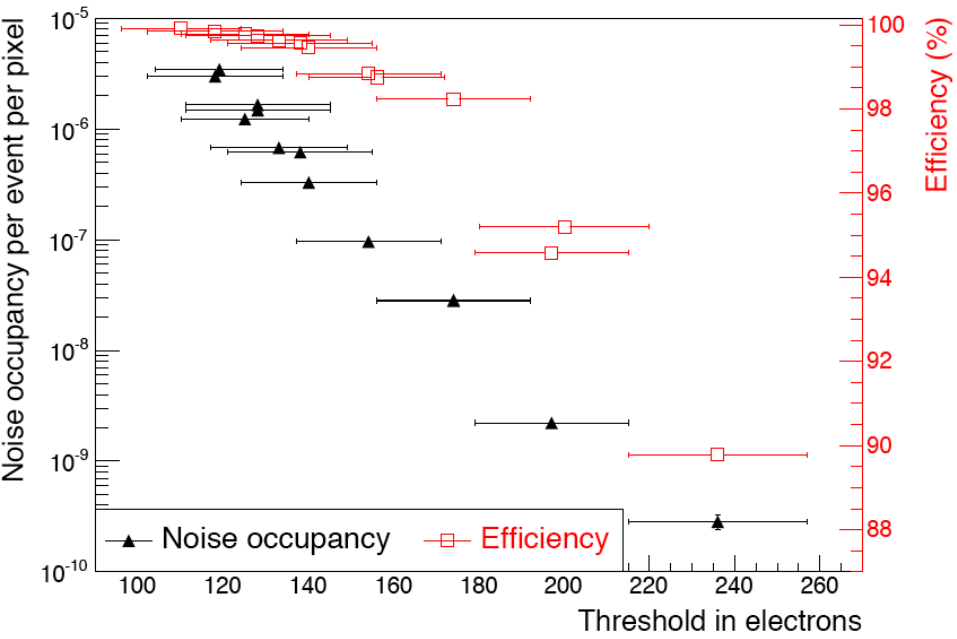


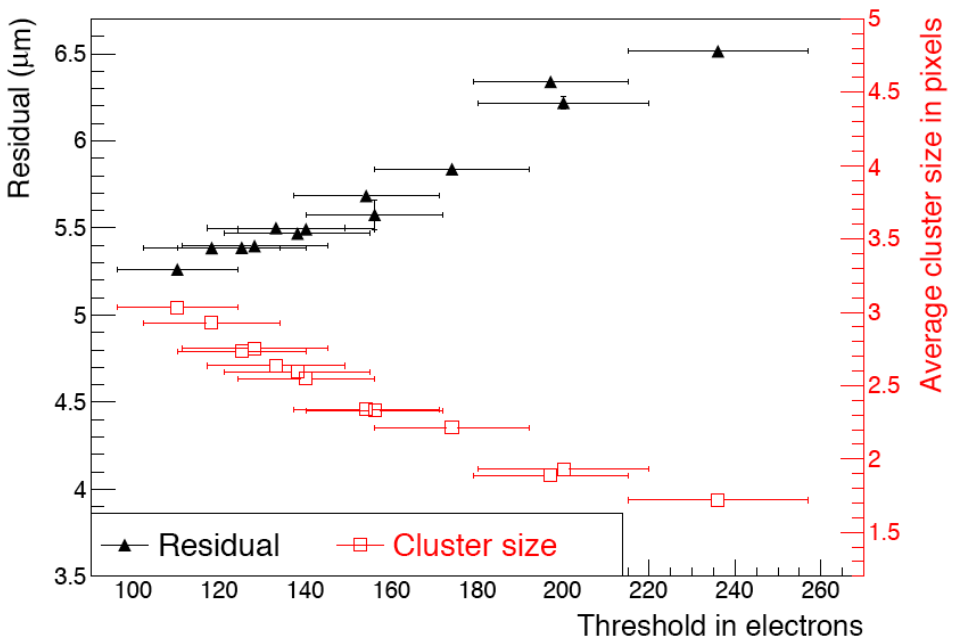
- Thinning and soldering do not affect the performance of the chip
- Band structure reflects different design options in the prototype chip
- Noise << Threshold spread ~ 18 e

ALPIDE test beam results

- 5 – 7 GeV pions at CERN PS
- Telescope of 7 planes
- Zero substrate bias
- Sector 2 (diode reset and 2 µm spacing)



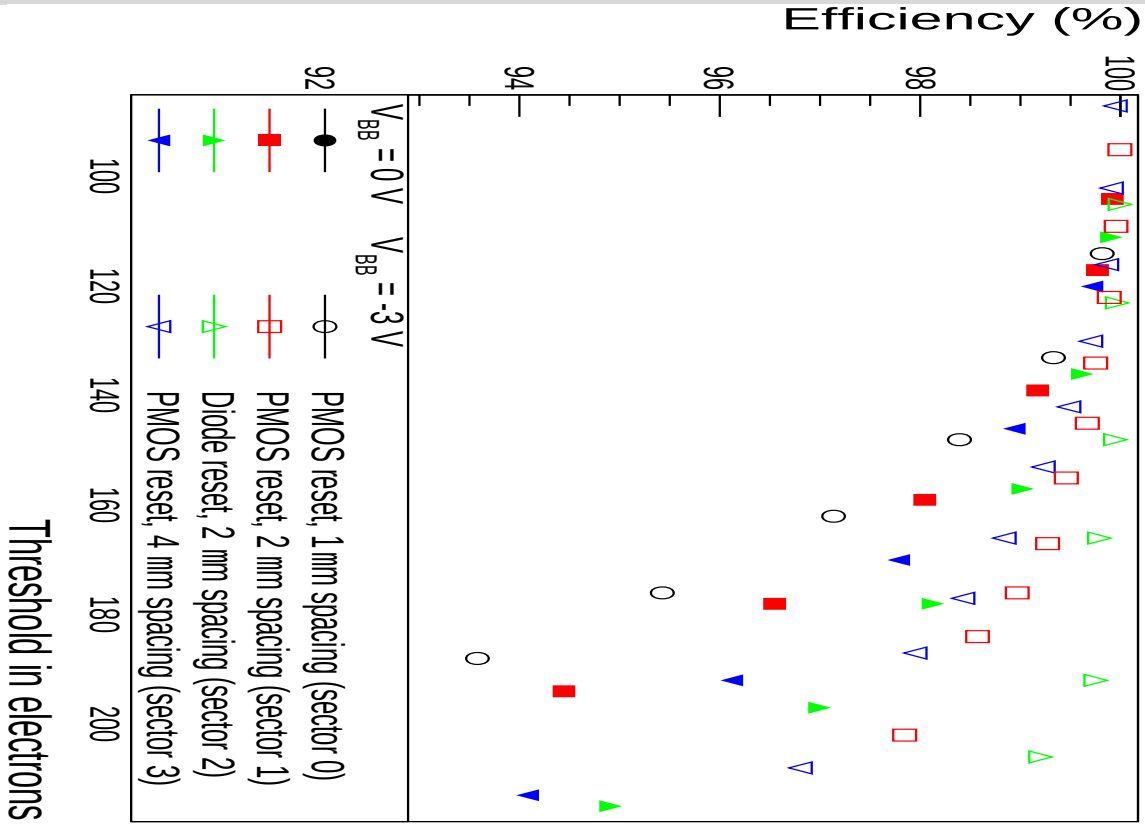




99% efficiency at fake hit rate of 10^{-5} achievable (only 20 pixels masked)

~ 5.5 µm spatial resolution (including tracking error of ~ 3 µm)

SENSOR OPTIMIZATION: IMPORTANCE OF Q/C



If thermal noise from the input transistor dominant, for a given S/N and bandwidth:

$$P \sim \left[\frac{Q}{C}\right]^{-m}$$

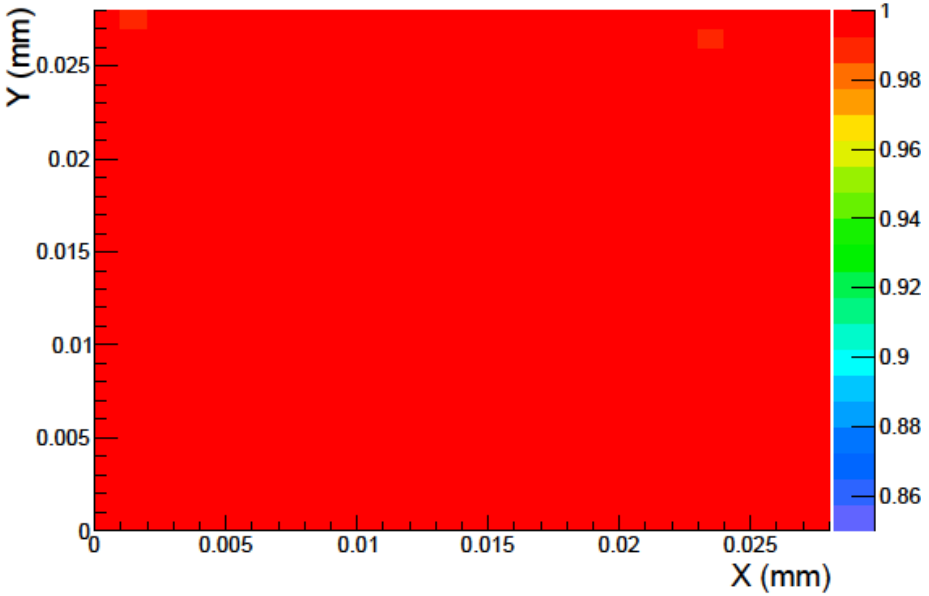
m = 2 for weak inversion
P = analog power
Q = collected signal charge
C = input capacitance

Q/C is THE figure of merit for a sensor

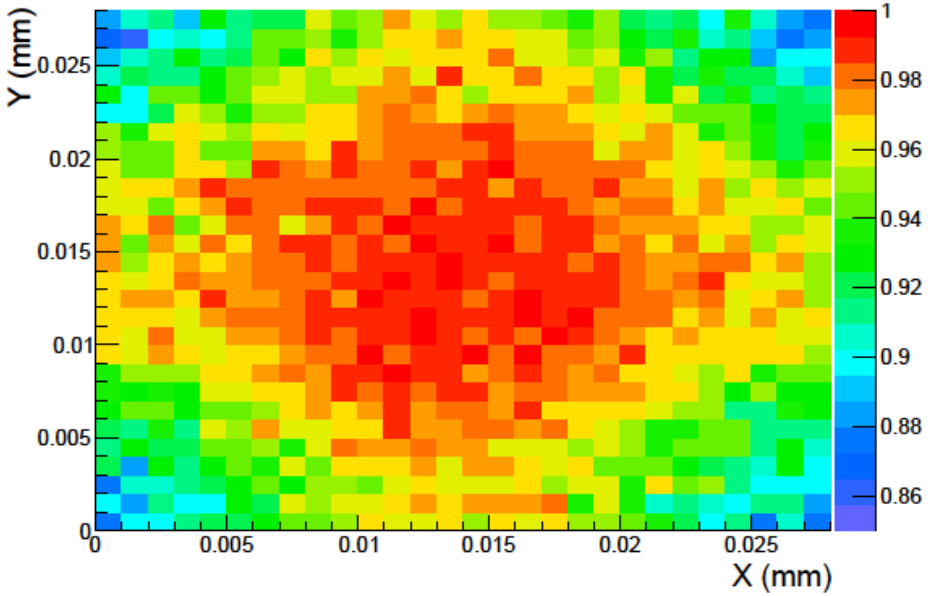
- Changes with different design options in the sensor
- Has a direct system impact, more margin with back bias

DETECTION EFFICIENCY AS A FUNCTION OF HIT LOCATION WITHIN PIXEL

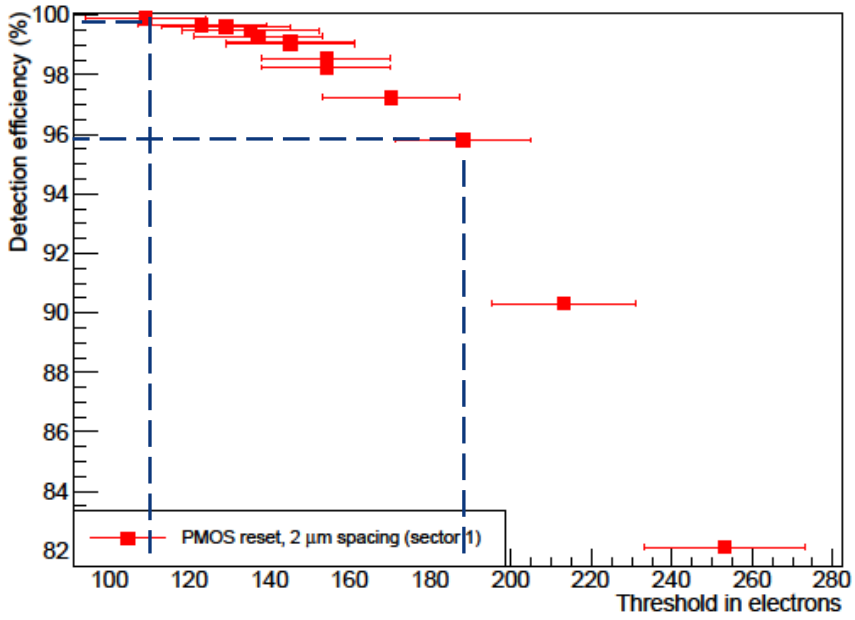
Threshold $109 \pm 15 e^-$



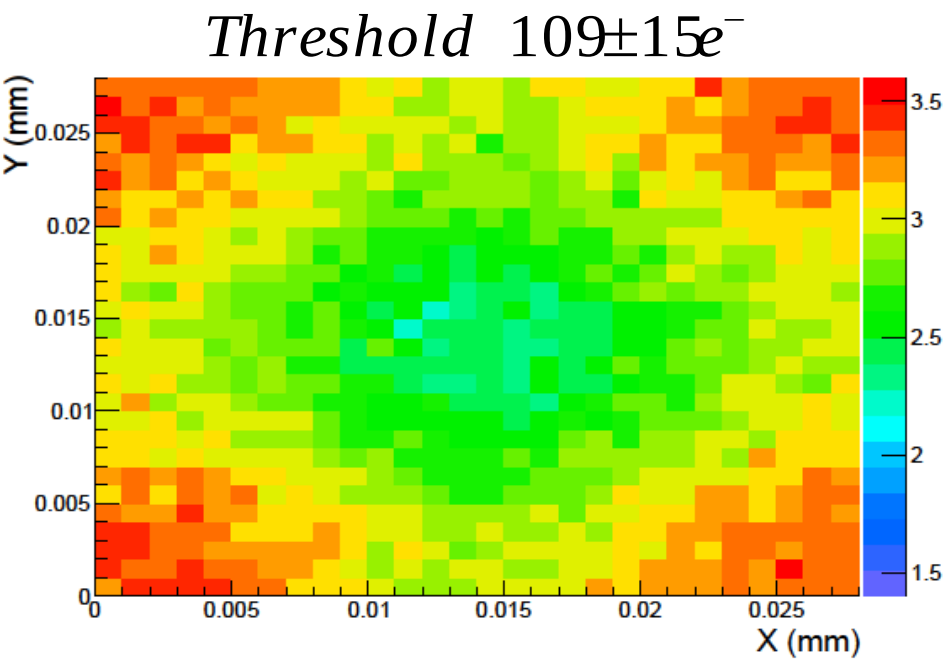
Threshold $188 \pm 17 e^-$

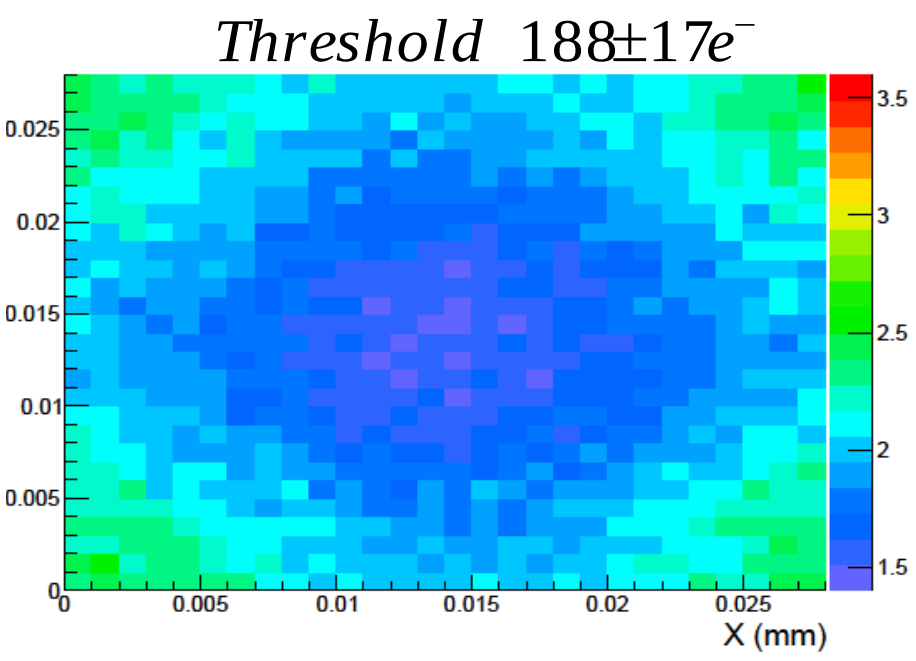


- Better efficiency for lower threshold
- Lower efficiency for higher threshold, start losing hits in the pixel corners



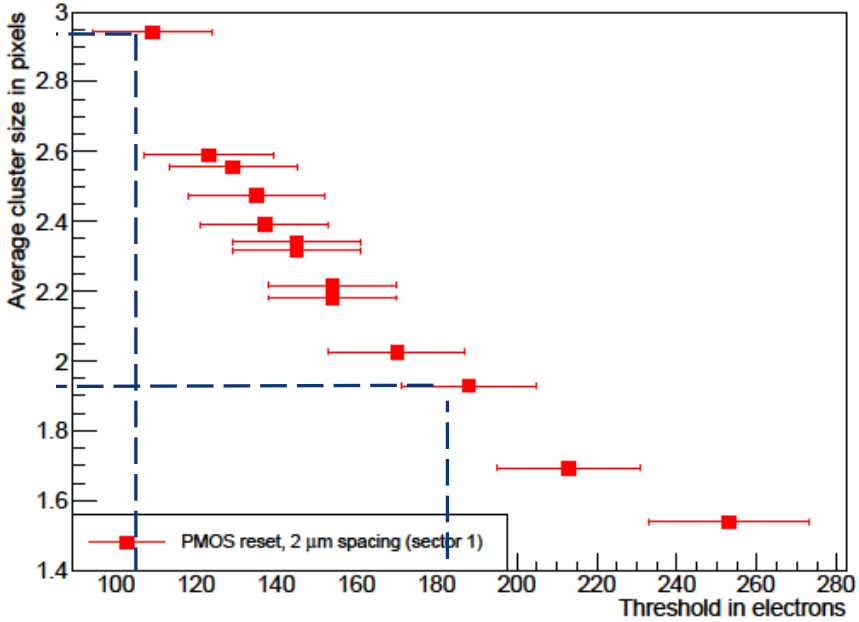
CLUSTER SIZE AS A FUNCTION OF HIT LOCATION WITHIN PIXEL



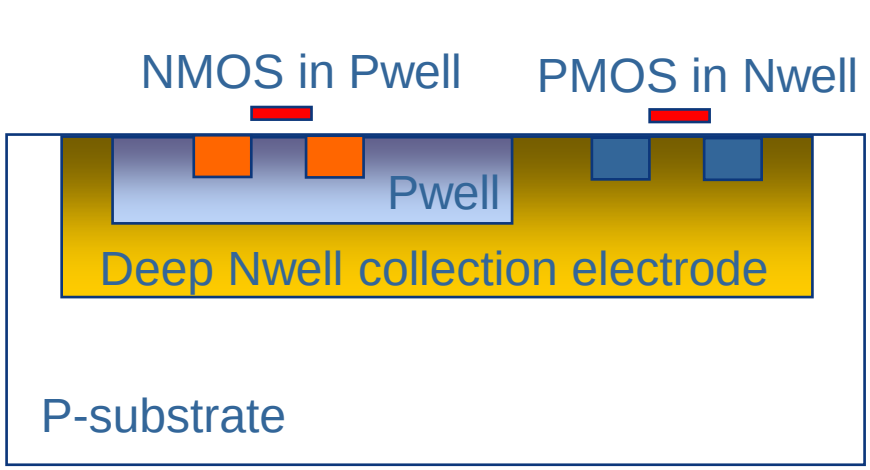


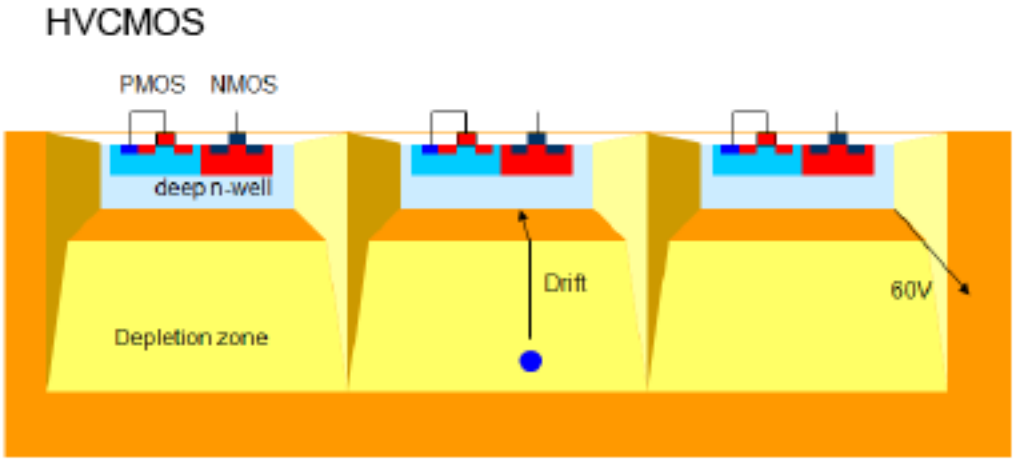
- Larger cluster size for lower threshold
- Smaller cluster size for higher threshold, charge sharing starts in the corners

Good telescope resolution needed for these plots



FULL DEPLETION FOR RADIATION HARDNESS





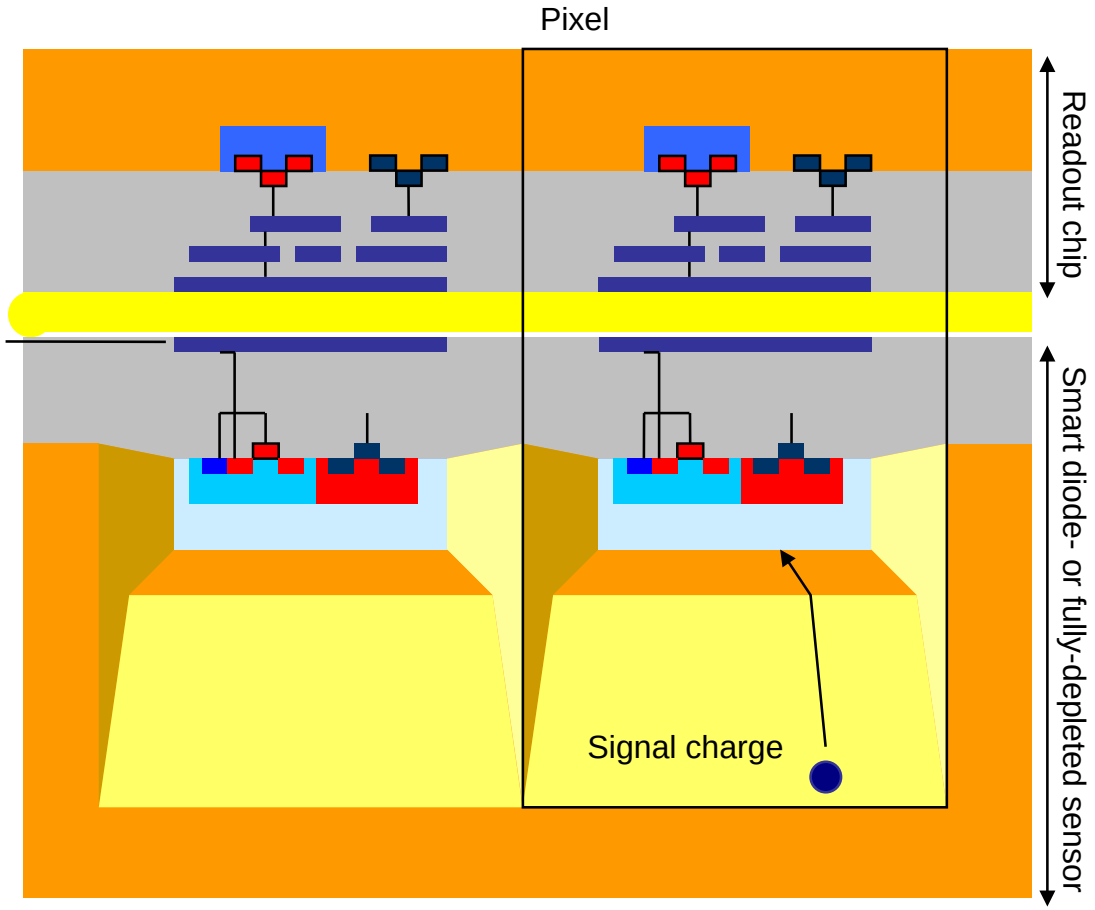
I. Peric

All circuitry in the collection electrode

- Can be done in any CMOS technology with deep Nwell (triple well)
- Apply high reverse substrate voltage (eg -60 V)
- Well protects transistors from HV
- Charge is collected by drift, good for radiation tolerance

- Risk of coupling circuit signals into input
- In-pixel circuit simple in small collection electrode for low C by
  - 'rolling shutter' readout as in MAPS,
  - special architectures (eg LePIX), or
  - use it as smart detector in hybrid solution (cfr ATLAS, I. Peric)

CAPACITIVELY COUPLED PIXEL DETECTOR (CCPD)



Signal >30mV for very thin sensors

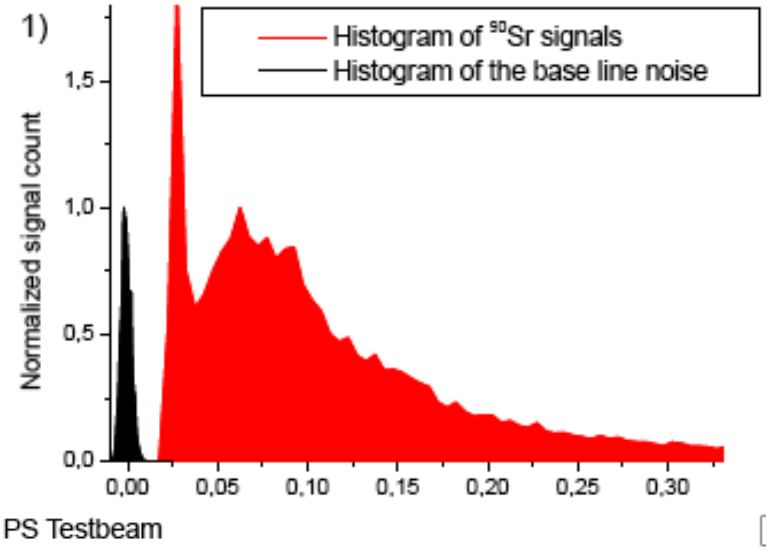
I. Peric

Sensor implemented as HVCMOS
Advantage:
Charge to voltage amplification on the sensor chip
Typical voltage signal ~100mV
Easier capacitive transmission
Can be thinned without signal loss

- Early example next page
- Now versions with FEI4 (eg CPPM GF)

EFFICIENCY and RADIATION TOLERANCE OF CCPD

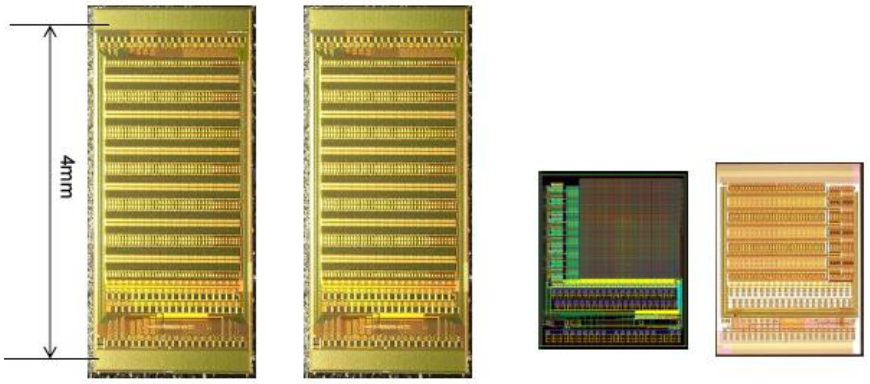
1) CCPDv1: SNR after neutron irradiation at Jozef Stefan Institute 10^{15} n_{eq}/cm^2 ~20 (5C, -55V bias)
(Signal ~ 1180e) (measured 2014) (Unirradiated chip @ -50V bias: 1600e)
2) CCPDv2: works after 862 Mrad (x-ray irradiation CERN) (noise at room temperature 150e)
3) CCPDv1: sub pixel encoding works measured for one pixel – still needs optimization



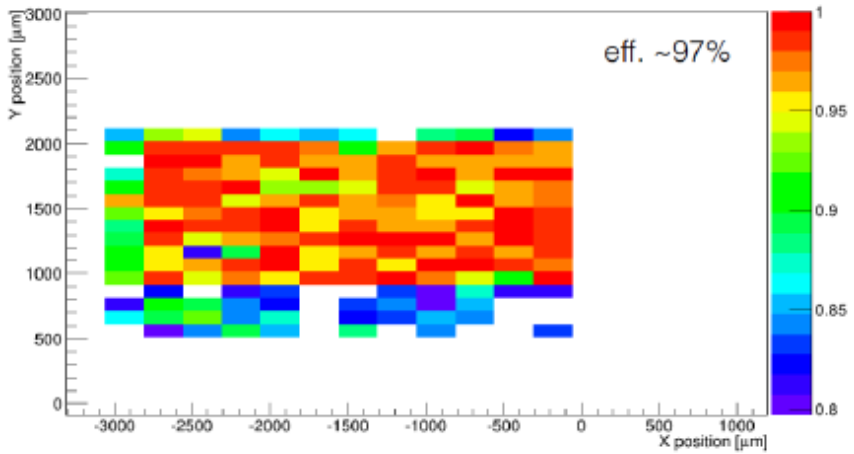
PS Testbeam

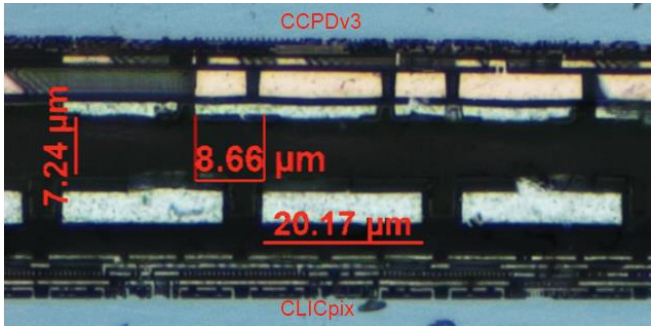
November 2011: CCPDv1
November 2012: CCPDv2
November 2013: CCPv3/CLICPIX
June 2014: CCPv4

I. Peric, CPIX14



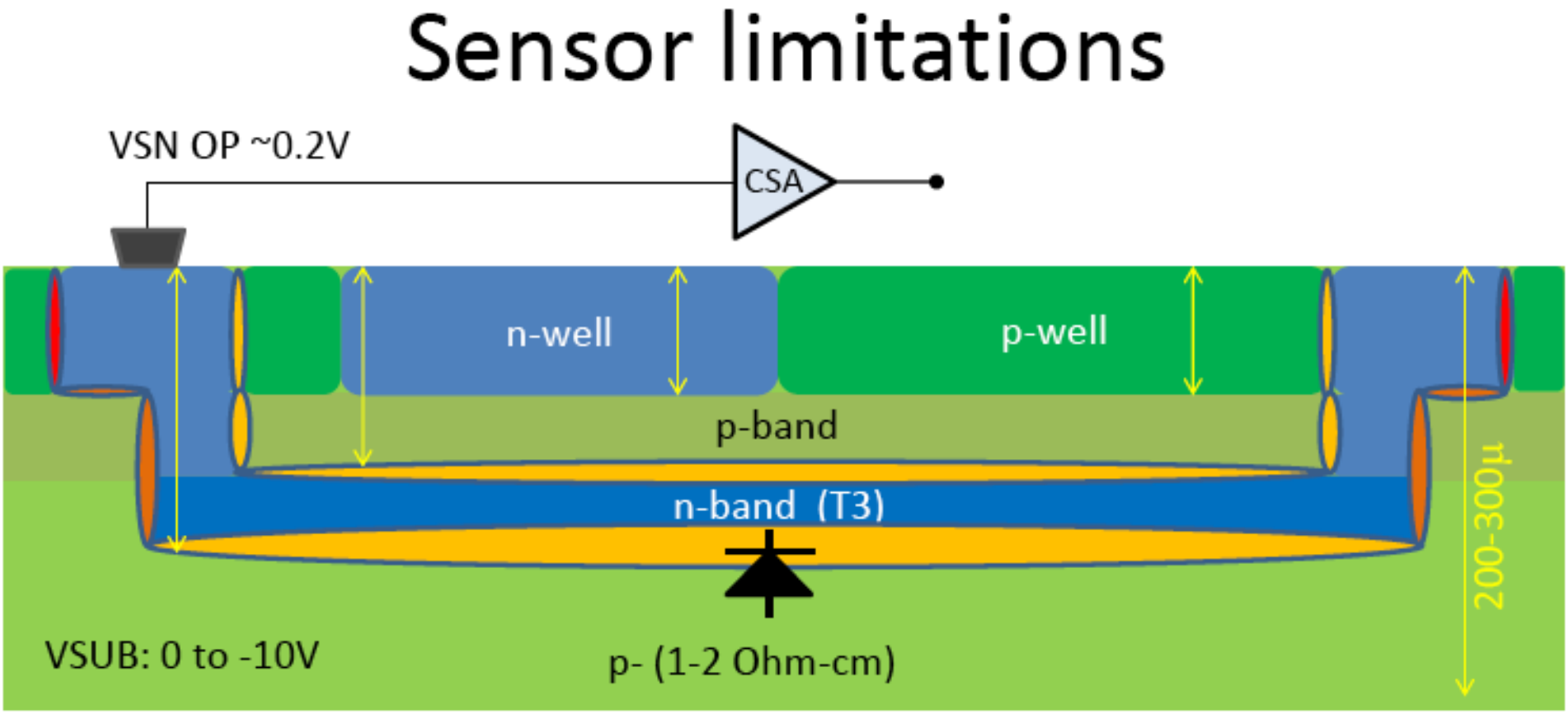
CLICPIX: M. Benoit, CPIX14





Similar developments: SLAC/UCSC (0.35 µm) J. Segal et al.

Deep N-band as collection electrode

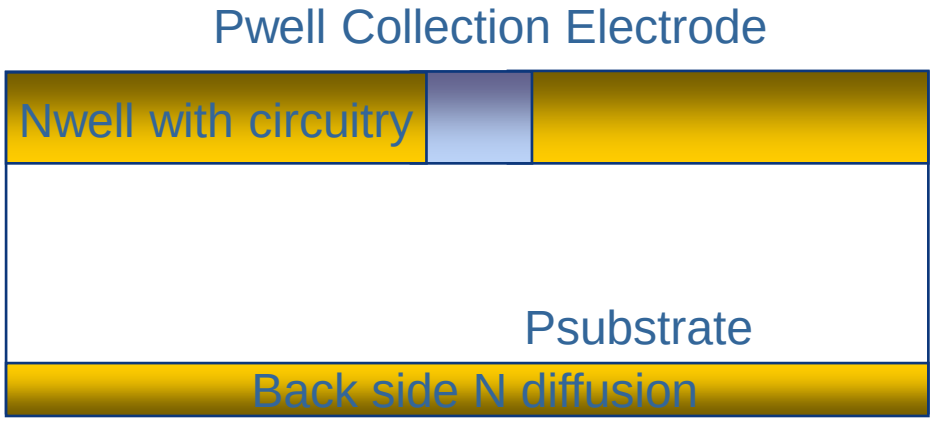


- S/N benefit from higher drift signal component
  - Increase depletion width
  - Increase BV (HR wafer were not available)
- Reasonable to assume surface twin-well junction determines BV
  - Limited silicon simulation data available…
- Intrinsic cap limitations from inner junction
  - CSA is DC-coupled…

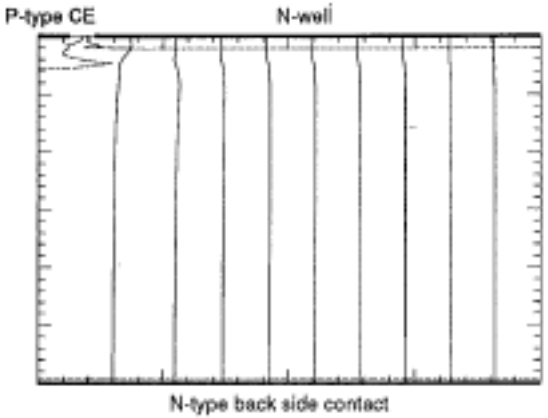
Better shielding from circuit, but large C

Dario Gnani LBNL

FULL DEPLETION WITH JUNCTION ON THE BACK

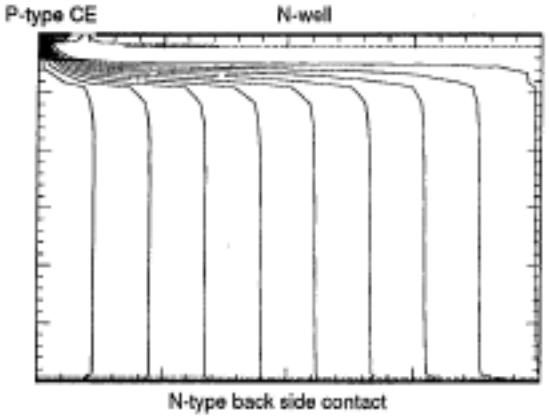


Only a few V on the Nwell diverts the flow lines to the collection electrode

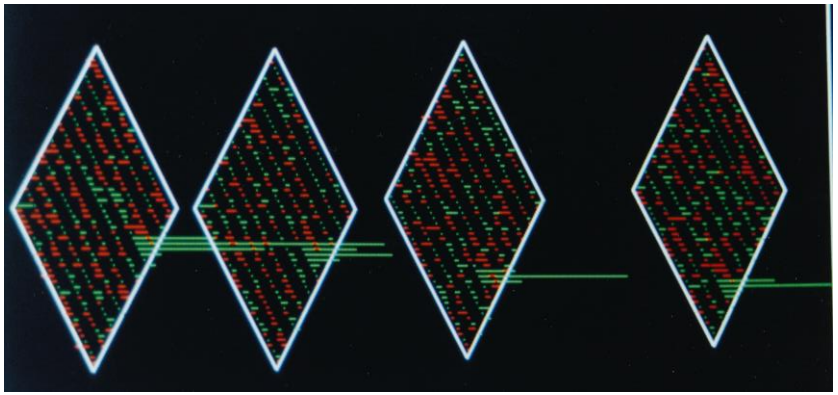


Vnwell = 0 V

- Need full depletion
- Double-sided process for junction termination, not really compatible with standard foundries

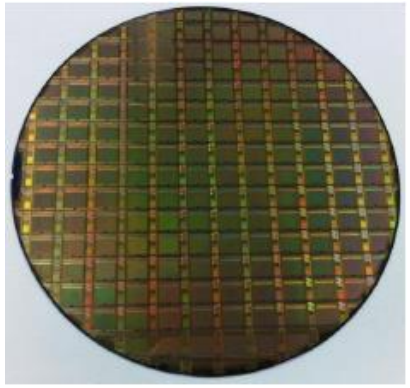


Vnwell = 2 V



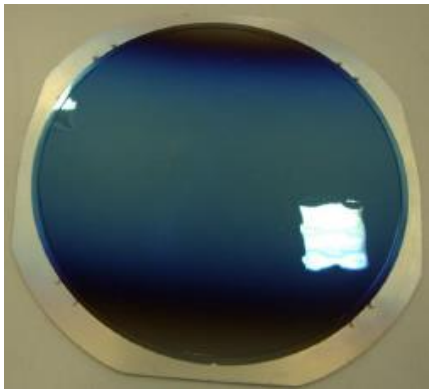
C. Kenney, S. Parker (U. of Hawaii), W. Snoeys, J. Plummer (Stanford U) 1992

OTHER WAYS TO OBTAIN JUNCTION ON THE BACK



Finished CMOS wafer on high resistivity

Wafer thinned to 50 um



Thinned wafer with anti-reflective coating

Chip mounted in camera

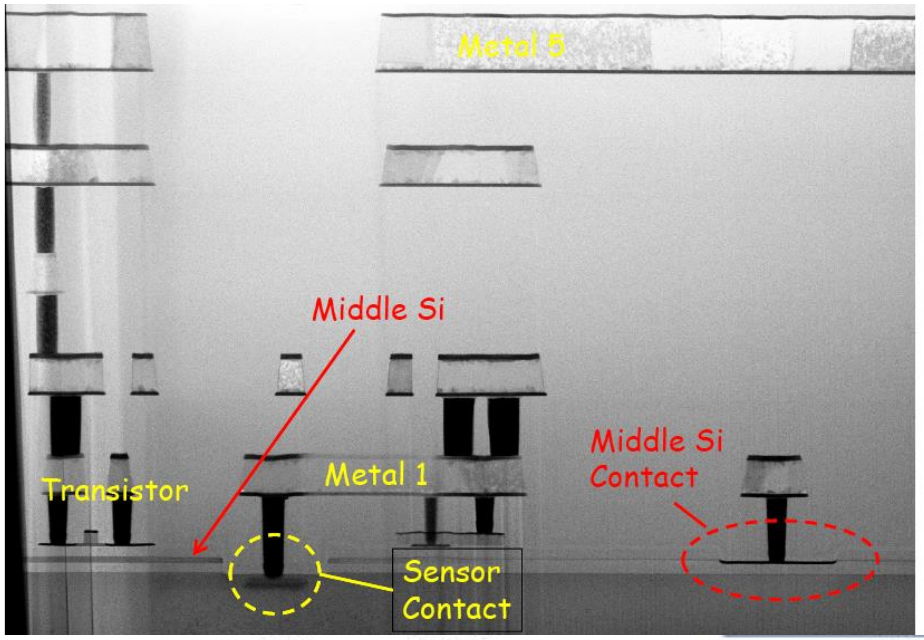
Example: post CMOS wafer thinning & back-side processing

S. Lauxterman CPIX14

Image (raw data)

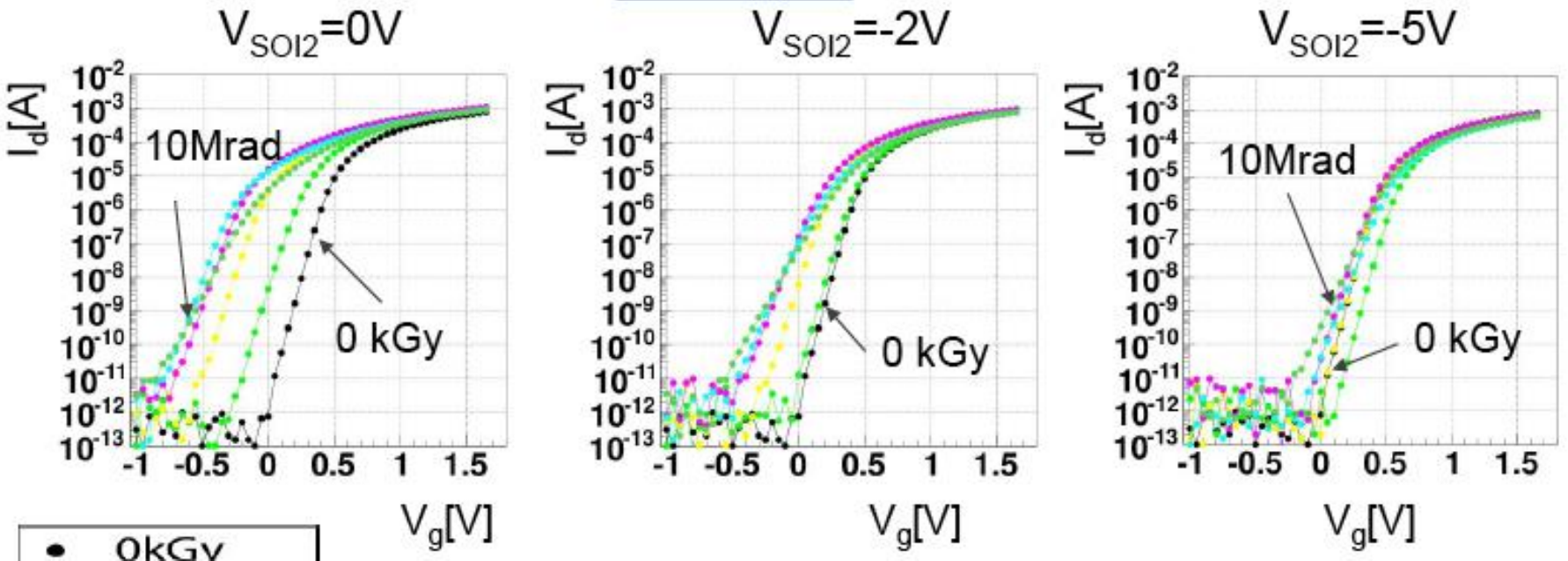
- Several other developments (eg T. Obermann(Bonn) with ESPROS)
- Also epitaxial layer and substrate of opposite type (R. Turchetta)
- In general:
  - Watch die edge/junction termination
  - Radiation tolerance to be investigated/confirmed

Silicon On Insulator (SOI) Y. Arai et al.



- Impressive development
- Now looking at double SOI for radiation tolerance and better back gating properties
- Bias on middle silicon can be used to compensate radiation induced threshold shifts (to 10 Mrad)
- New people in the collaboration:

  N. Teranishi, S. Kawahito, I. Kurachi
- Other presentation on SOI: T. Kishishita, CPIX14 (rad tol transistors ok, leakage current issue)



CONCLUSIONS and OUTLOOK

- Radiation tolerant particle sensors can now be produced in CMOS technologies at lower cost than traditional sensors
- Analog active sensor and modified digital readout chip
  - cfr ATLAS HV/HR CMOS collaboration
  - maintain high Q/C, minimize cross-talk and increase density
  - can choose a different CMOS technology for both
  - cheap bonding or gluing in combination with capacitive coupling
  - Rad tolerant to 10^{15} n_{eq}/cm^2, more development needed
- Integrate the full readout into the sensor:
  - further advantages in terms of assembly, production cost and Q/C
  - adopted for ALICE ITS upgrade with full-scale prototypes in test:
    - MISTRAL: rolling shutter, more conservative and mature
    - ALPIDE: front-end with data driven readout, more aggressive
      Perspective for 20-30 mW/cm^2 and a few µs integration time
    - Beam tests: good position resolution and detection efficiency
    - Tests on irradiated devices ongoing, expect to meet requirements
    -

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CONCLUSIONS and OUTLOOK

Full depletion for higher radiation tolerance

- Junction on the front: in principle possible, but requires high circuit well voltage and ac coupling. Easier with simple circuit.
- Circuit in collection electrode: radiation tolerance demonstrated to ~ 10^{15} n_{eq}/cm^2, but need simple circuit to maintain reasonable C.
- Junction on the back side: need full depletion, but double sided processing incompatible with standard foundries. Some processing alternatives become available, but radiation tolerance still needs verification

Power consumption

- ALPIDE prototype reaches about 100 mV divided over a few pixels
- ~ 300 mV on a single pixel would practically eliminate analog power: it would be sufficient to “turn on” a transistor
- Need more work on architectures to reduce digital power
- Power for transmission of data off-chip may well become dominant

THANK YOU

and also to ALICE ITS and CERN collegues

and to people providing material and suggestions for this presentation

More on ESSCIRC/ESSDERC later

Presentations in Bonn CPIX14.org

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