Construction of a Medium-Sized Schwarzschild-Couder Telescope for the Cherenkov Telescope Array: ***Implementation of the Cherenkov Camera Data Acquisition System***

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ABSTRACT

A medium-sized Schwarzschild-Couder Telescope (SCT) is being developed as a possible extension for the Cherenkov Telescope Array (CTA). The Cherenkov camera of the telescope is designed to have 11328 silicon photomultiplier (SiPM) pixels capable of capturing high-resolution images of air showers in the atmosphere. The combination of the large number of pixels and the high trigger rate (> 5 kHz) expected for this telescope results in a multi-Gbps data throughput. This sets challenging requirements on the design and performance of a data acquisition system (DAQ) for processing and storing this data. A prototype SCT (pSCT) with a partial camera containing 1600 pixels, covering a field of view of 2.5 x 2.5 square degrees, will be assembled at the F.L. Whipple Observatory starting in Fall 2015. We present the design and current status of the SCT data acquisition system.

The SCT Project

- **Medium-sized dual-mirror (9.6-m primary, 5.4-m secondary) Cherenkov telescope.**
- **SiPM-based compact camera. 8° FoV.**
- **Prototype SCT to be built at the F.L. Whipple Observatory (Arizona, USA) starting Fall 2015.**

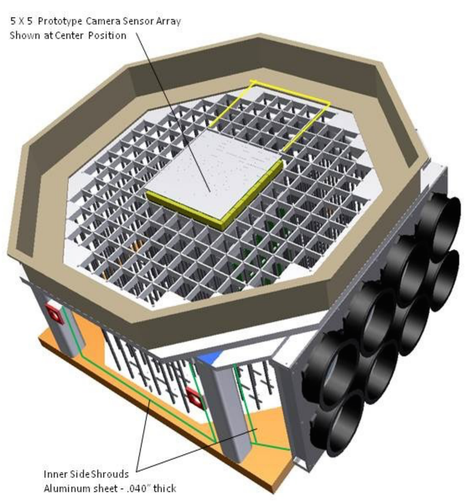

Fig. 1: The SCT camera in its prototype configuration with 5x5 SiPM modules installed in the focal plane.

SiPMs and frontend electronics

- **177 photo-detection modules with 64 SiPM pixels each. The signals are digitized by TARGET ASICs in the frontend electronics (FEE) at 0.5 or 1 GSa/s. A Level-0 trigger is based on 4-pixel clusters.**
- **400 trigger signals are sent to the backplane FPGA and combined in the Level-1 trigger.**

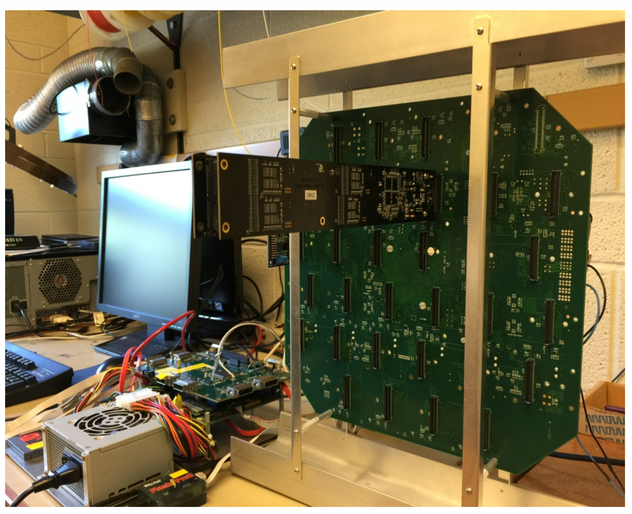

Fig. 2: Backplane with Target 7 FEE module in test setup at Washington University.

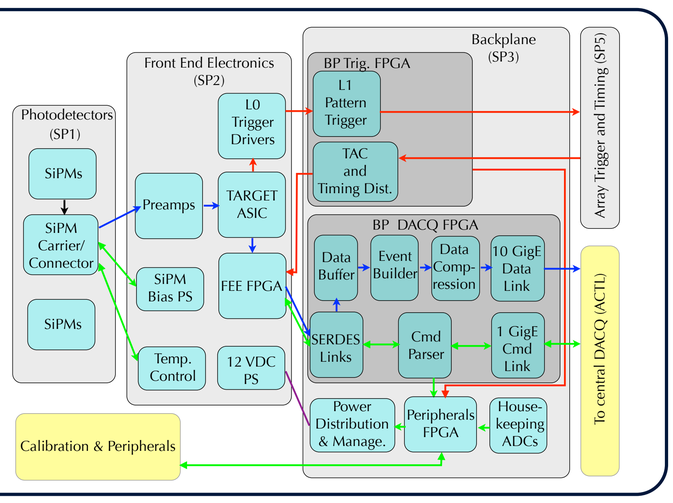

Fig. 3: Schematic representation of the SCT DAQ system from the SiPM detectors to the camera data server.

Camera backplane (BP)

- **The BP submits trigger signals (TACK) to the FEEs that locate the time segment in the analog memory and start digitization.**
- **The digitized waveform is written to the FEE FPGA FIFO and then transmitted over PGP SerDes links to the backplane.**
- **Relative timing is adjusted to ns-level in the backplane.**
- **Timing based on an internal 125 MHz clock phase-locked to a 62.5-MHz oscillator from DIAT and distributed to FEE modules.**
- **Level-1 event builder implemented in commercial Seven Solutions DAQ boards.**
- **The DAQ board currently offers 2x1 Gbps links, which can be upgraded to 10 GBps.**
- **The BP also performs housekeeping, power distribution, control and monitoring functions.**

Camera Data Server (CDS)

- **Will receive and process a ~2.5 kHz raw-event rate.**
- **Each event is 1.42 MB (@ 125 bytes/pixel). The throughput is ~3.5 GB/s per SCT.**
- **4 x 10 Gbps optical fibers transmit data from the camera over UDP links.**
- **Event fragments are buffered for up to 0.5 seconds (~1.8 GB buffer depth).**
- **Event fragments are assembled into full events using the CTA event format and transmitted to the central CTA DAQ servers.**
- **The prototype CDS computer is a Dell PowerEdge R730xd.**

Next steps

- **Backplane tests are underway in Washington University in St. Louis, USA.**
- **First integration and throughput tests with Camera Data Server software to start in mid-August.**
- **DAQ software and hardware to be available for the tests and installation of the prototype SCT, scheduled to start in Fall 2015.**

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