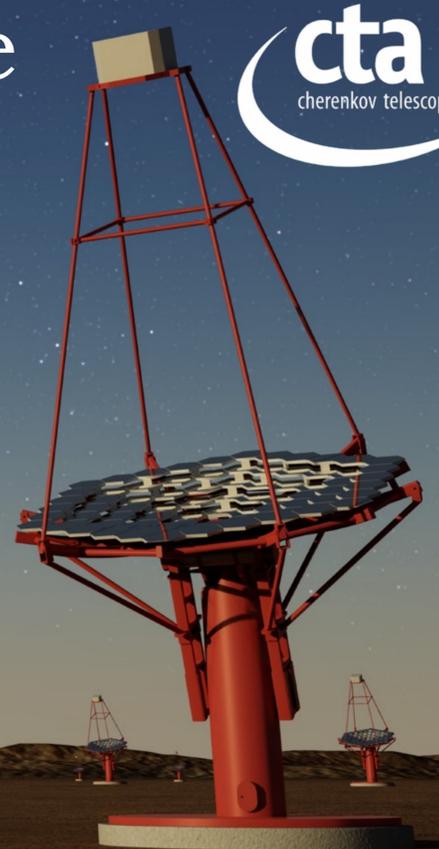


TARGET: toward a solution for the readout electronics of the Cherenkov Telescope Array

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ABSTRACT

TARGET is an application specific integrated circuit (ASIC) designed to read out signals recorded by the photosensors in cameras of very-high-energy gamma-ray telescopes exploiting the imaging of Cherenkov radiation from atmospheric showers. TARGET capabilities include sampling at a high rate (typically 1 GSample/s), digitization, and triggering on the sum of four adjacent pixels. The small size, large number of channels read out per ASIC (16), low cost per channel, and deep buffer for trigger latency ($\sim 16 \mu\text{s}$ at 1 GSample/s) make TARGET ideally suited for the readout in systems with a large number of telescopes instrumented with compact photosensors, like multi-anode or silicon photomultipliers, combined with dual-mirror optics. Possible advantages of such systems are better sensitivity, a larger field of view, and improved angular resolution. The two latest generations of TARGET ASICs, TARGET 5 and TARGET 7, are soon to be used for the first time in two prototypes of small-sized and medium-sized dual-mirror telescopes proposed in the framework of the Cherenkov Telescope Array (CTA) project. In this contribution we report on the performance of the TARGET ASICs and discuss future developments.

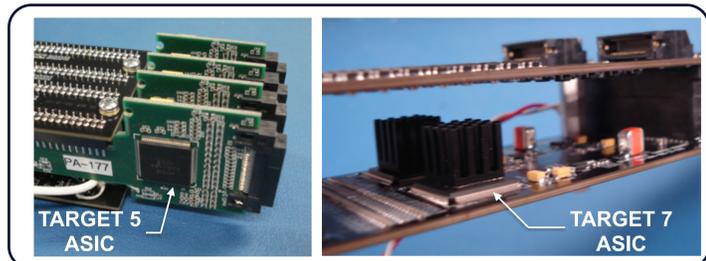


Fig. 2: TARGET 5 and 7 ASICs on the front-end-electronics modules in cameras of prototype telescopes proposed for CTA, left — GCT (De Franco et al. poster 954), right — SCT (Otte et al. poster 1052).

ASIC ARCHITECTURE: TARGET 5 AND 7

Sixteen channels are processed both for trigger formation, as well as analog sampling. A timebase generator controls the sampling of signals into dual groups of 32 sampling cells. Ping-pong operation transfers samples from one group of 32 to storage while the other group is sampling, with the roles reversed in the next half sampling cycle. These groups of 32 storage cells can be randomly accessed on demand for readout by an onboard Wilkinson Analog-to-Digital Converter (ADC) on 32 samples in parallel for all 16 channels. Individual converted samples may then be selected and serially transmitted off-ASIC on all 16 channels concurrently. In parallel the analog signals from groups of 4 adjacent channels are used to form triggers that are provided to off-ASIC high-level logic to generate the readout requests. Sampling, digitization, and triggering are highly configurable, with operating parameters programmed through a serial-parallel interface.

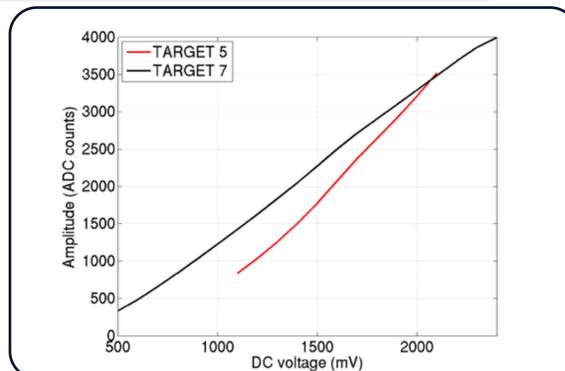


Fig. 3: DC transfer function.

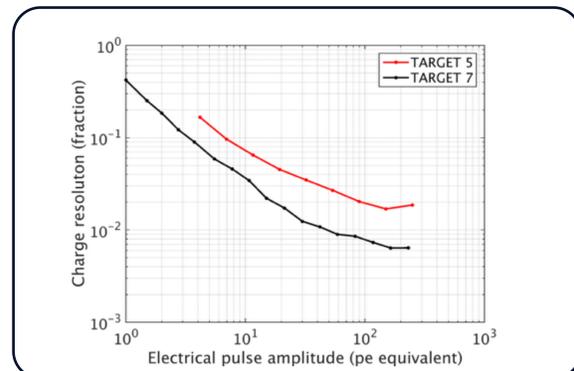


Fig. 4: Charge resolution (ASIC only).

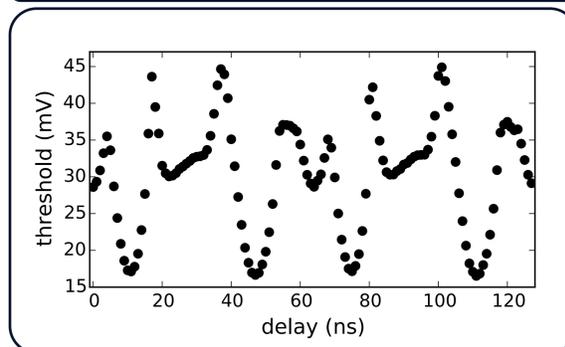


Fig. 5: Trigger threshold in TARGET 5 for a fixed ASIC configuration as a function of delay between input pulse signal and sampling clock, over two periods of the 64-ns sampling clock.

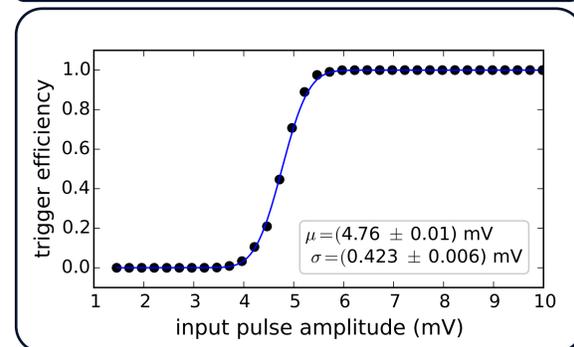


Fig. 6: Example of trigger performance in TARGET 5 with sampling disabled. Efficiency as a function of input pulse amplitude, and best-fit model with threshold μ and trigger noise σ (4 mV \sim 1 pe).

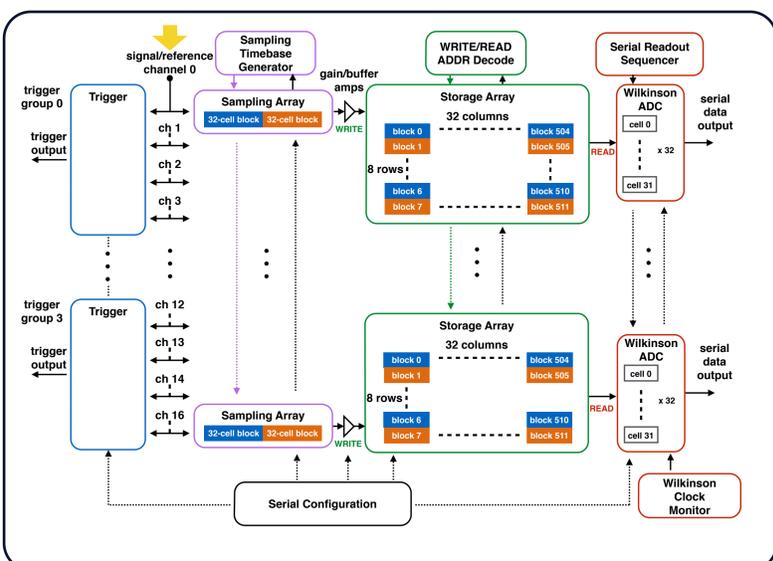


Fig. 1: Functional block diagram of the TARGET 5/TARGET 7 ASICs, with key components shown.

ACKNOWLEDGEMENTS

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SUMMARY AND OUTLOOK

Modifications to the sampling and Wilkinson clock generation, along with improved digitizer biasing, provided a dramatic improvements in performance from TARGET 5 to TARGET 7 (Fig. 3 and 4). The trigger performance is limited by intrinsic coupling between sampling and triggering (Fig. 5), that was not addressed by additional gain stages in the trigger circuit in TARGET 7.

A new generation of ASICs was manufactured and is currently under evaluation. TARGET C, for sampling and digitization, is equivalent to TARGET 7 without trigger. A separate companion ASIC for triggering, CCTV, is expected to provide a performance equivalent to TARGET 5 with sampling disabled (Fig 6).

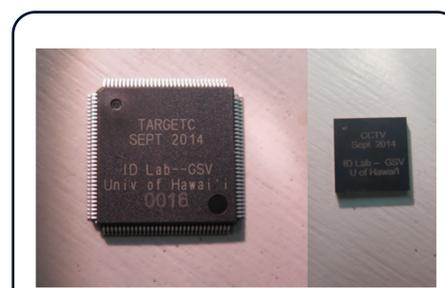


Fig. 7: TARGET C and CCTV ASICs.