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Development of integrated circuits in 3DIC technology at FNAL

Grzegorz DEPTUCH

Fermi National Accelerator Laboratory, Batavia, IL, USA

email: deptuch@ieee.org

on behalf of the FERMILAB
ASIC design group:
R. Yarema ldr.,
G.Deptuch, J.Hoff, A.Shenai, M.Trimpl, T.Zimmerman
and:
M.Demarteau, R.Lipton, W.Wester and others

1) information where we are with work using 3DIC technology at FERMILAB,
2) *discussion of perspectives and introduction to future steps in the exploration of 3DIC,*
3) *a few words about high density bonding and SoI monolithic detectors,*
4) *Discussion (comments and suggestions more than welcome)*

FNAL detector/electronics R&D policy

- **approach taken at Fermilab for detector/electronics R&D:**
  - to pursue those technologies that look to be the most promising despite the fact that some seem very challenging,
  - to work with longer time horizon within the base of existing manpower and competences,
  - to search for a broad range of applicability, balancing between generic detector R&D vs concept/application driven R&D,
  - to establish collaborative efforts as much as possible,

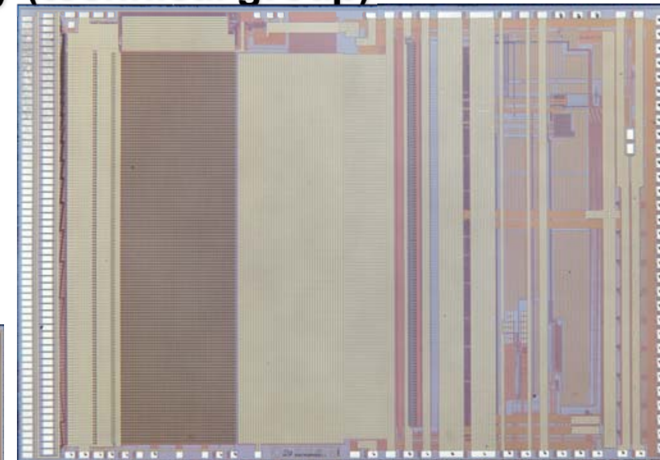
- **directions of detector R&D for future:**
  - precision,
  - speed and data throughput,
  - processing in-situ (close to source),
  - radiation hardness,

  } generally the performance is required to go about one order of magnitude beyond what has been achieved to date

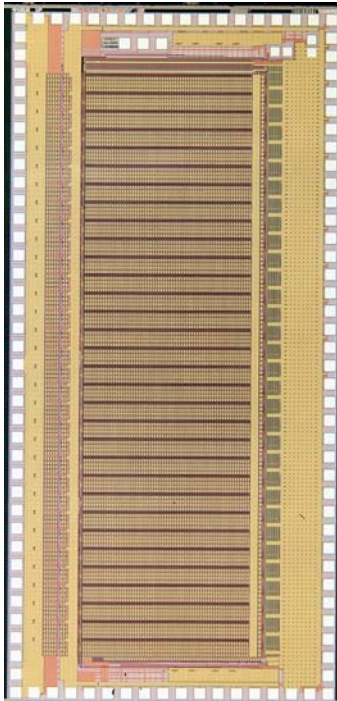
- **goals and means:**
  - under current circumstances the goal is to convey a coherent det./electronics R&D under an umbrella of generic multiaspect R&D,
  - among others the objectives are to be present in upgrade of the LHC experiments (detectors, ROCs, powering schemes, auxiliary ICs), ILC,

ASIC Expertize

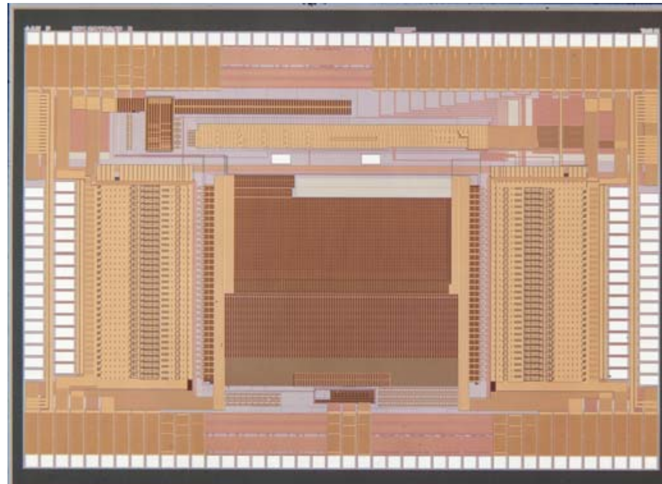
- **FERMILAB capabilities:**
  - design of analog and digital ASICs (group of 5 designers),
  - in-house tests, wafer probing, radiation tests, robotic testing (testing group),
  - tests support, board level design, layout, assembly (technical group)
- **Past ASIC experience:**
  - designs fabricated in numerous silicon foundries: OKI, MITLL, TSMC, IBM, AMS, Agilent, Atmel
  - designs for KTEV, CMS, CDF, BTEV, D0, ILC, NoVA, SNAP



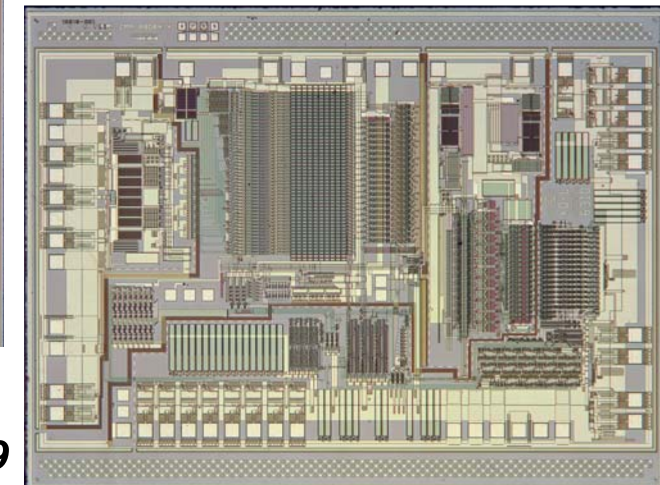
SVX4



NOVA1



DCAL



QIE9

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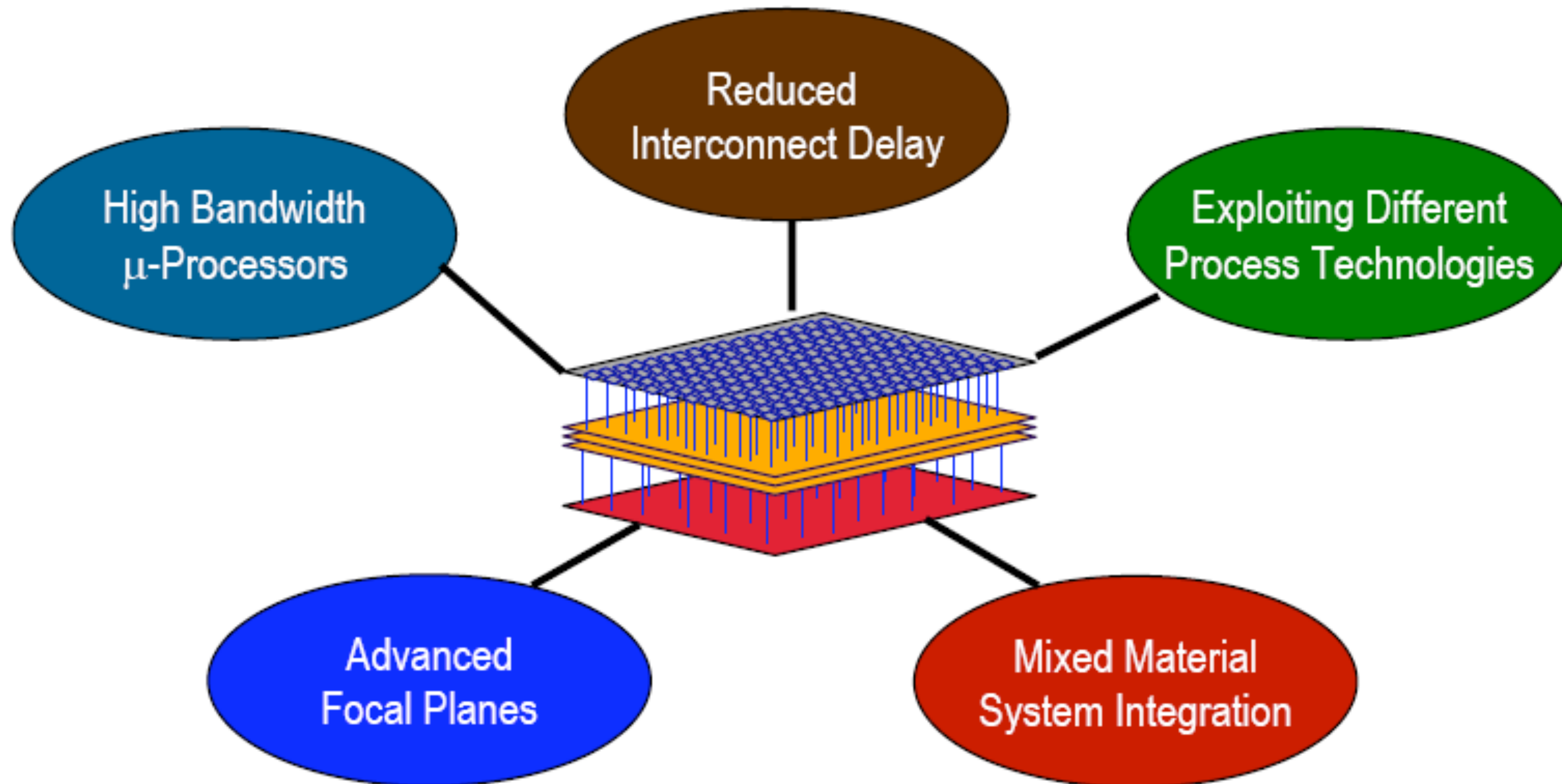
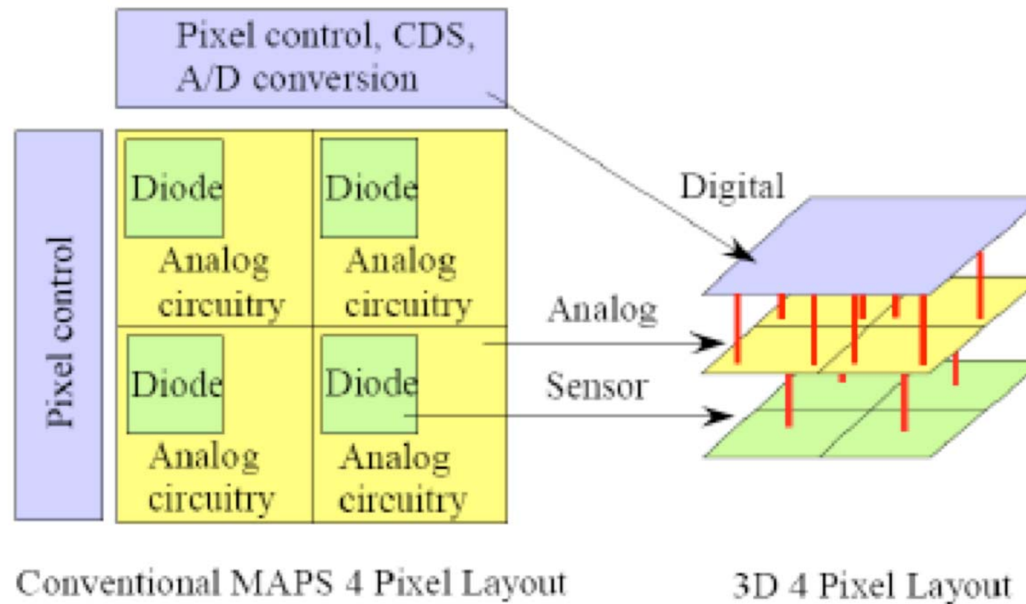
Motivation for 3DIC technology



from Craig Keast MITLL

Motivation for 3DIC technology



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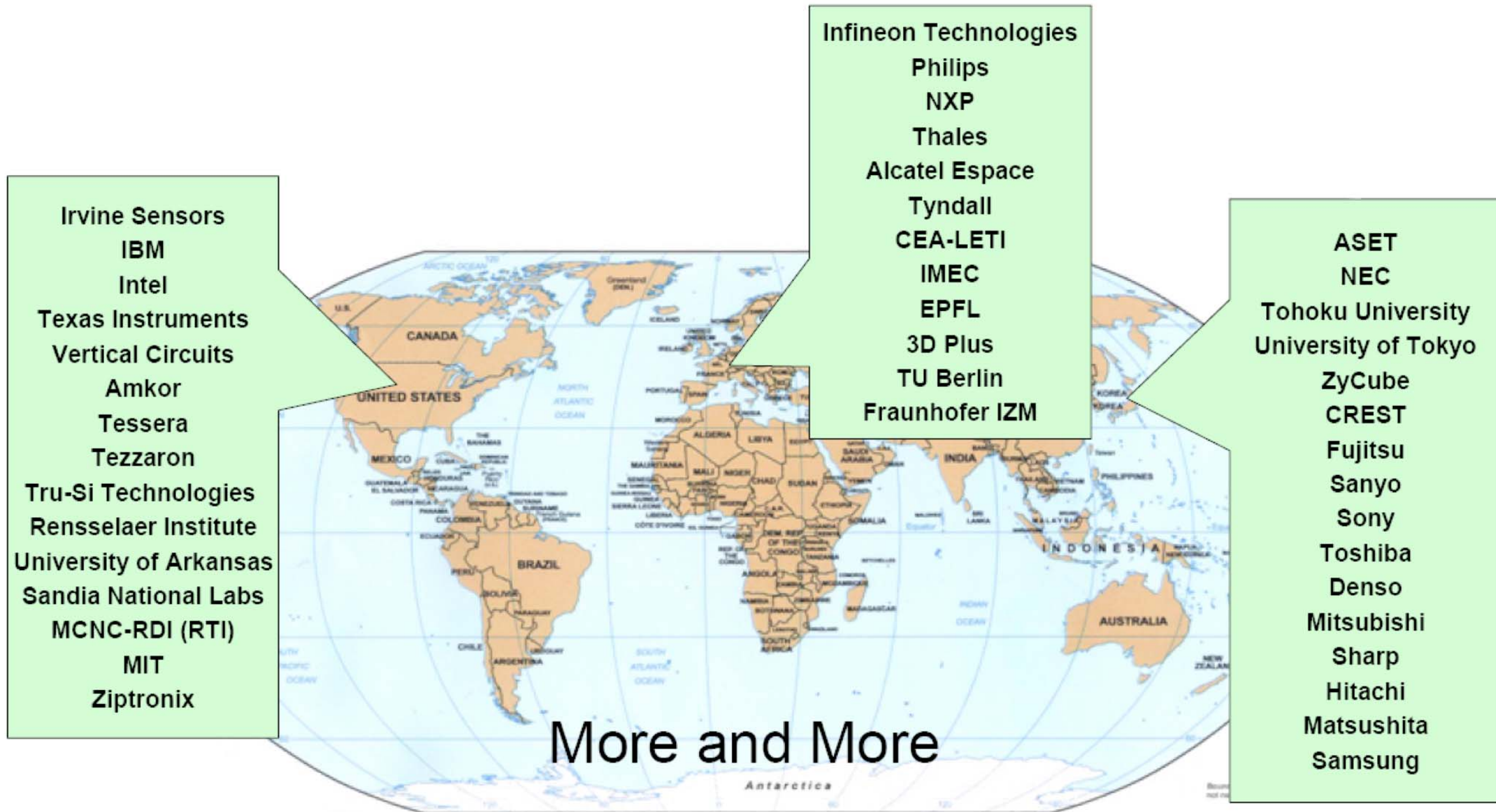
Motivation for 3DIC technology



from EMC3D

3DIC is already an industry standard,

Motivation for 3DIC technology

- **Fermilab 3D work started in 2006 – first major talk at Ringberg, May 2006**

R. Yarema, *Fermilab Initiatives in 3D integrated Circuits and SOI Design for HEP*, ILC Vertex Workshop, Tegernsee, Germany, May 29-31, 2006

Rather successful attempt to work out a common platform of technology providers and users from the scientific community for the 3DIC effort.

- **Previous 3D-oriented work at Fermilab:**
  - **MIT LL – 3D circuit design for ILC,**
  - **IZM – wafer thinning,**
  - **RTI – wafer bonding,**
  - **OKI – SOI monolithic detector/readout.**

First submission to the process with TSVs (through silicon vias)

- **New activities in 2008 – will focus more on industrial vendors:**
  - **OKI – new SOI detector design,**
  - **MIT LL – new 3D design with on board ADCs.**
  - **Tezzaron (Chartered Sem.) – 3D circuit design.**
  - **Ziptronix – low mass bonding.**

First run through a fully commercial 3dIC technology provider

Summary of ‘done and planned’ in IC

- **work done and work in progress:**
  - **design of 3D integrated readout circuit for ILC** ***(VIP1 vertically integrated pixel) in 0.18 μm MITLL 3DM2 process (Oct.2006) – tests underway (test infrastructure developement takes time),***
  - **design of SoI detector/readout system for imaging** ***(MAMBO Monolithic Active Matrix with Binary cOunters) in 0.15 μm OKI process (Dec.2006) – tests done,***
  - **design of SoI detector/readout system for imaging** ***(MAMBO2 in 0.20 μm OKI process (Jan.2007) – one lot with bad CS2 for electronics testing already available, second lot with corrected CS2 expected within 1 month,***
  - **design of 3D integrated readout circuit for ILC** ***(VIP2 vertically integrated pixel) in 0.15 μm MITLL 3DM3 process (Sept.2008) – should have started design already,***
  - **design of 3D integrated readout circuit for ILC/SLHC/imaging FERMILAB hosted** ***0.13 μm Tezzaron/Chartered process (Dec.2008/Jan.2009) 2 tier low cost processing– reticle booking almost finished.***

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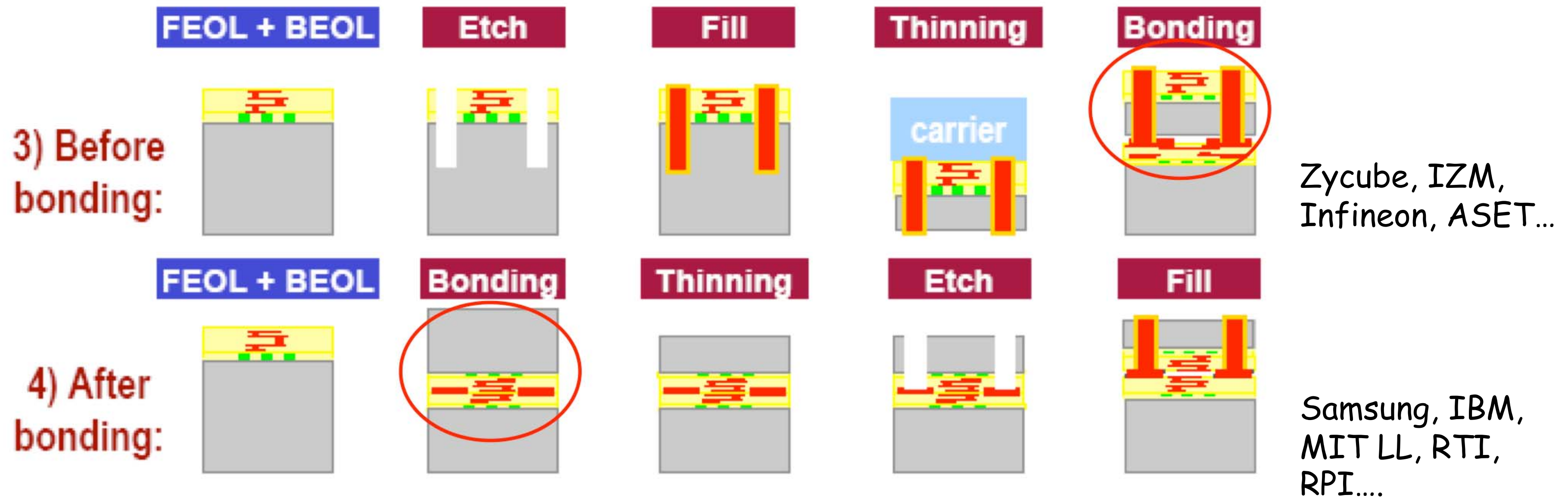
Approaches for TSVs

Via last approach occurs after wafer fabrication and either before or after wafer bonding



Zycube, IZM, Infineon, ASET…

Samsung, IBM, MIT LL, RTI, RPI….

Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

Basically wafers from different processes/vendors could be used as via creation is a postprocessing operation.

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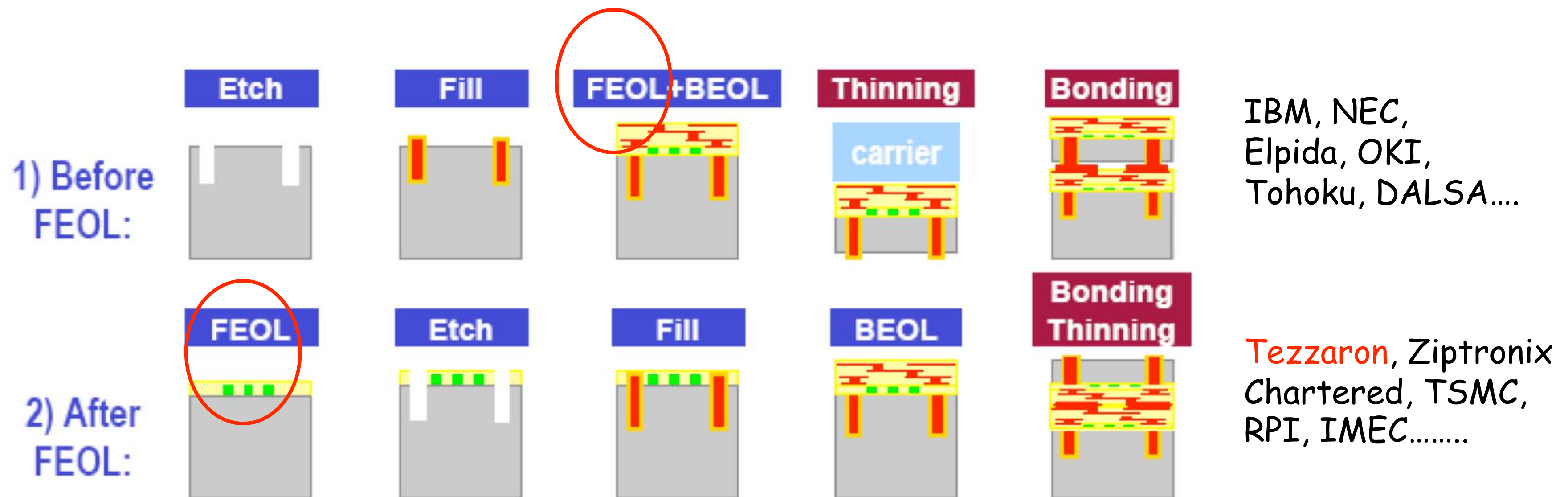
Approaches for TSVs

Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing



Vias are fabricated as a part of the process flow.

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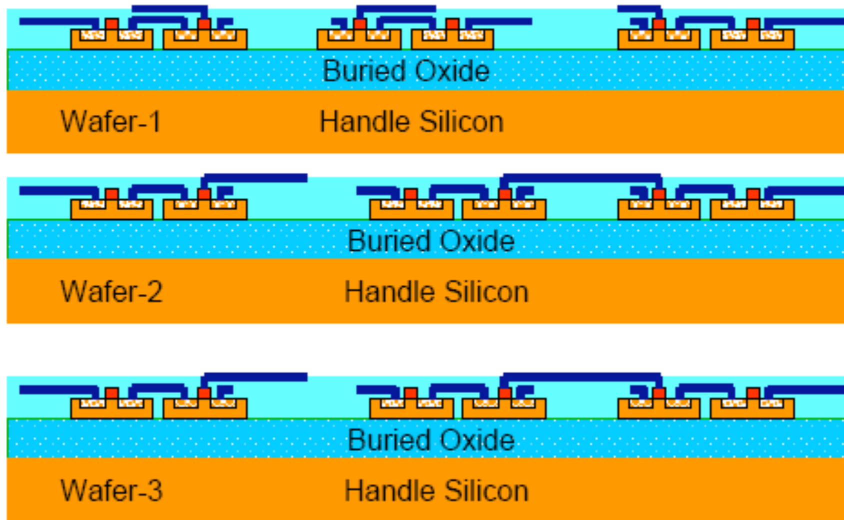
MITLL 3DM2 flow:

- 3 tier chip; 3DM2 includes 2 *"digital"* 180-nm FDSOI CMOS tiers and 1 RF 180-nm FDSOI CMOS tier
- 11 metal layers including: 2-μm -thick RF backmetal, Tier-2 backmetal

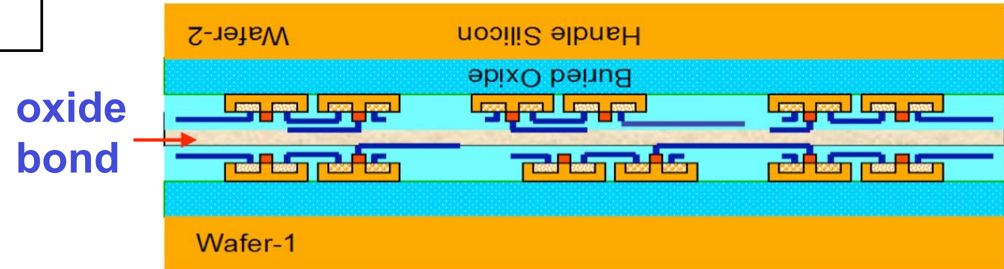
Step 1: Fabricate individual tiers



In principle wafer 1 could also be bulk

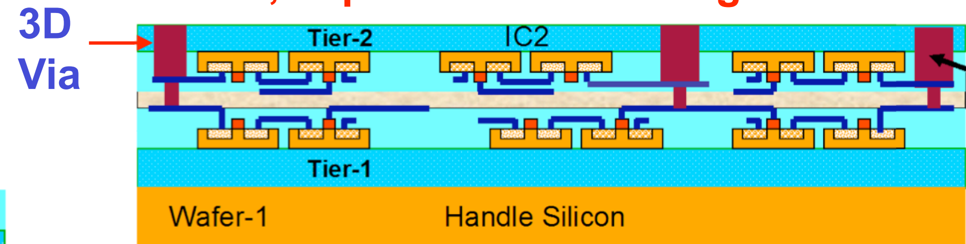
Step2: Invert, align, and bond wafer 2 to wafer 1

oxide bond

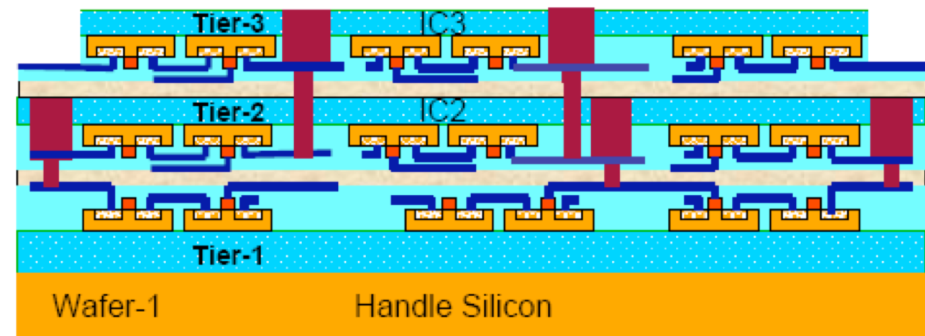


Step 3: Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via



Step 4: Invert, align and bond wafer 3 to wafer 2/1, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3, etch bond pads



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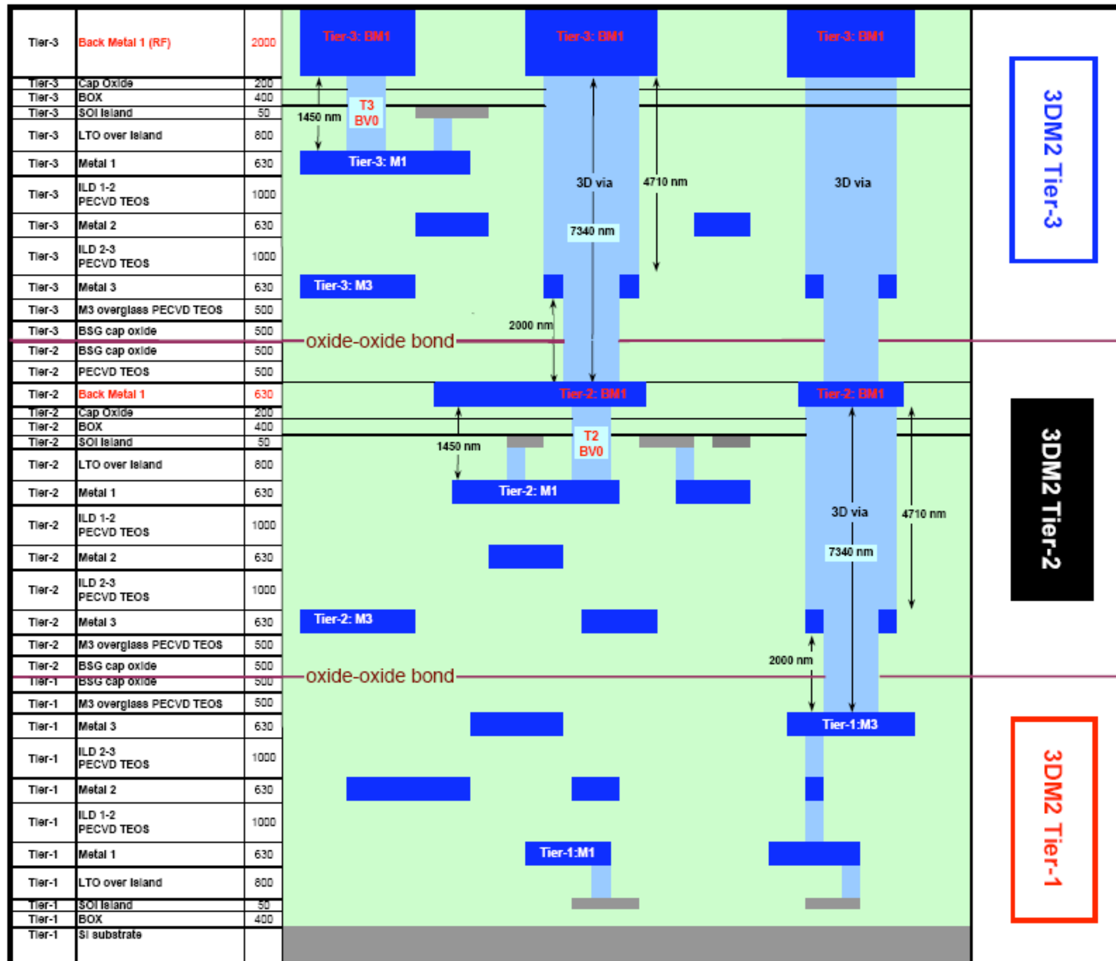
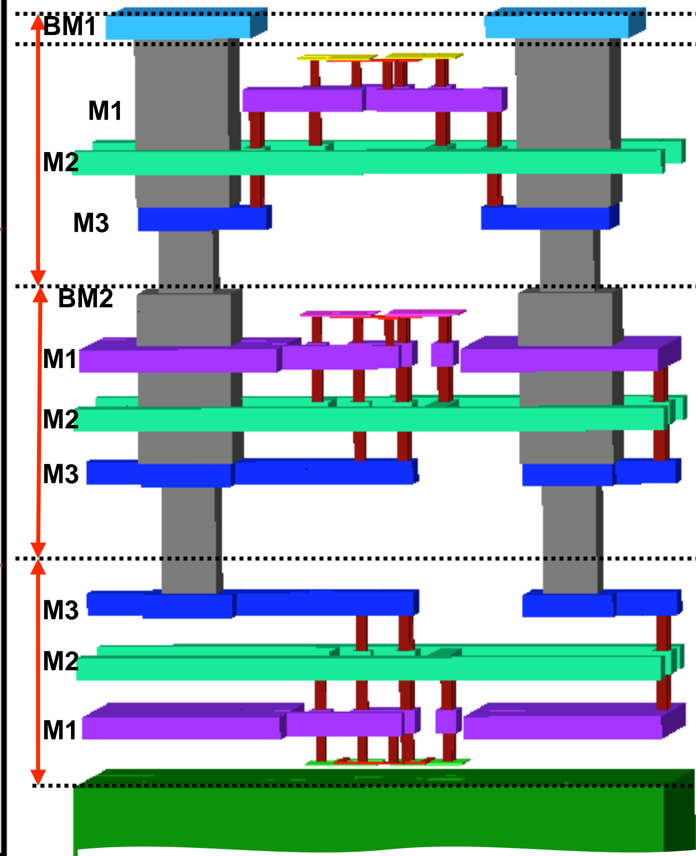
MITLL 3DM2 flow:

Process used for the design in 2006 (submission: Oct.2006 delivery Nov.2007 ☹)

MITLL 3DM2 (SoI) process (2006):



Full 3D Model with active elements in all layers (tiers)



from CFDRC

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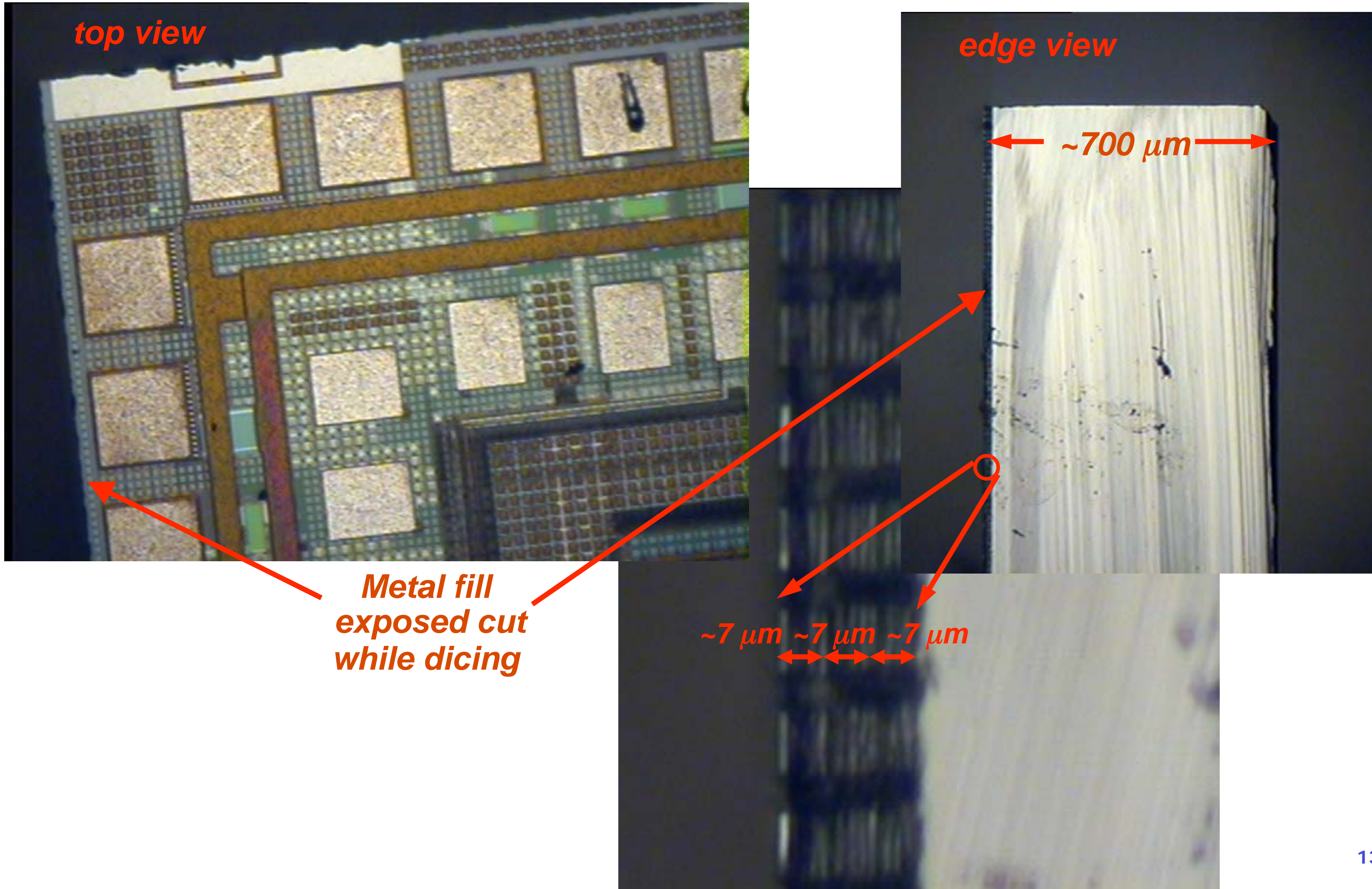
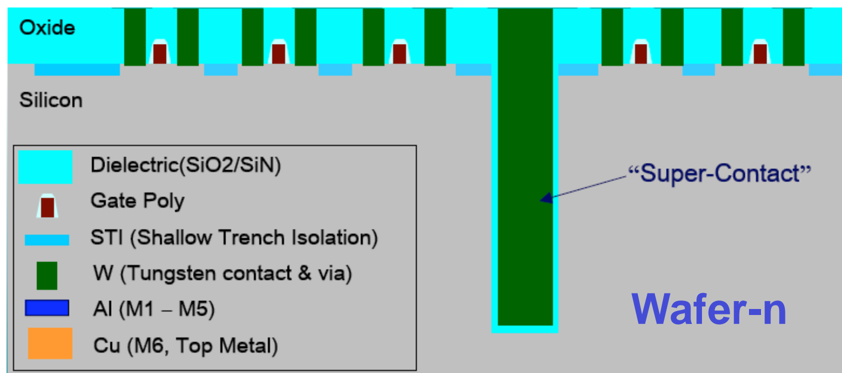
VIP: pixel 3D stack view



Tezzaron process flow:

- multi-tier tier chip; Tezzaron includes 130-nm bulk CMOS (fabrication Chartered Sem.),
- choice between 3 technology flavors including different VT transistors (usually nominal and low or high VT) and off -transistor lekage current, up to 8 routing metal layers + 3 different logic levels I/O transistors

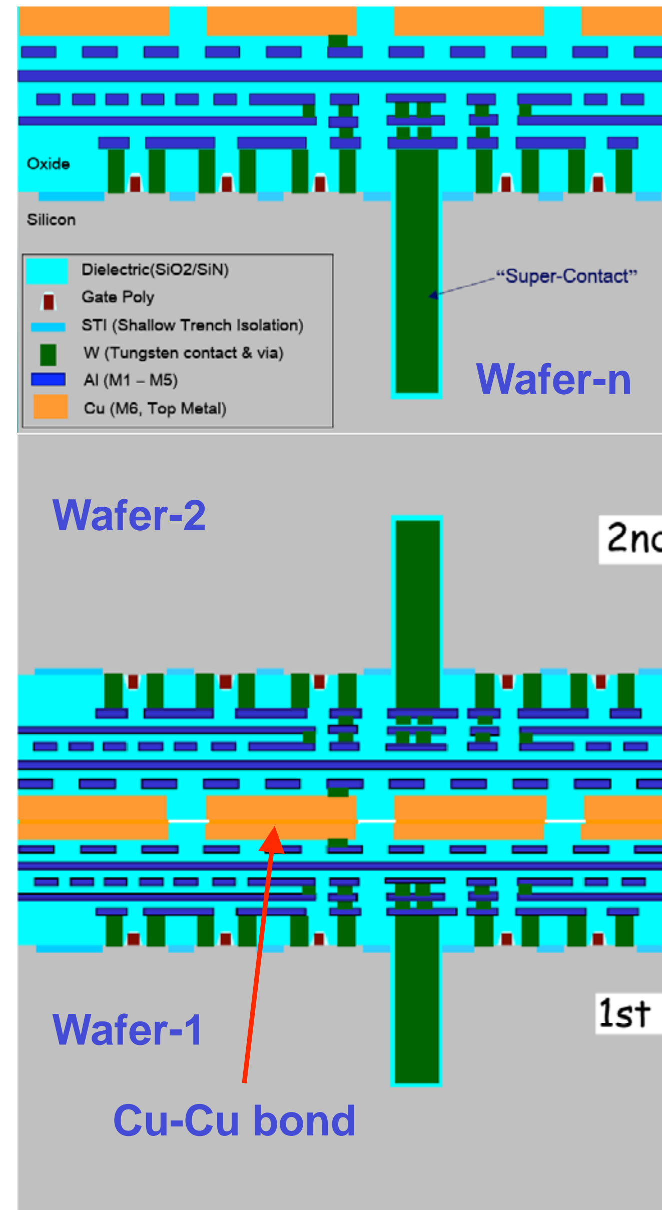
Step 1: Fabricate individual tiers; on all wafers to be stacked: complete transistor fabrication, form super via Fill super via at same time connections are made to transistors



All wafers are bulk

Step2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7 um)

Step 3: Bond wafer-2 to first wafer-1 Cu-Cu thermo-compression bond



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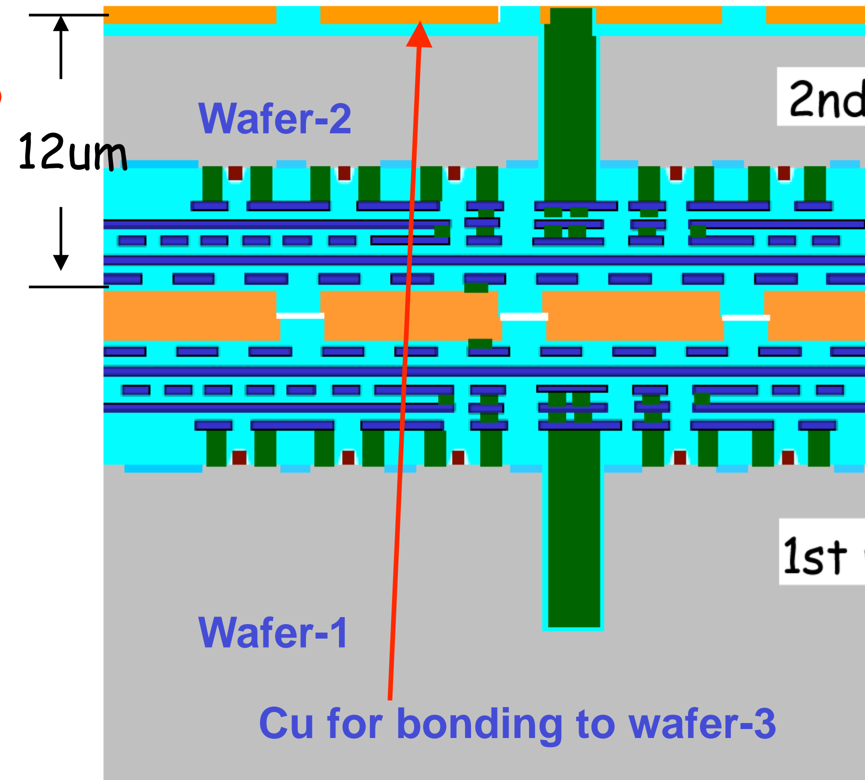
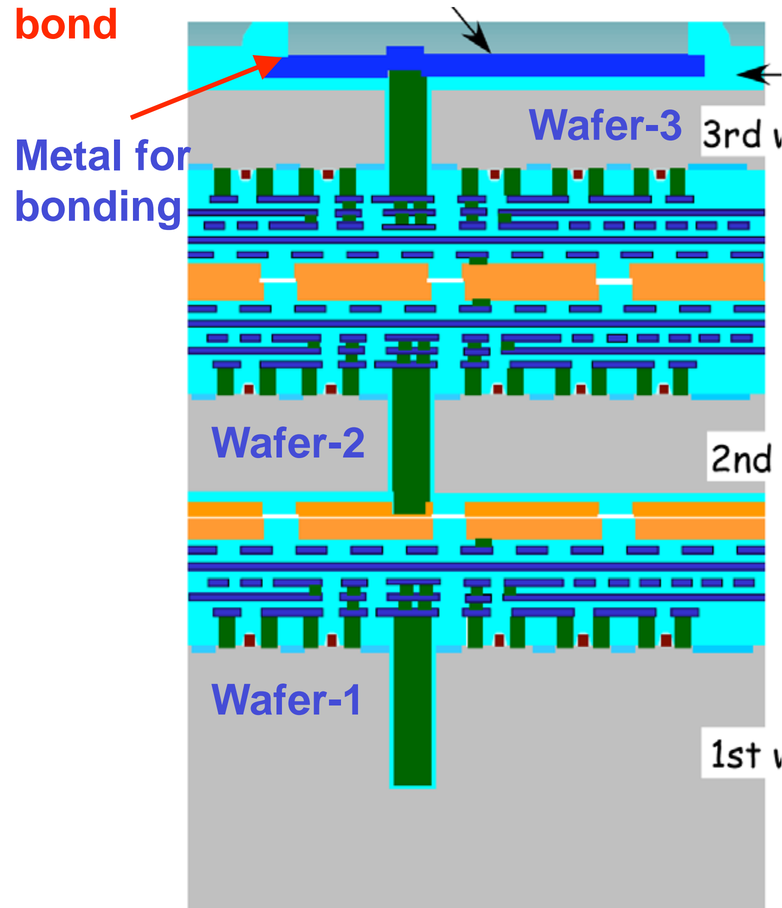
Tezzaron process flow:

Step 4: Thin the wafer-2 to about 12 um to expose super via. Add Cu to back of wafer-2 to bond wafer-2 to wafer-3
OR stop stacking now! add metallization on back of wafer-2 for bump bond or wire bond



Metal for bonding



Step 5: Stack wafer-3, thin wafer-3 (course and fine fine grind to 20 um and finish with CMP to expose W filled vias) Add final passivation and metal for bond pads

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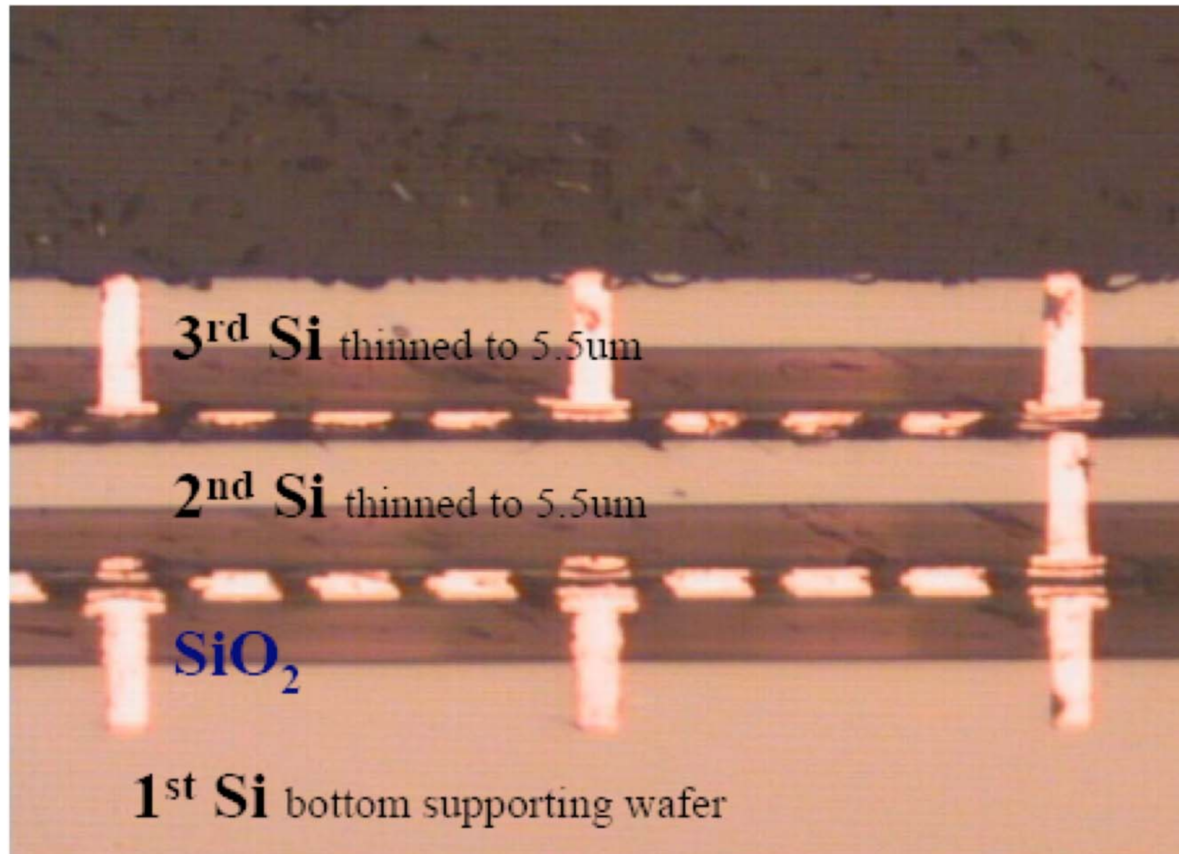
X-section of Tezzaron 3DIC stack:



Stack wafer bonding:

- Bonding performed at 40 PSI and about 375 degrees C.
- Bonding done with improved EVG chuck
  - 3 sigma alignment = 1 μm
- Missing bond connections = 0.1 PPM
- Temp cycling of bonds from -65 to + 150 C
  - 100 devices, 1500 cycles, 2 lots, no failures

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Pre and post boding transistor chcaracteristics:

	Threshold Voltage VT0 (V)						Saturation Current Idsat (uA) (Vd= Vg=1.2V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	0.395	0.485	0.479	-0.355	-0.399	-0.398	122.520	5152.000	9696.000	26.940	2061.800	5986.200
Post Ave	0.393	0.484	0.465	-0.357	-0.396	-0.404	121.500	5094.333	9840.333	26.897	1997.333	4473.000

	Breakdown Voltage BVDSS (V) (Ids=2uA)						Leakage Current Ioff (pA) (V=1.4V)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	3.380	3.220	3.220	4.100	4.000	2.780	151.820	638.900	3655.000	136.460	1285.120	282050.000
Post Ave	3.377	3.230	3.217	4.147	3.970	3.113	140.433	433.667	3237.667	211.333	910.333	121680.000

	Subthreshold Slope SUBSLP (mV/dec)						Gate Leakage Current GLEAK (nA)					
	NMOS W/L			PMOS W/L			NMOS W/L			PMOS W/L		
	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13	20/20	20/0.3	20/0.13
Pre Ave	75.840	76.820	79.380	-73.040	-76.960	-89.460	1.200	1.172	1.190	0.909	0.883	0.886
Post Ave	74.367	76.100	78.567	-74.733	-76.833	-88.600	1.250	1.287	1.300	1.018	1.011	0.767

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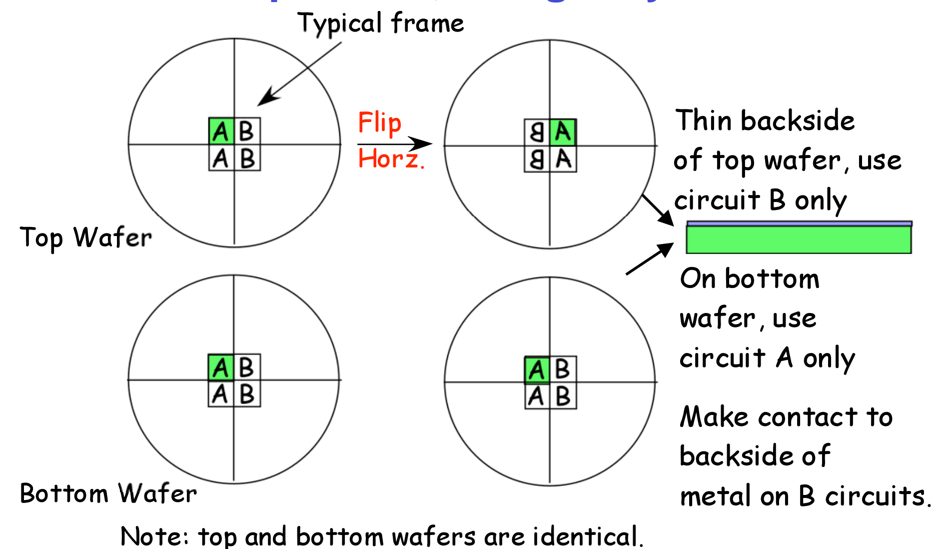
Limited information about Chartered process and fabrication plan:

- deep N-wells, MiM capacitors, single poly up to 8 levels of routing metals, variety of transistors (VT optimized) nominal, low power, high performance, low voltage, 8" wafers, reticle 24×32 mm^2;
- Tezzaron vias are very small: Φ_{via}=1.2 μm, $\Phi_{landing_pad}$=1.7 μm, d_{min}=2.5 μm

- Fermilab will be submitting a 3D multi project run using Tezzaron.
- Cost-efficient option is considered with only 2 layers of electronics fabricated in the Chartered 0.13 um process, using only one set of masks



Face to Face Bonding

Planned submission Dec.2008/Jan.2009 (delivery 12 weeks after ☺)

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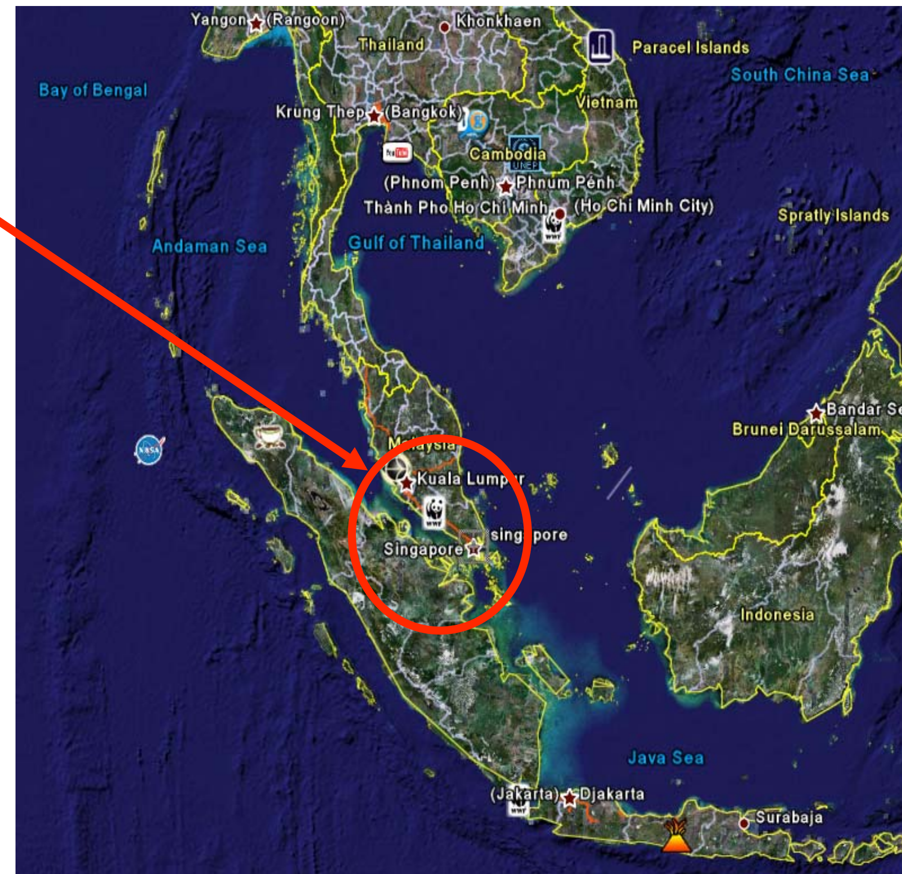
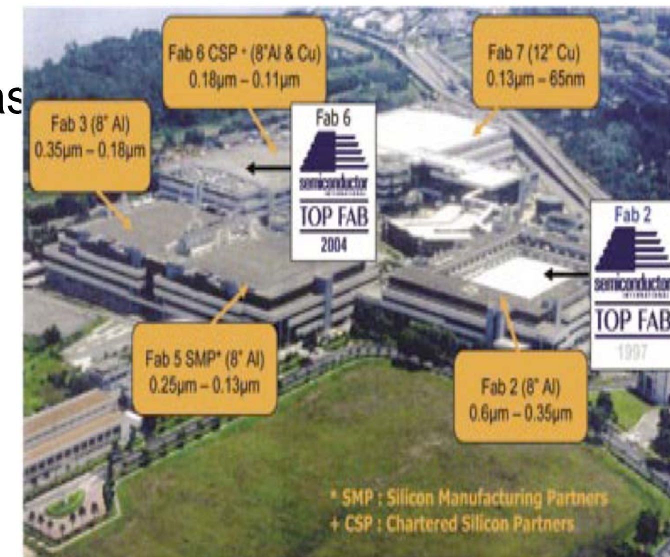
Tezzaron background:

- Founded in 2000, located in Naperville, Illinois
- Has fabricated a number of 3D chips for commercial customers
- Tezzaron uses the "Via First" process
- Wafers with "vias first" are made at Chartered Semiconductor in Singapore.
- Wafers are bonded in Singapore by Tezzaron.
  - Facility can handle up to 1000 wafers/month
- Bonded wafers are finished by Tezzaron
  - Bond pads
  - Bump bond pads
- Potential Advantages
  - Lower cost
  - Faster turn around
  - One stop shopping!!
- Process is available to customers from all countries



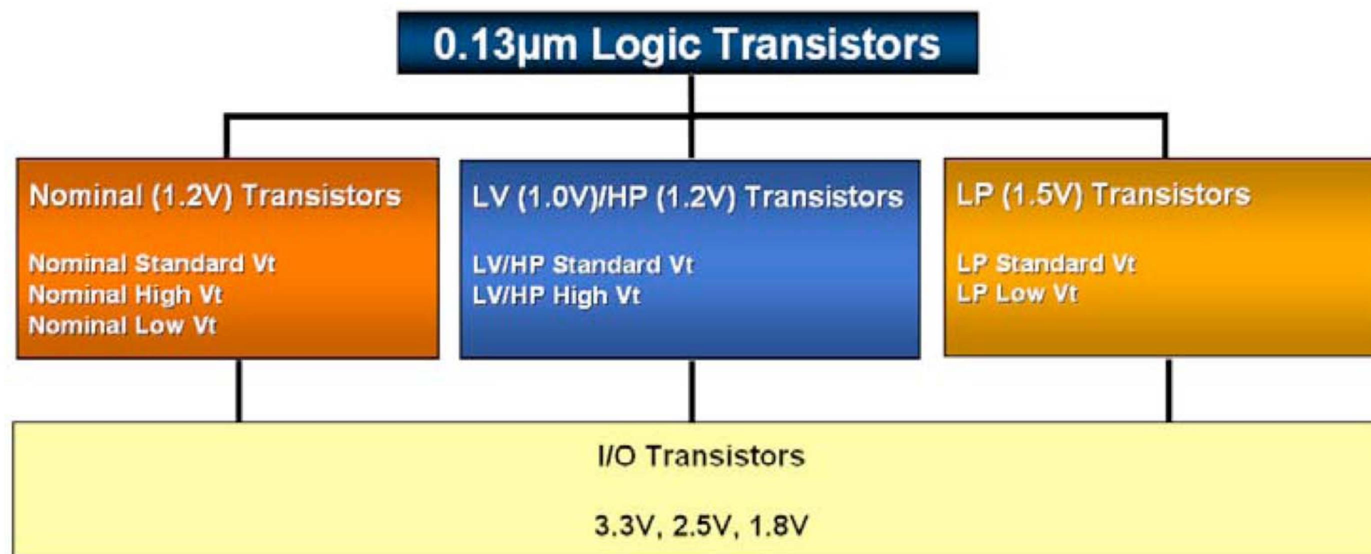
Chartered Sem.:

- One of the world's top dedicated semiconductor foundries, located in Singapore, offering an extensive line of CMOS and SOI processes from 0.5 um down to 45 nm.
- Offers Common Chartered-IBM platform for processes at 90 nm and below.
- Chartered 0.13 um mixed signal CMOS process was chosen by Tezzaron for 3D integration
  - Chartered has made nearly 1,000,000 eight inch wafers in the 0.13um process
- Extension to 300mm wafers and 45nm TSVs underway
- Chartered 0.13 um process has different layer arrangement and transistor thresholds than IBM process.
- Commercial tool support for Chartered Semiconductor
  - DRC – Calibre, Hercules, Diva, Assura
  - LVS - Calibre, Hercules, Diva, Assura
  - Simulation – HSPICE. Spectre, ELDO, ADS
  - Libraries – Synopys, ARM, Virage Logic



Chartered Campus

Chartered Sem. Process flavors:



Choose one of three processes and one of three I/O transistors types

A few words about cirucits fabricated in MITLL

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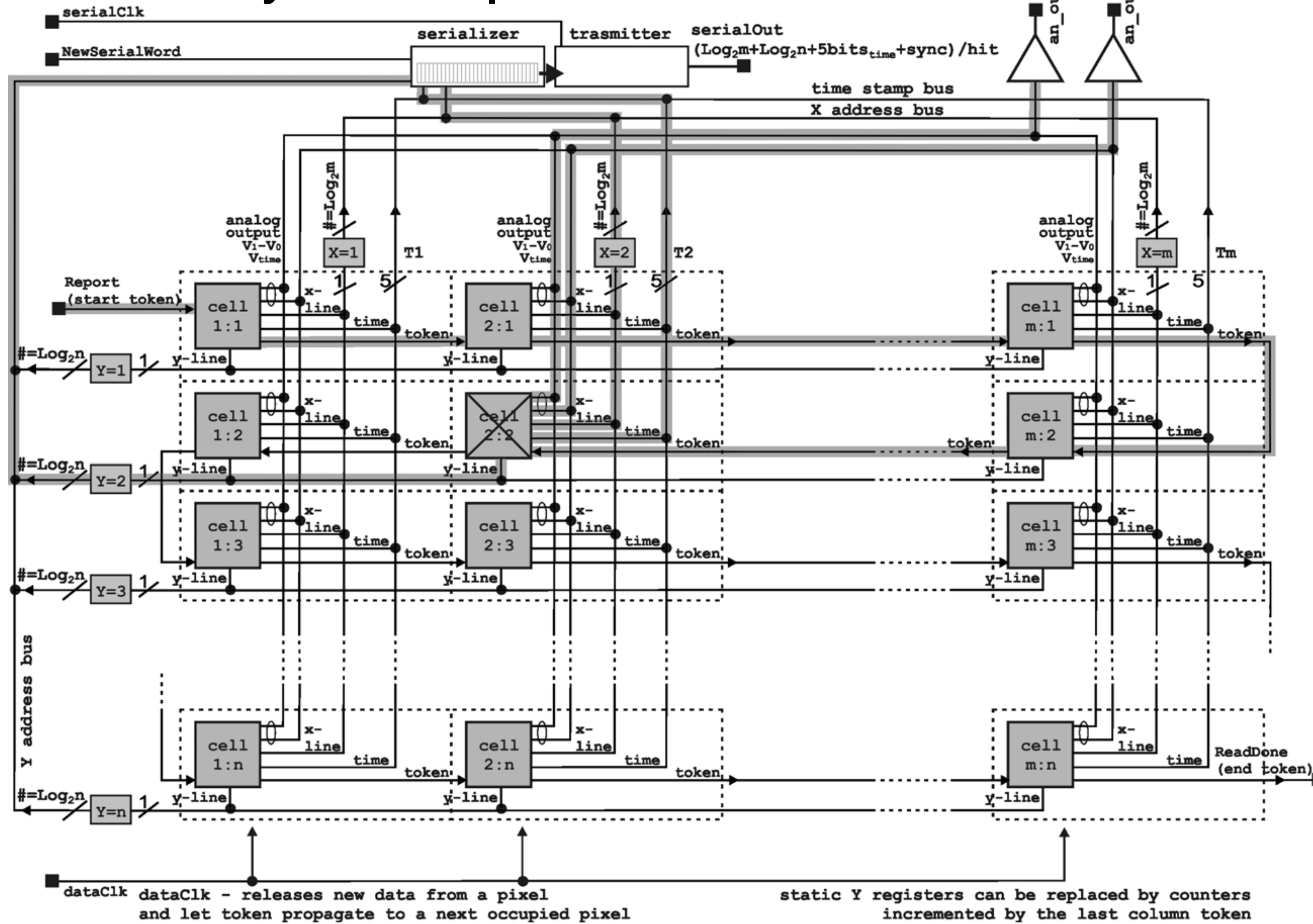
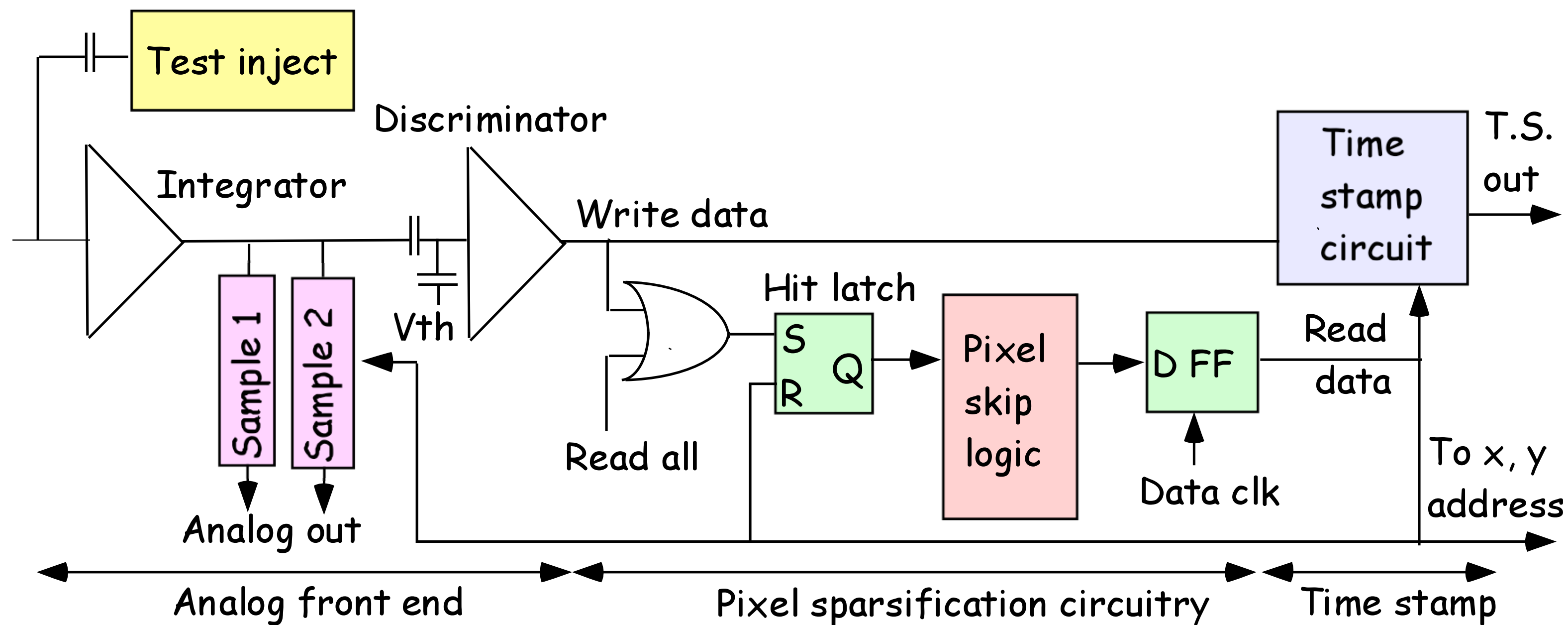
Pixel array with sparsification oriented on ILC:



Very simplified pixel block diagram for ILC:



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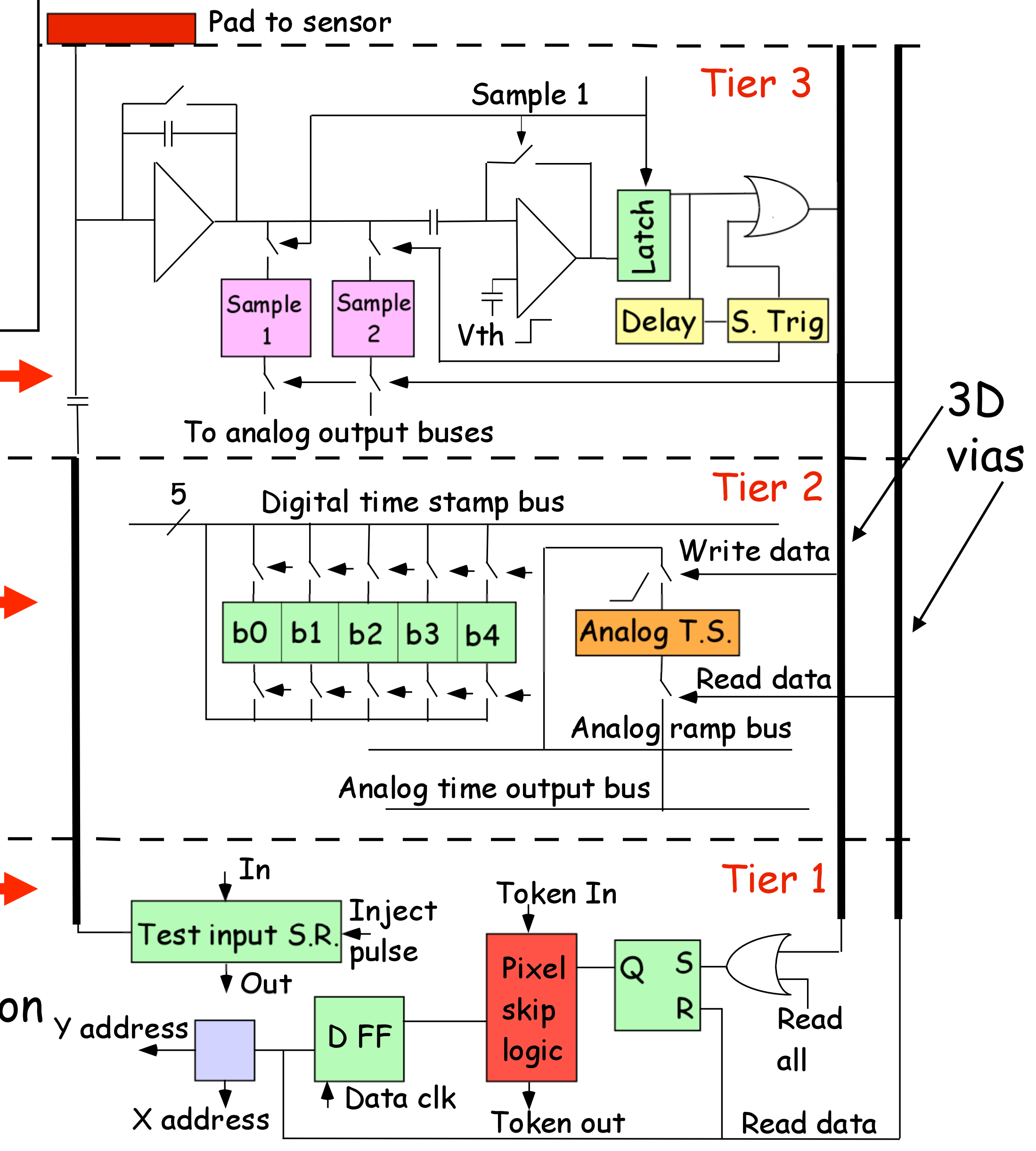
Distribution of fucntionalities between tiers for the ILC design::

38 transistors Tier 3 analog

72 transistors Tier 2 Time Stamp

65 transistors Tier 1 Data sparsification



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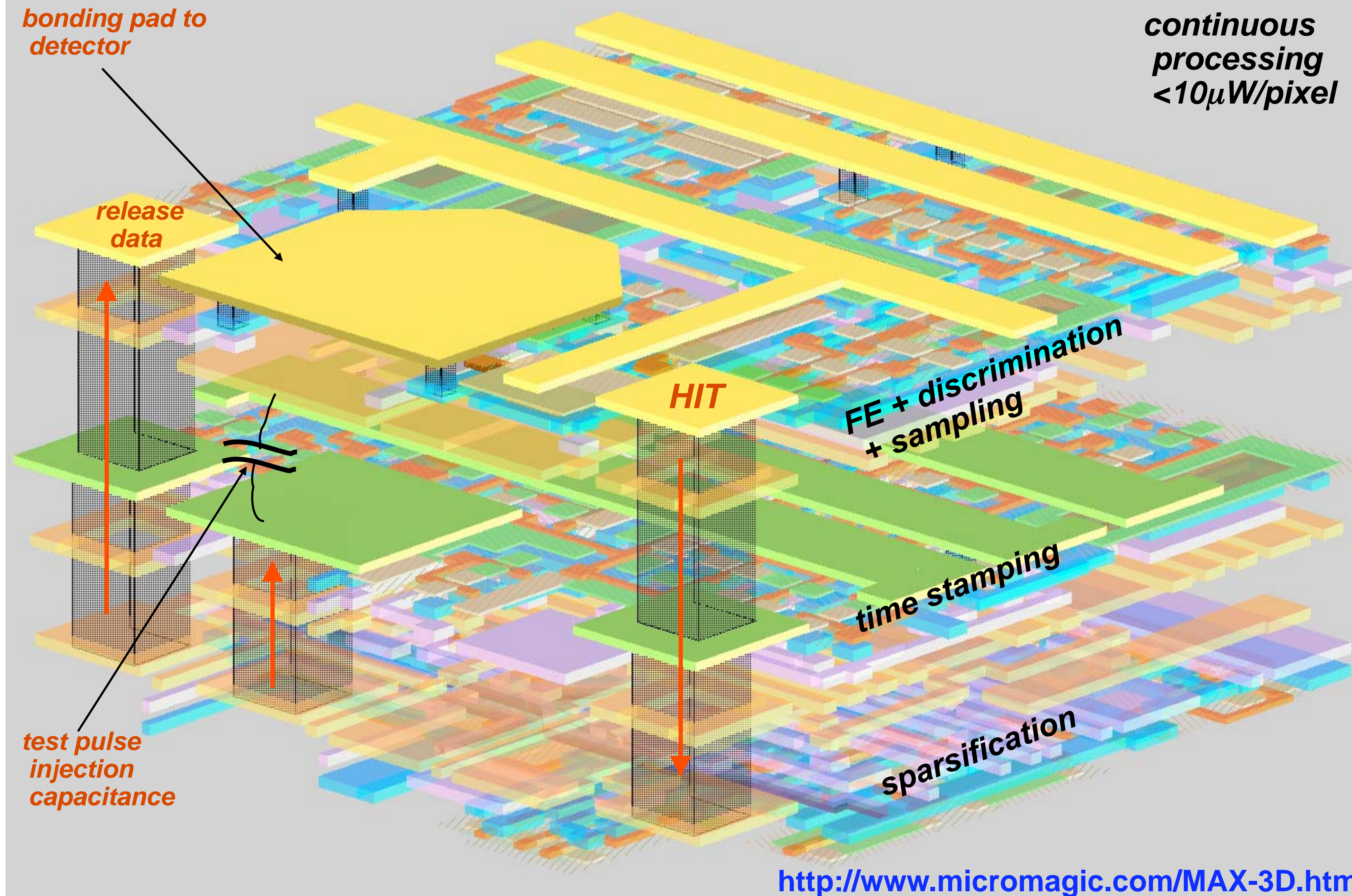
VIP: pixel 3D stack view



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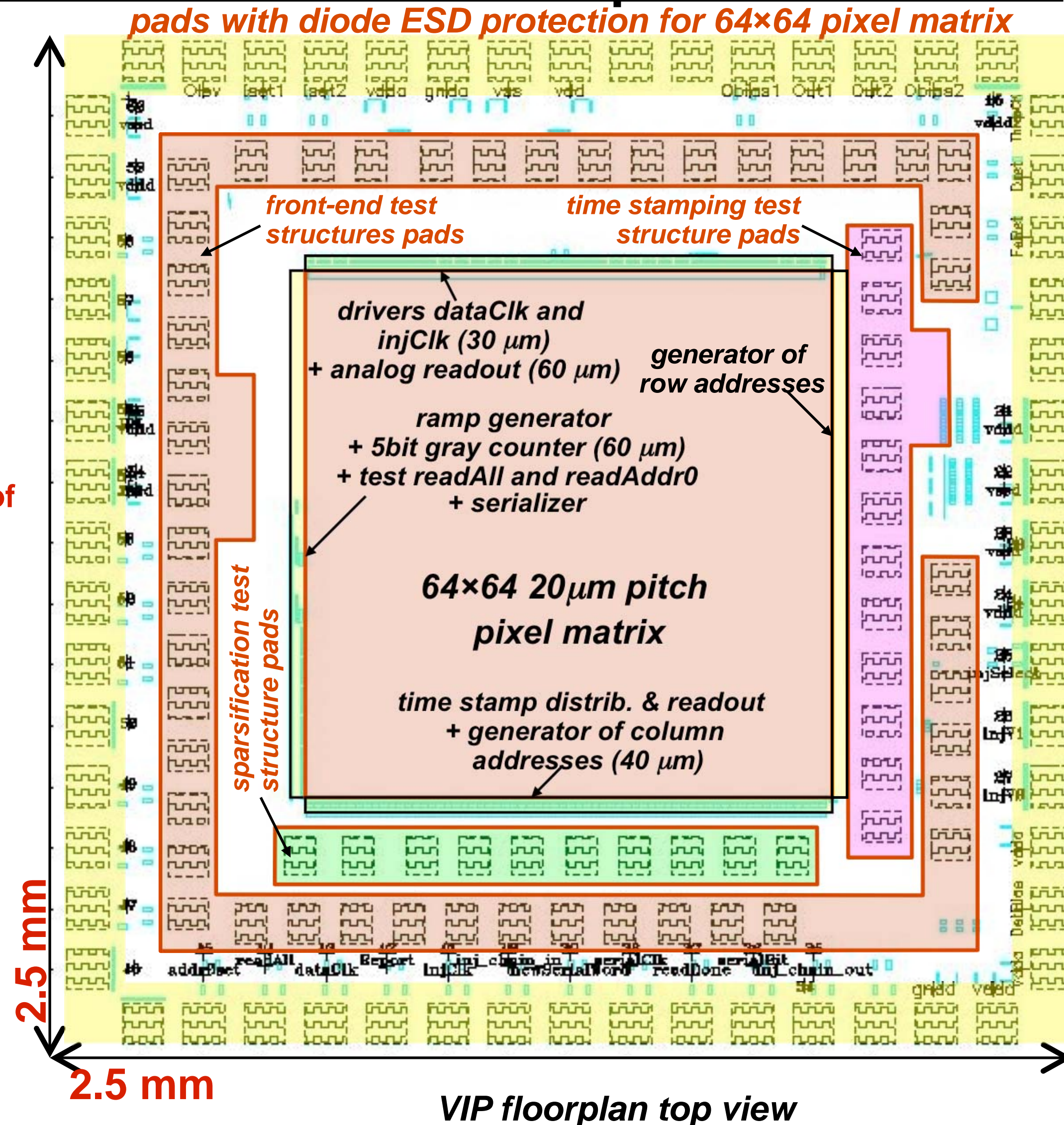
Floorplan of the VIP chip:

design contains:

- a fully functional matrix of 64×64 pixels, using peripheral pads, all pads are ESD protected with anti-parallel diodes
- single pixel test structures, placed on corresponding layers using internal ring of pads, reduced, or NO ESD protection.

•VIP stands for Vertically Integrated Pixel

Yield problems faced in tests – looks like process problems – investigations underway



VIP floorplan top view

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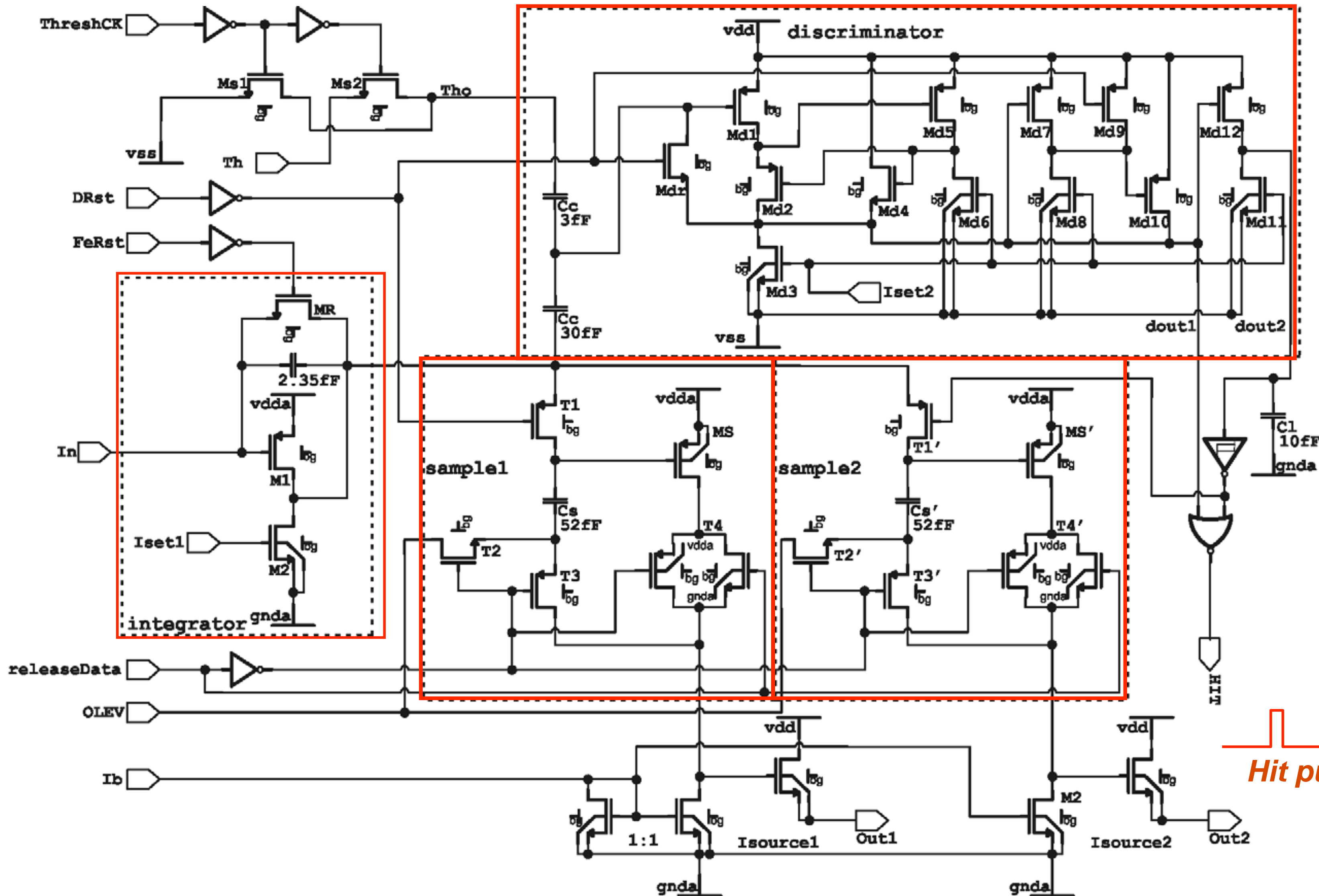
Details of the front-end (tier3):



Hit pulse

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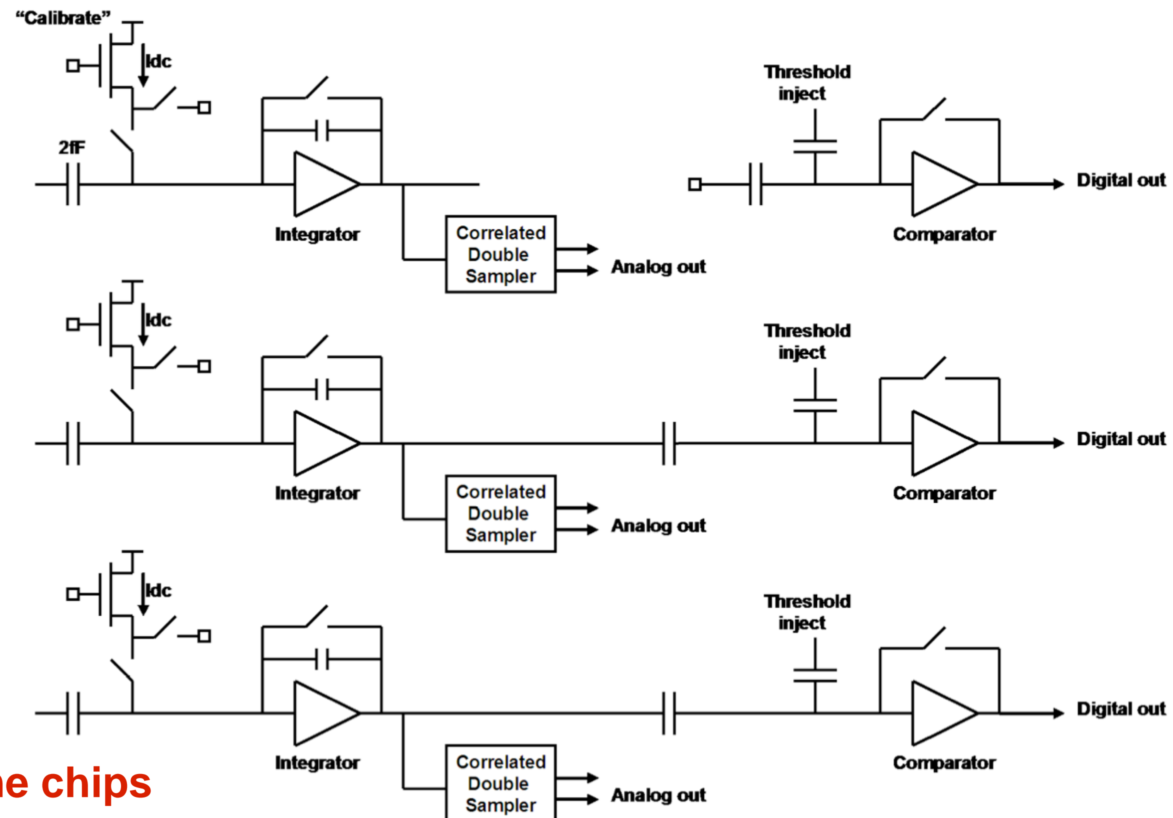
Details of the front-end (tier3):

- tested tests structured laid out outside the 64×64 pixel matrix,
- access to integrator output, output of CD sampler, discriminator,

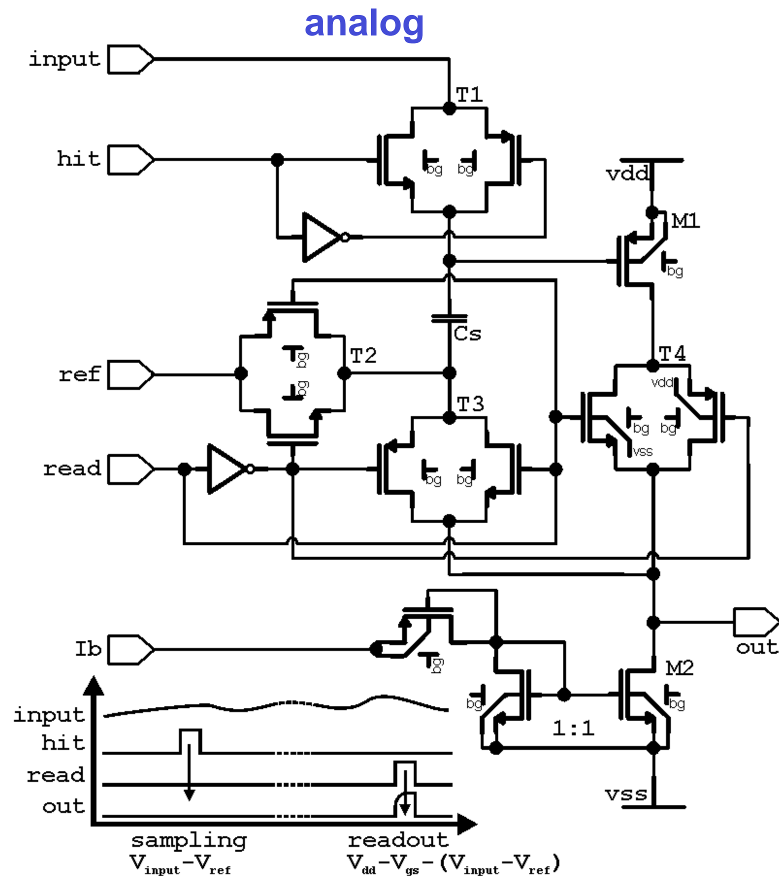


- Integrators work on some chips
- Discriminators work on other chips
- Analog circuits are a little faster than simulations.
- Noise performance appears close to simulations on the few circuits that work

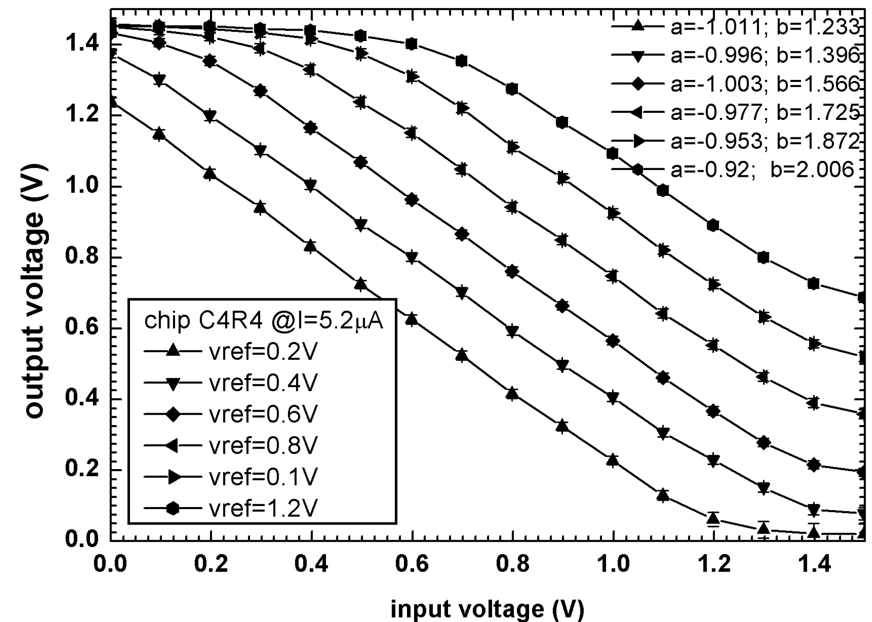
Details of the time stamping (tier2):

• each pixel contains: analog (sample and hold and readout buffer) and digital (reset latch and readout buffer),

analog



measurements on C4R4



• sample and hold circuit with follower readout,
• 'hit' signal samples ramp value,
• new voltage follower type circuit allowing sampling voltage signal almost rail-rail!

nice linear characteristics, allowing sampling almost rail-to-rail voltages (with adjusted reference level); although very high kTC noise (10-30mV @ C=50fF) - measured as variation of output voltage resulting from many sampling -readout cycles.

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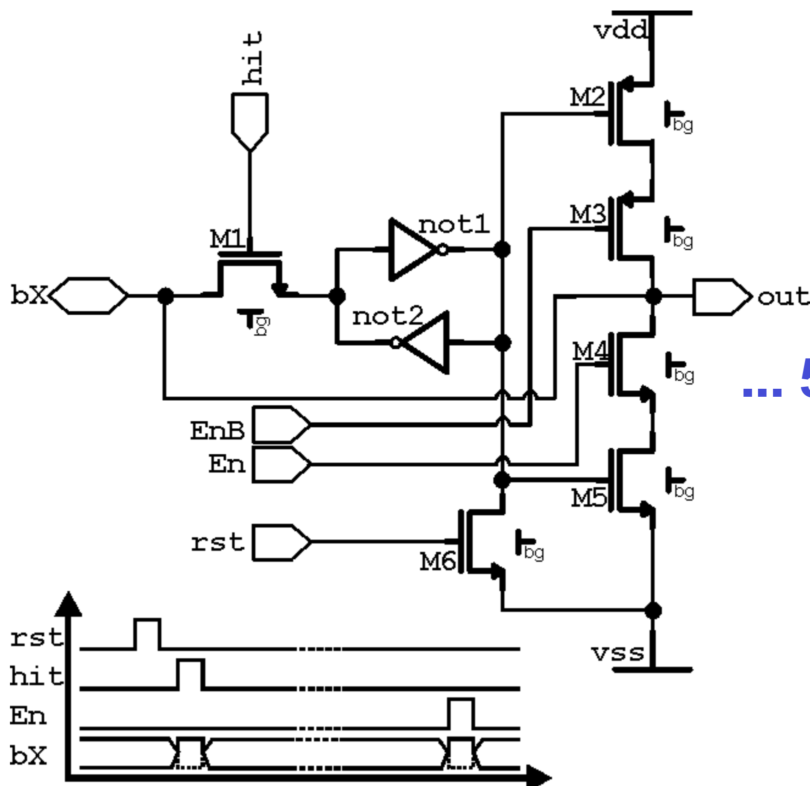
Details of the time stamping (tier2):

digital

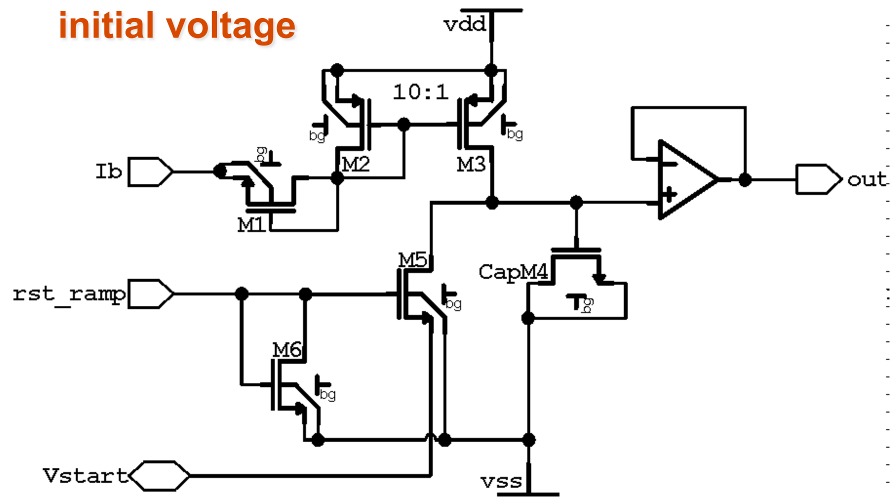


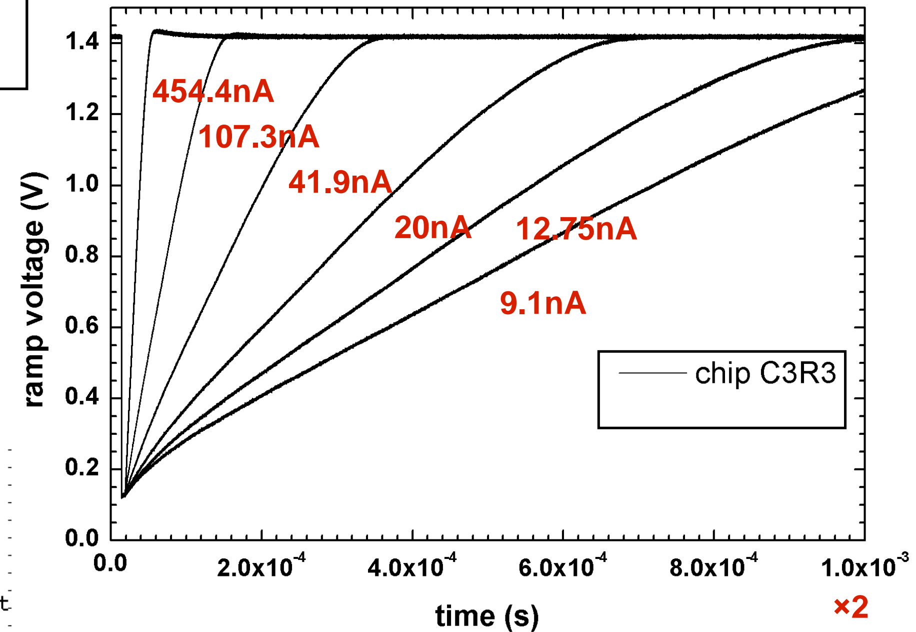
... 5 ×

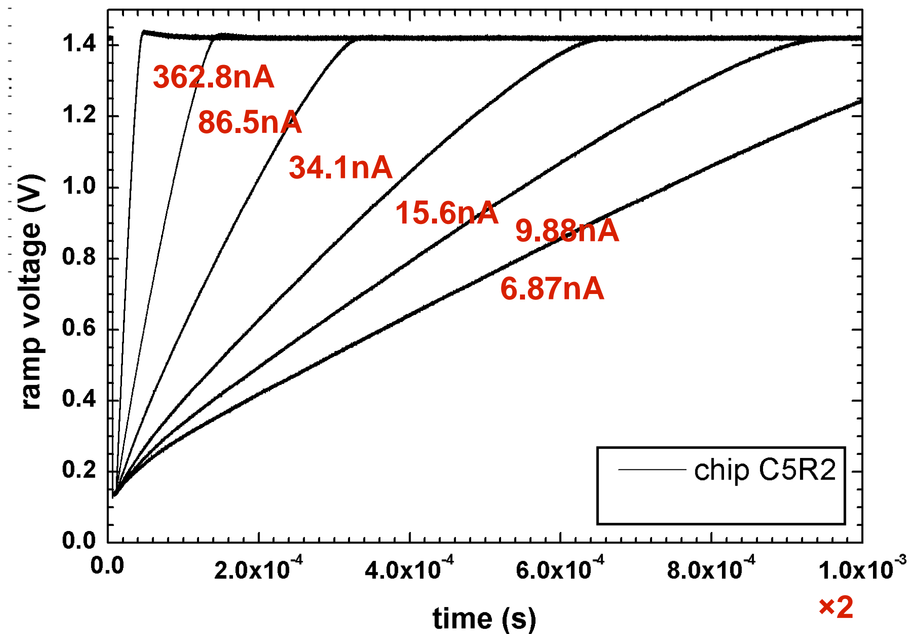
- simply resettable SRAM-type cell with tri -statable buffer
- input from 5 bit Gray code counter placed at the periphery, active during acquisition
- output on the same lines during reporting

time stamping (tier2):

- ramp generation circuit: current repeated by current mirror and integrated on a capacitor (2.5pF designed); result of integration is distributed to the matrix after buffering with a follower (OpAmp); capacitor is reset with a switch to the initial voltage



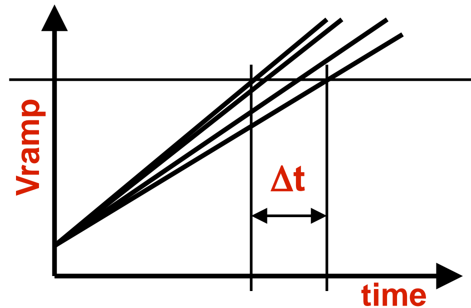




- values of currents on the primary side of the current mirror,
- problems with big spread of current mirroring ratio,
- noticed rather high leakage currents of ESD diodes,

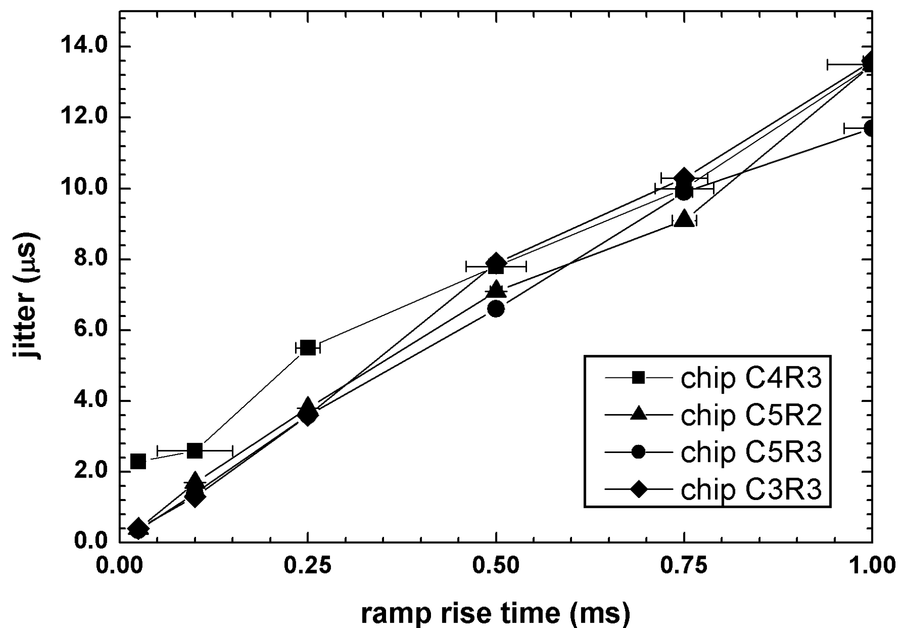
time stamping (tier2):

- Noise of the ramp measured as variation of time after which ramp reaches the desired voltage level,



- observed:
  after each reset the slope is slightly different (it is not kTC),

- Although the ILC physicist may be perfectly happy with ~10 μs time stamping precision... the electronics enginners cannot accept it!



Vstart=0.2V

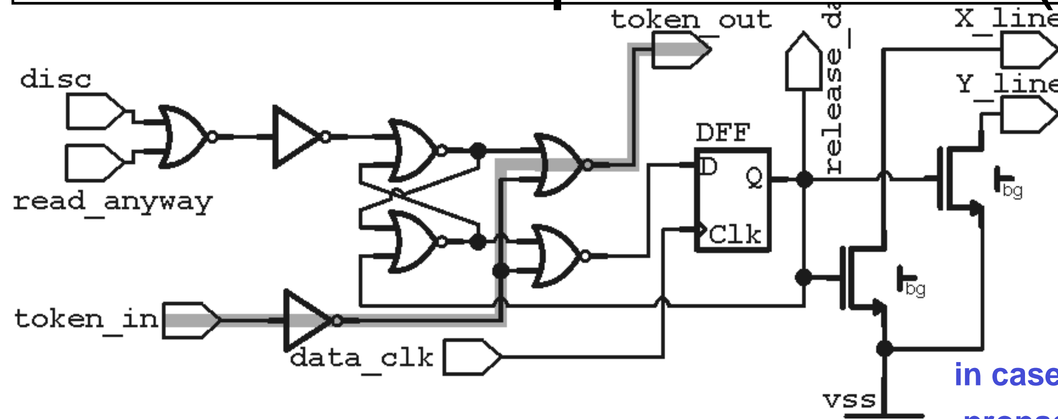
- why this jitter is so high?
  we don't know, it is a part of learning curve

- maybe this is the noise due to leaking ESD diodes – that are seen as 20 MΩ parallel resistors

- maybe this is something related to transisors in SoI process – they are much different from bulk transistors we are commonly familiar (kink effect, hysteresis,interface effect)

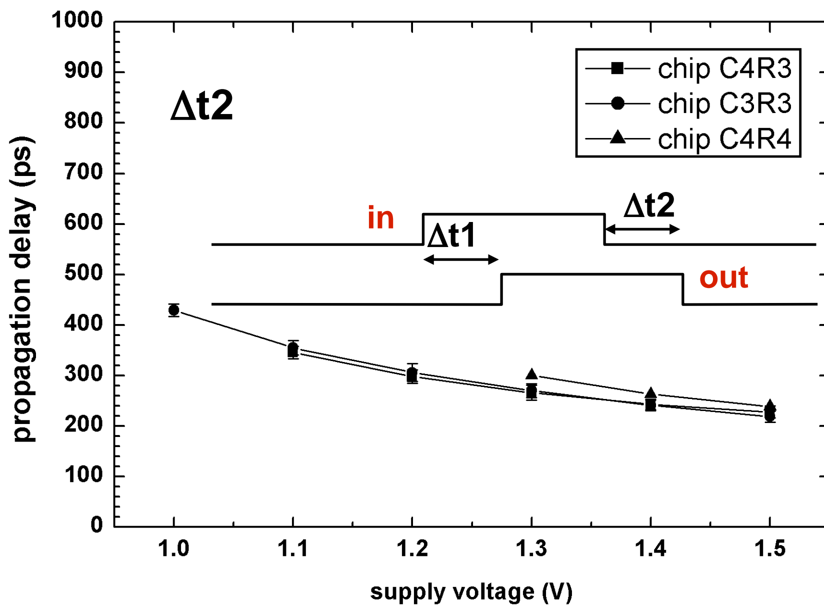
- we're interacting with MITLL to work out plausible hypothesis – any experience shared with us is welcome

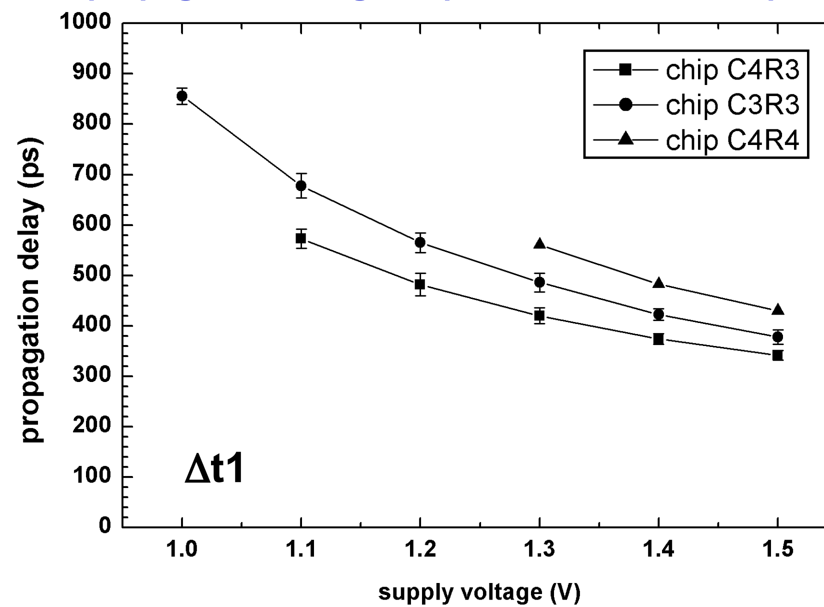
sparsification (tier1):



token propagation circuitry is part of sparsification circuitry; if pixel has data to send out high level at the token_in is not transmitted to token_out until the readout of the pixel address, time stamp and signal amplitude is not accomplished.

in case of lack of any hits recorded high level propagates through all pixels without interruption





propagation of falling edge:
NMOS transistors work; faster and less spread between chips

propagation of raising edge:
PMOS transistors work; slower and more spread between chips

Tests summary

- Tests are underway, they are slow due to face serious yield problems
  - Digital Results
    - Serial readout for addresses generated with X- and Y lines from hit pixels partially working on 3 of 6 chips and only for $0.9<V_{DDD}<1.3$ V. Circuits do not work at nominal power supply voltage,
    - Serial Shift Register for charge injection works on 3 of 4 chips for $1.0 <V_{DDD}<1.2$V,
    - Feature needed for large arrays (read all cells in column 1) works as shown on the next slide (Option of Addr0Set allows set S-R register in all pixels in the first column to emulate hit state of pixel – this feature is implemented for Mpixel arrays to leave enough time for token to propagate, while reading known data).
  - Analog Results
    - Full data acquisition used to measure analog pedestals on sample V0 output,
    - Results shown below on the next slide for 64 pixels,
    - The full 64 x 64 array has subarrays with different transistor sizes in the front-end,
    - Tests are underway, development of data acquisition system needed for further testing.

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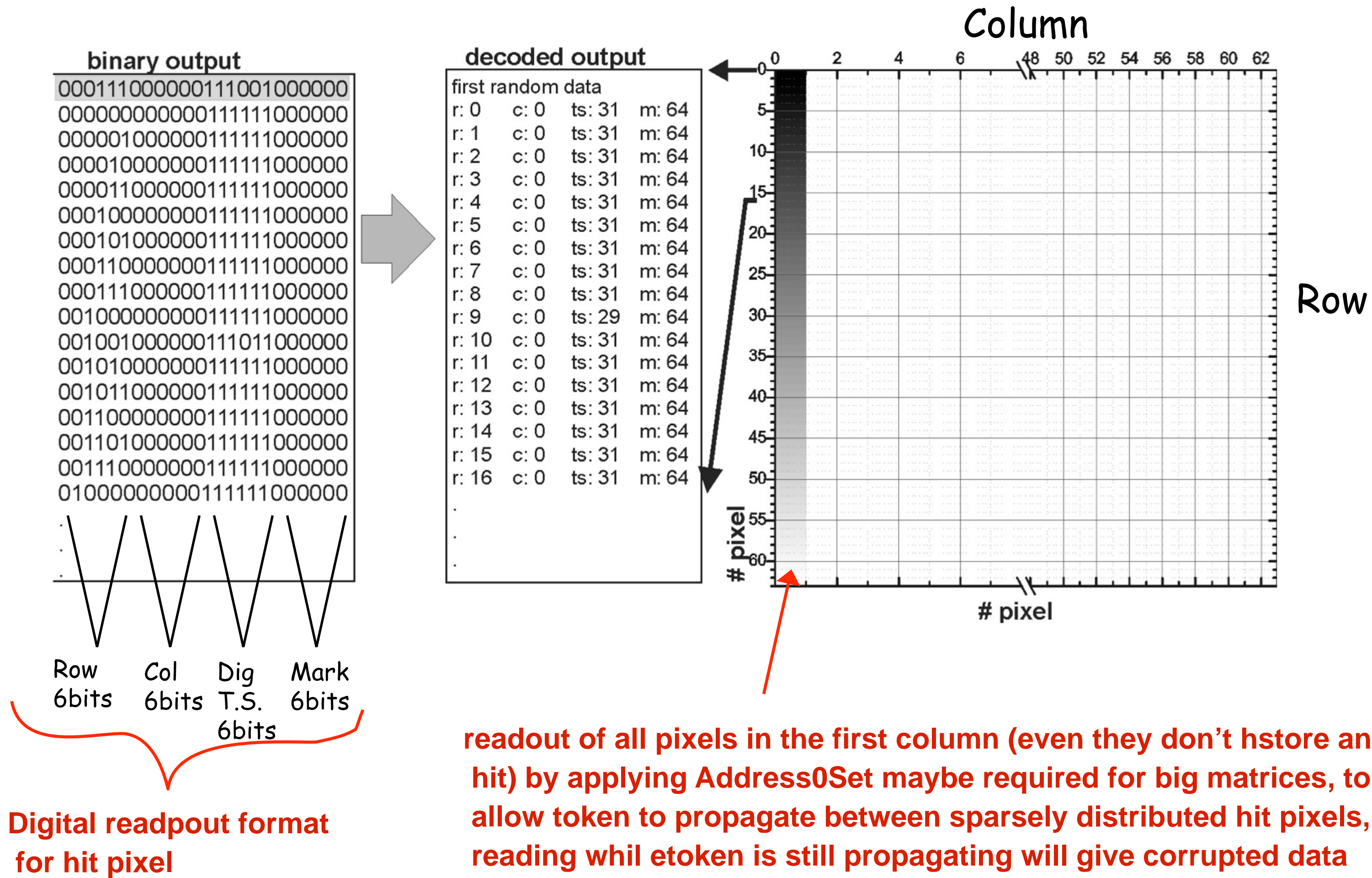
Tests summary

Digital Results



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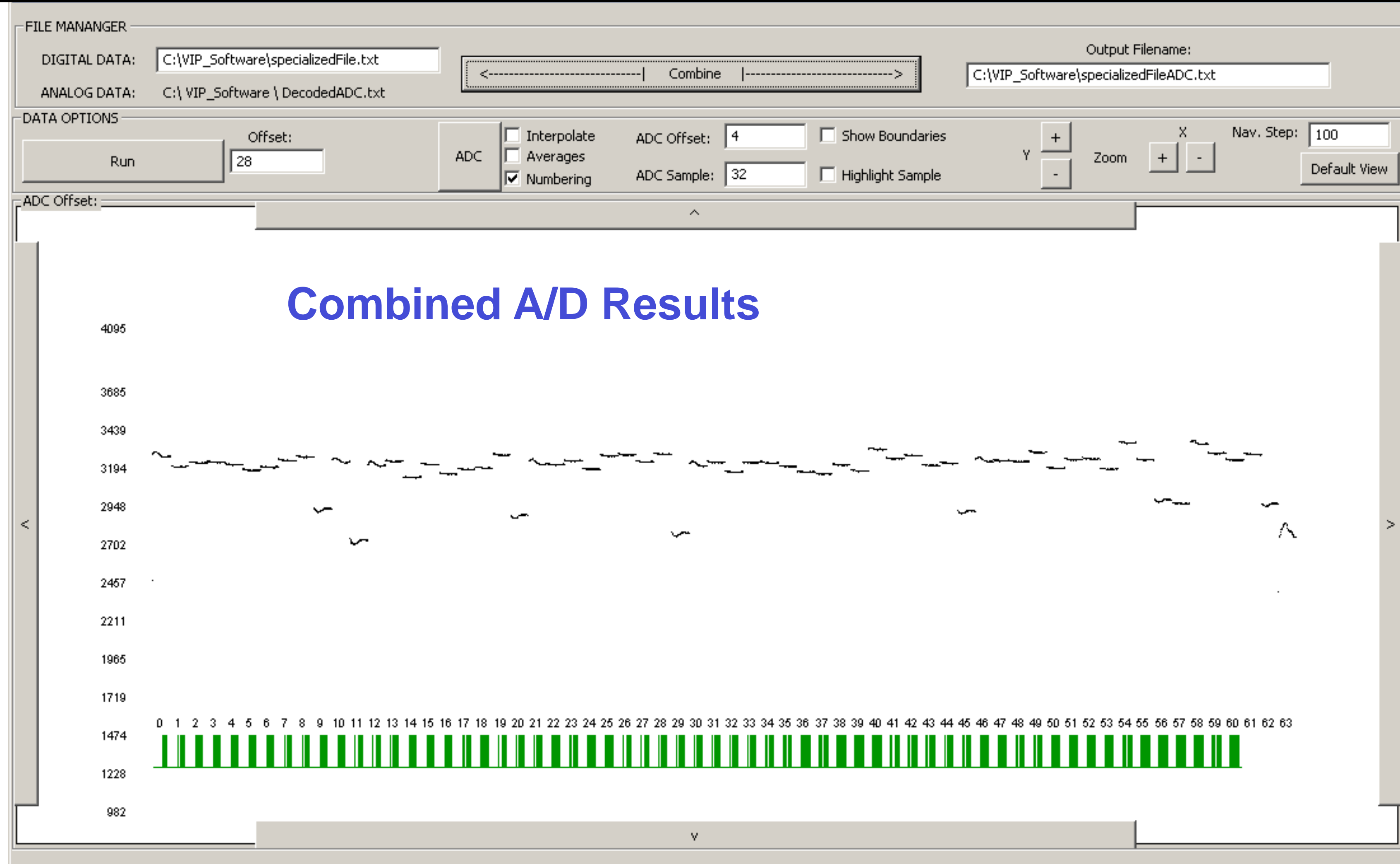
Tests summary



Screen snaphot from readout of column of addresses and corresponding analog data from sample V0 – using ReadAllCell testing feature on the chip (tests done @V_{DDD}=0.94V and V_{DDA}=1.5V)

Understanding VIP problems:

Interact with the vendor:

- Trapped charge between tiers 2 and 3 during fabrication caused NMOS transistor thresholds to shift from 500 mV to 200 mV,
- Attempts are being made by vendor to correct the problem after the fact with UV radiation,
- Backup lot being processed with different tier2-tier3 bonding conditions to remove threshold shift problem.
- ESD protection diodes are very leaky causing serious problems for circuits with analog inputs.
- Current mirrors used for biasing are not working properly - problem thought to be due to leakage path in the current mirror circuits.
- There are significant variation between chips resulting in low yields - reasons unknown at this time.
- Testing will continue with parts from a different wafer
- Discussions are ongoing with other users

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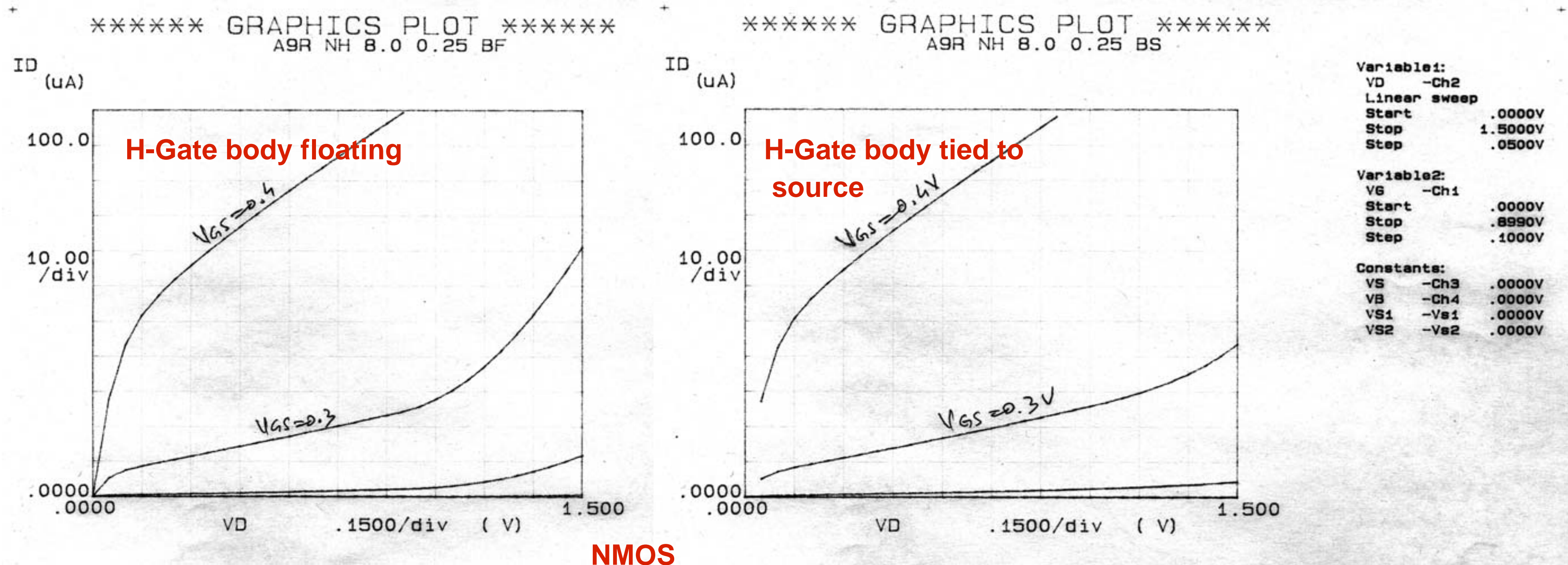
Understanding FD SoI Transistors

A few examples of transitor output characteristics for MITLL



NMOS

Having well characterized transistors, accurate models addressing different allowed configurations of transistors (BF, SBC, HGate) is crucial for successful design (not easy ofr analog design in SoI particularly in FDSoI)

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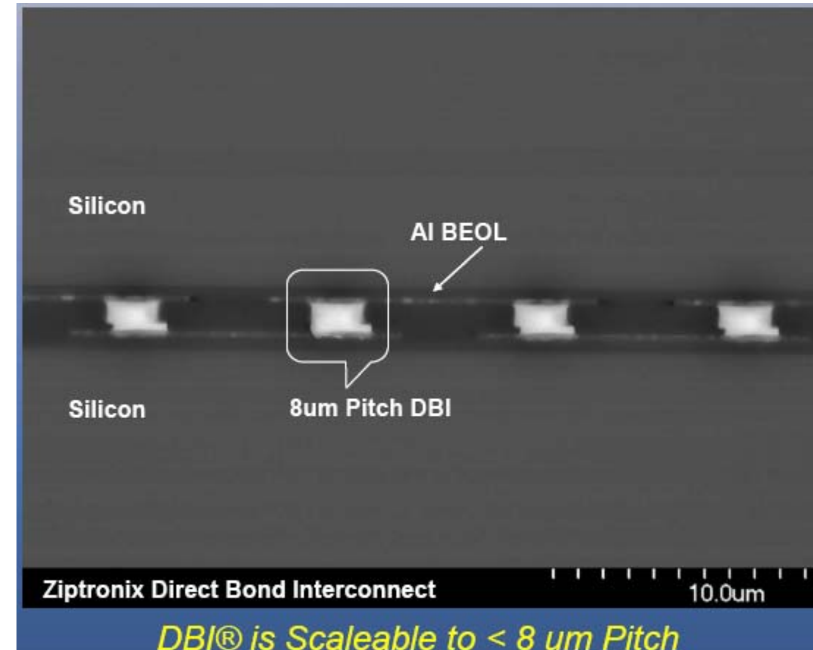
High density bonding options

- Some parts received from Tezzaron will be bonded to sensors.
- Fermilab sensors are being made at MIT LL.
- Some 3D bond processes introduce significant material between bonded layers.
  - Conventional solder bumps or CuSn can pose a problem for low mass fine pitch assemblies
- IC bonding to a detector will be done by Ziptronix using the Direct Bond Interconnect (DBI) process.6
  - Xo < 0.001%
- Tezzaron and Ziptronix have formed an alliance.
  - Good communication between companies for pad metallization for sensor bonding, etc. now exists.



- Ziptronix is located in North Carolina
- Fermilab has current project with Ziptronix to bond BTEV FPIX chips to 50 um thick sensors.
- Orders accepted from international customers

High density bonding options

- After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.

DBI™ Electrical Interconnections

CMOS Back End of Line

Bond Interface

CMOS Back End of Line

1) Place DBI Surfaces into Contact

Conventional Pick-&-Place
Room Temperature, Direct Oxide Bonding

CMOS Back End of Line

Bond Interface

CMOS Back End of Line

2) 300-350°C Bake (Batch)

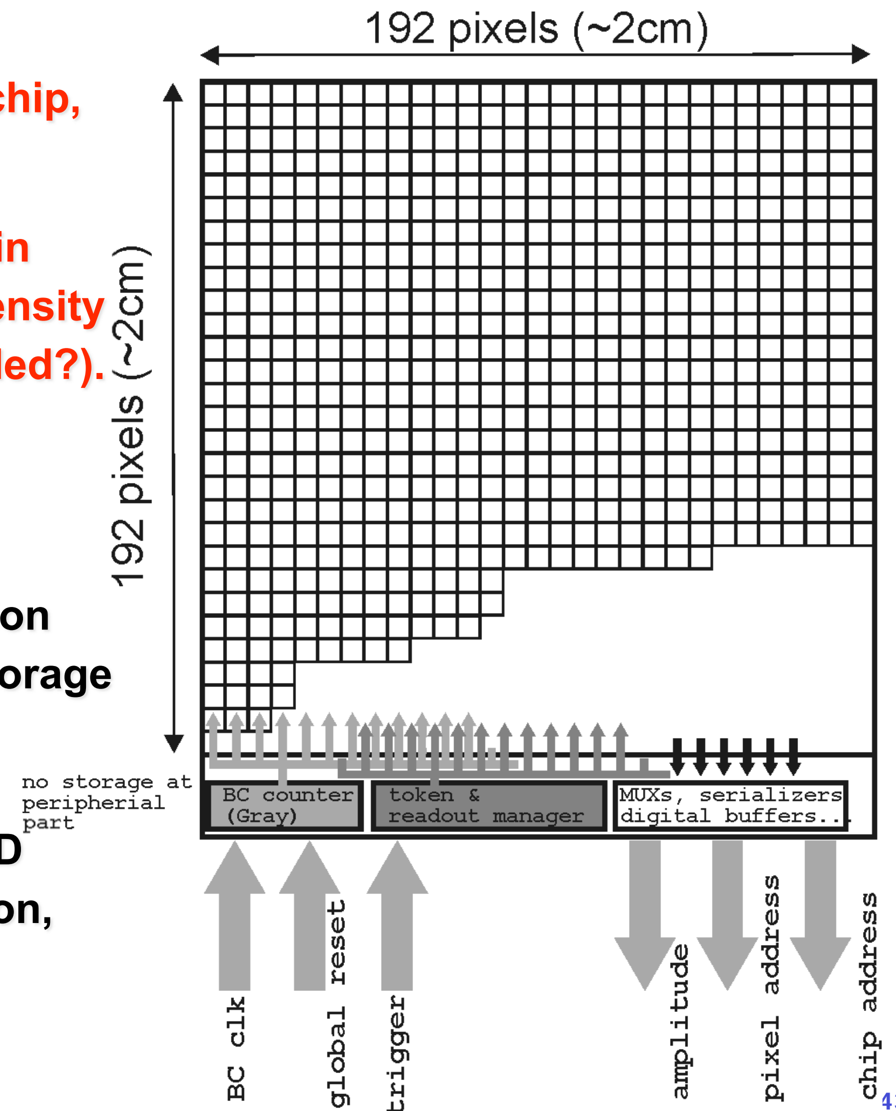
Metal CTE > Oxide CTE
Metal Compression
Oxide Tension (Requires High Bond Strength)

3) DBI Interconnection

Fermilab

R&D for pixel for LHC upgrade work

- FNAL is willing to contribute to the LHC upgade with a design of the pixel readout chip,
- Going from 1 layer in 0.25μm to 2 layers in 0.13 μm can increase circuit density × 7, density can by traded for smaller pixel size (if needed?).
- the key points are:
  - low power consumption (not more than current design),
  - high speed and data throughput, reduction of data loss (large digital storage – no storage at the periphery),
  - radiation hardness,
  - parallel processing in-situ (in pixel A-to-D conversion event triggered), sparsification,
  - reduction of peripheral circuitry,
  - can pixels have trigger capability?



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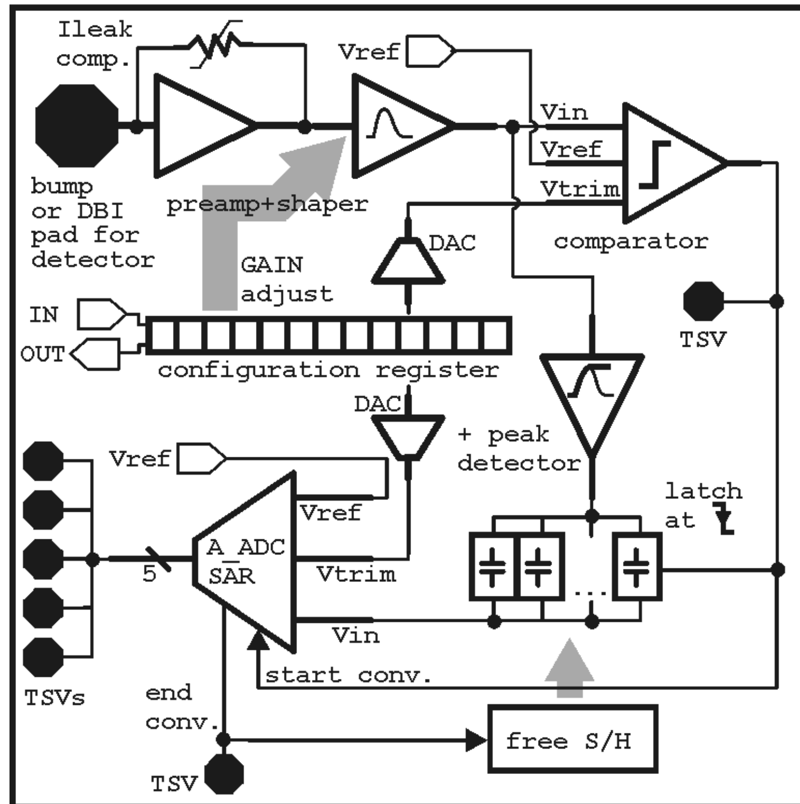
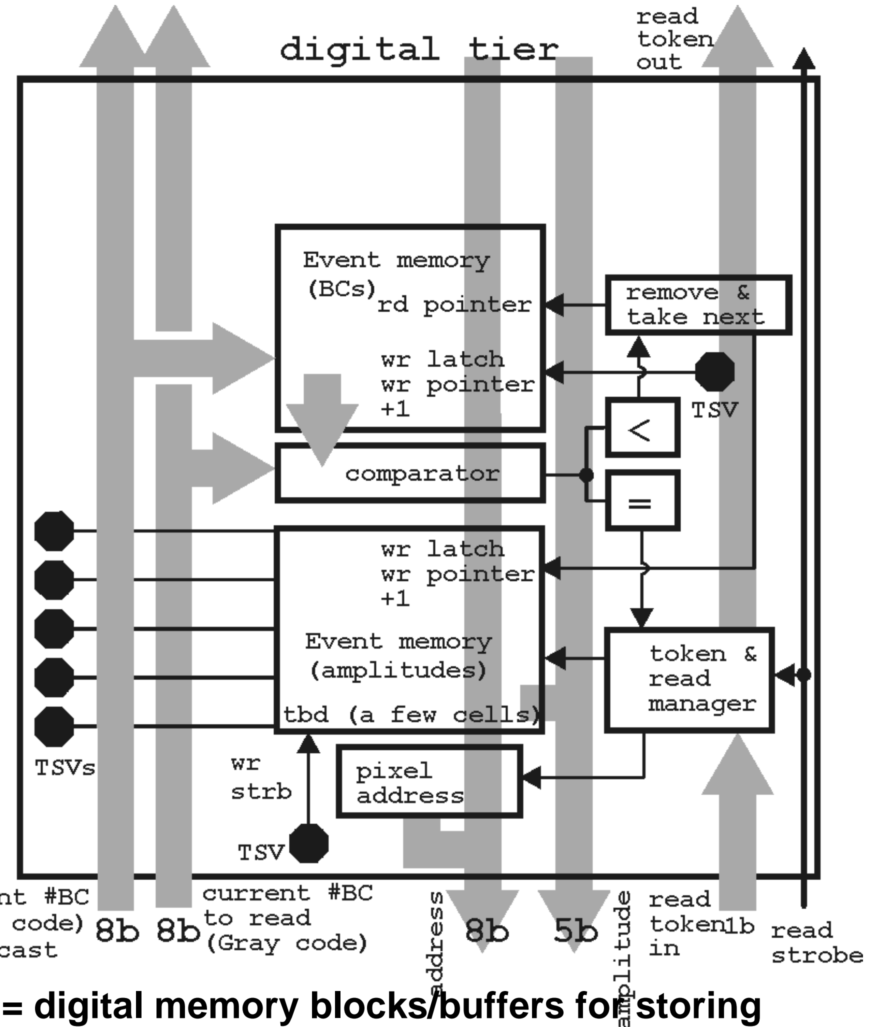
R&D for pixel for LHC upgarde work

Pixel concept





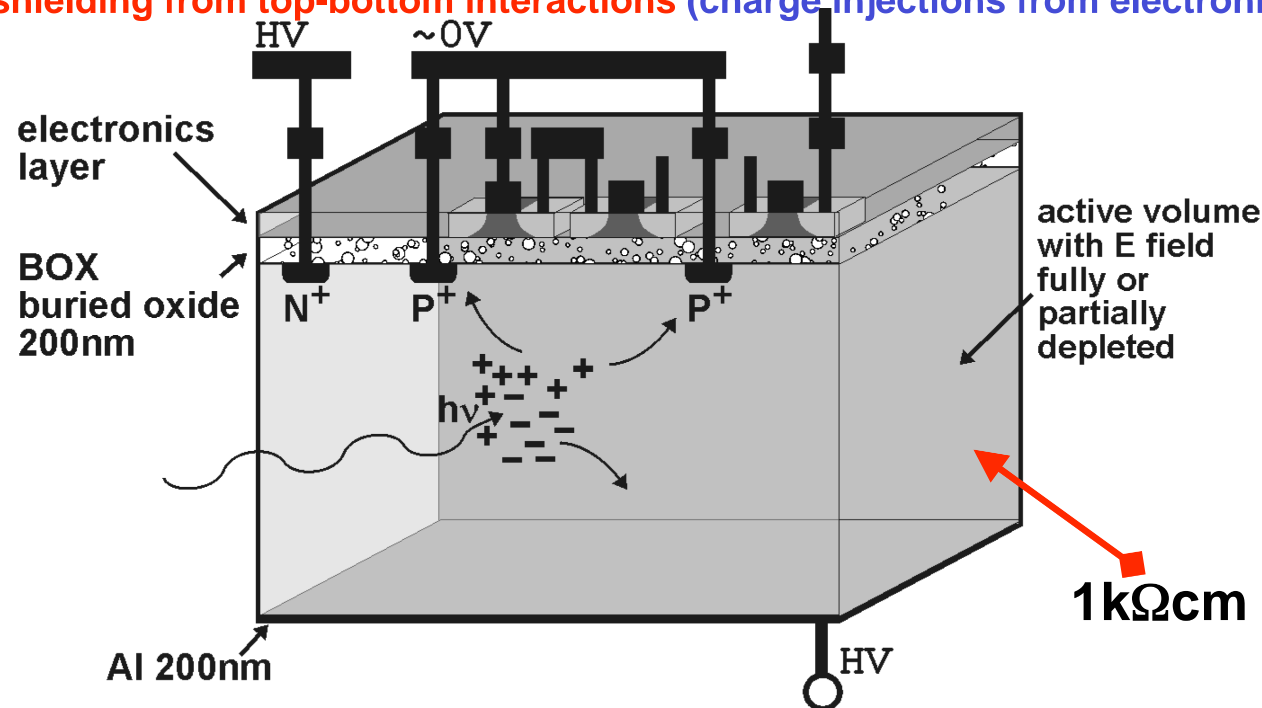
pixel = continuous pulse processing, discriminator (for BC time), peak detector and asynchronous ADC, trimming DAC seems difficult to avoid, no deadtime

pixel = digital memory blocks/buffers for storing #BCs and pulse height information, difficult to avoid broadcasting current #BC.

Fermilab

Monolithic SoI detectors;

- A bonded wafer (high resistive substrate + low resistive top Si),
- Standard CMOS electronics (NMOS, PMOS, MIM cap, etc. can be used for circuit design),
- Thru BOX vertical contacts reaching handle wafer for connectivity eliminating bump bonds (lower cost, ready to use thin monolithic device) + n and p type implants in the handle wafer,
- Small size and high density of thru BOX contacts (smaller pixel size is possible and efficient use of upper Si design of electronics),
- Use of handle wafer in partial or full depletion with controlled/limited electric field gradients close to the surface (gradients of Efield should be harmless for transistor operation),
- Way of shielding from top-bottom interactions (charge injections from electronics activity),



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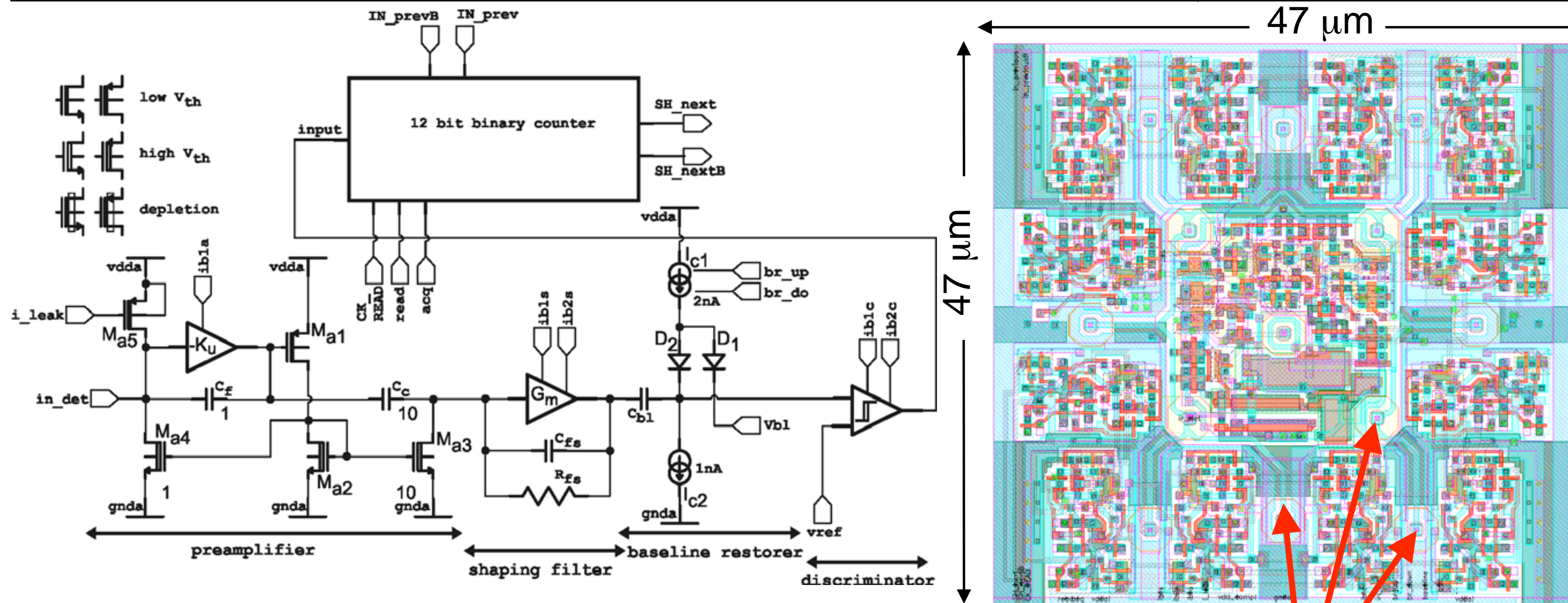
Monolithic SoI detectors;



Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、~1k Ω-cm (*n-type*), 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).

OKI 0.15 μm Process description

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Conclusions:

Actually ther are no conclusions yet, the work has just been started, so I will skip conclusions

3DIC development for HEP has to be done on several fronts:

1) Choice of 3DIC technology (vendor) and assure access,
2) Selection and design of IC,
3) Choice of technology for sensors,
4) Exploration of high density low mass bonding technology.

All these inseparably and closely related