Contribution ID: **202** Type: **Plenary**

Getting ready for next generation computing

Thursday, 6 November 2008 09:00 (40 minutes)

The ALICE High Level Trigger is a high performance computer, setup to process the ALICE on-line data, exceeding 25GB/sec in real time. The most demanding detector for the event reconstruction is the ALICE TPC. The HLT implements different kinds of processing elements, including AMD, Intel processors, FPGAs and GPUs. The FPGAs perform an on the fly cluster reconstruction and the tracks are planned to be computed on GPUs for speed. The ALICE event reconstruction software is designed from scratch to support multi core architectures. The status of the system- and analysis code architecture, which are optimised for speed are presented.

Several design and programming features of the ALICE HLT have been integrated into the plan to build a T2 "Landesrechner"in Frankfurt with up to 3000 processing nodes. The architecture and status of the project will be outlined. The planned system is founding member of the German Gauss Alliance.

Summary

Programming for multi core architectures and also FPGAs requires special attention. An outline of the key aspects is given together with the special requirements of the HEP event reconstruction. The availability of high performance computing able GPUs makes their use very attractive with respect to their cost. The planned architecture of the ALICE HLT, using both FPGAs and GPUs is discussed together with the next planned steps to build a general purpose high performance computer based on those principles

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Session Classification: Thursday, 06 November 2008

Track Classification: 2. Data Analysis