ALICE Inner Tracking System (ITS) Upgrade Overview

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4th ALICE ITS, MFT and O2 Asian workshop
Pusan, South Korea, 15-16 December 2014

ALICE ITS Upgrade Overview

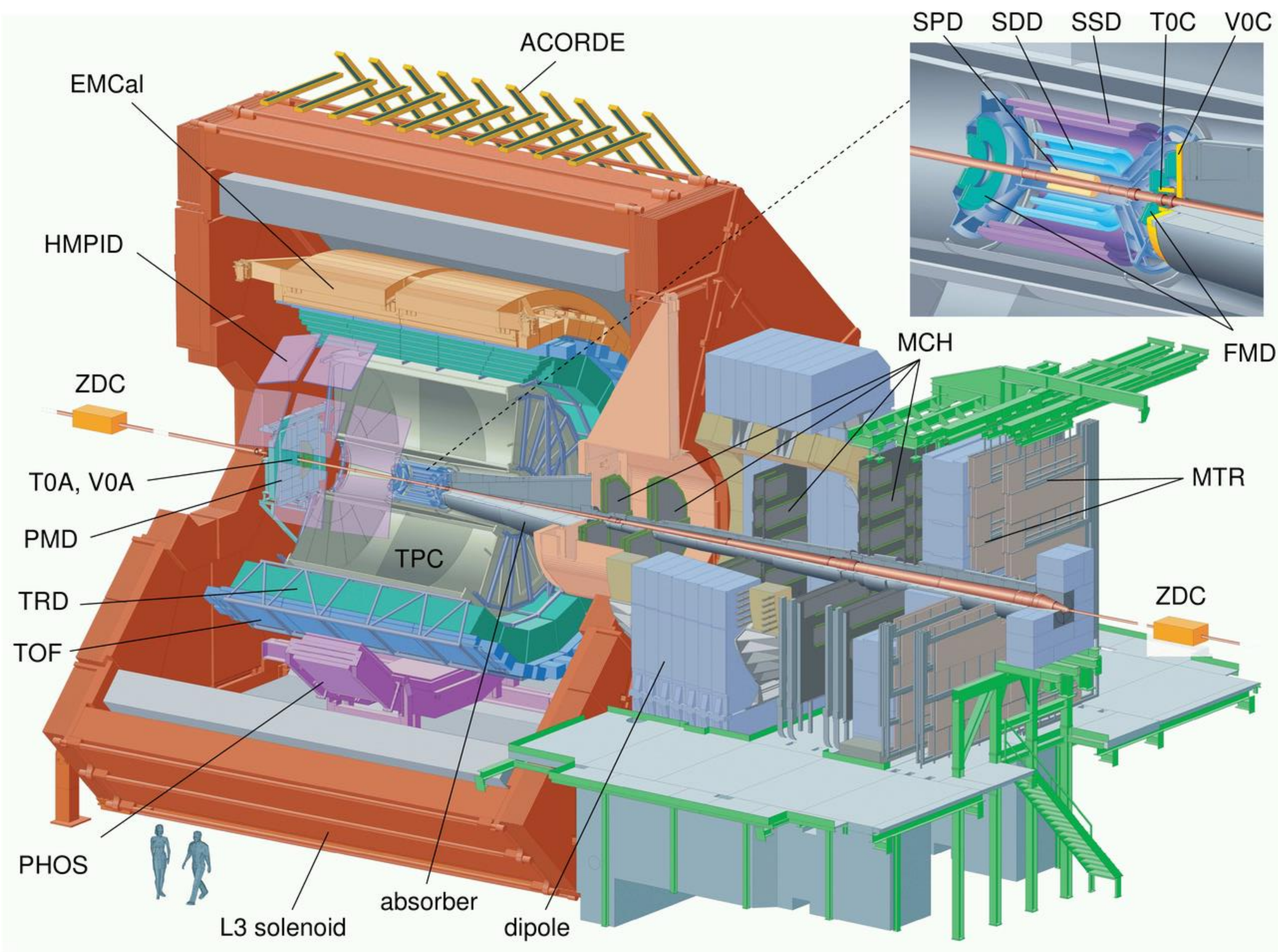
Status and Plans

OUTLINE

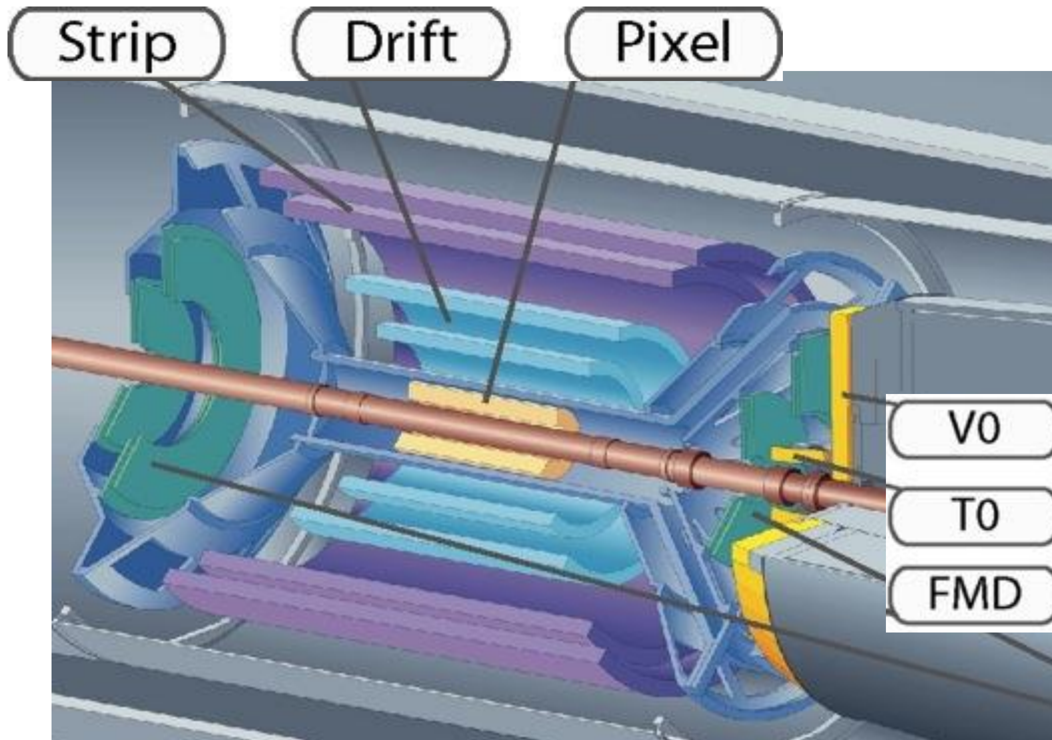
- Upgrade of the ALICE ITS: motivations and specifications
- Layout and main components of the new ITS
- Status and plans
- Conclusions

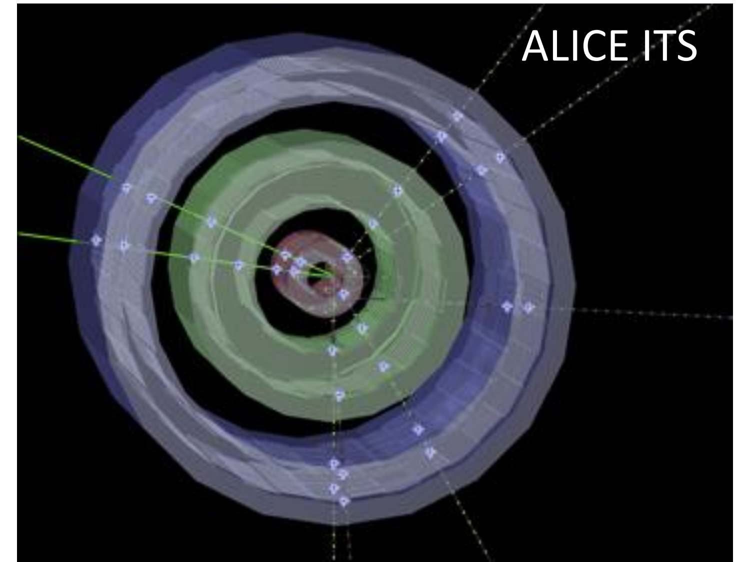
Disclaimer: this talk is not a comprehensive review of the ITS upgrade
but rather focuses on the aspects of the project relevant with Asian contribution

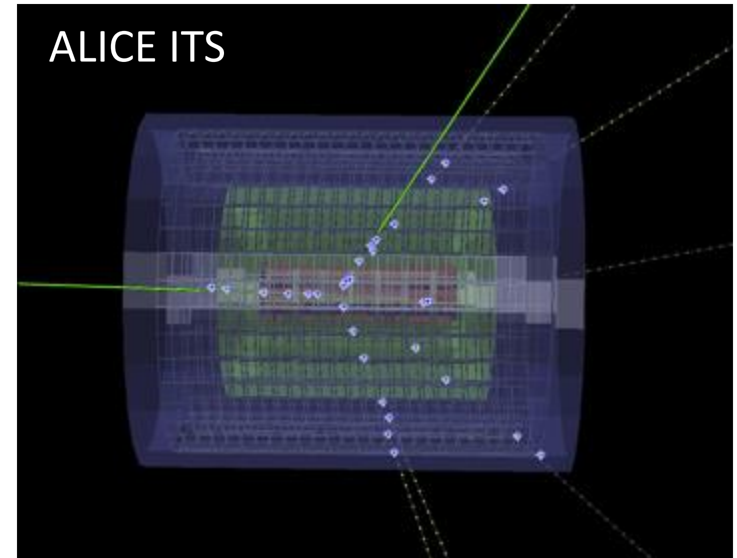
The Current ALICE Detector



The Current ALICE Inner Tracking System







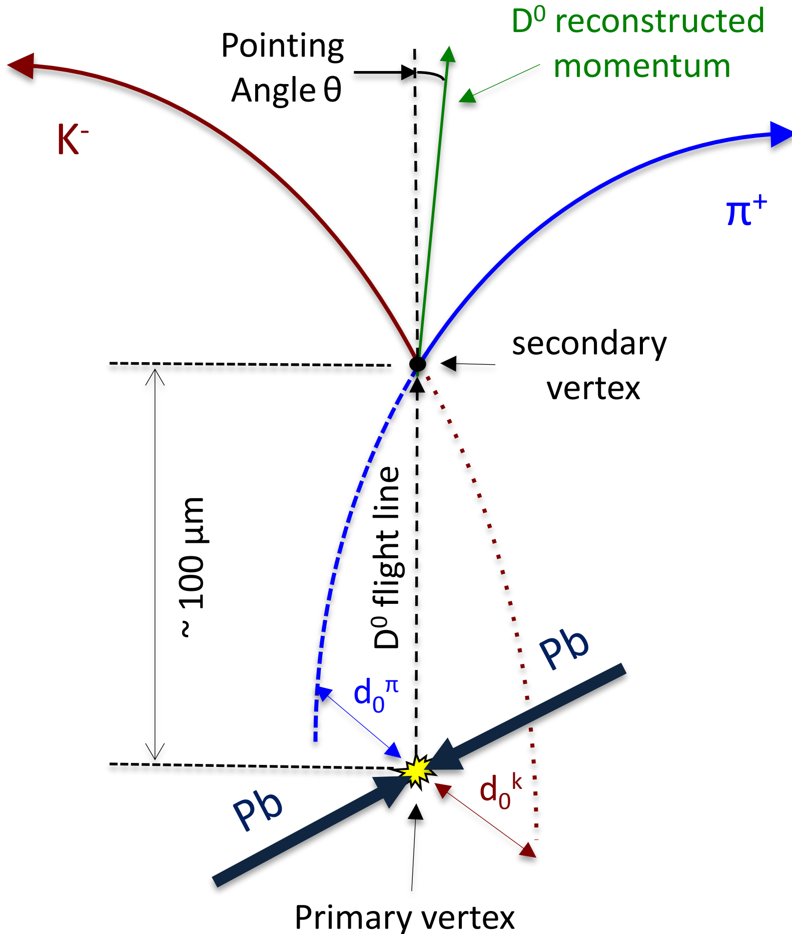
Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

Performance – Secondary vertex determination

Example: D^0 meson



Analysis based on decay topology and invariant mass technique

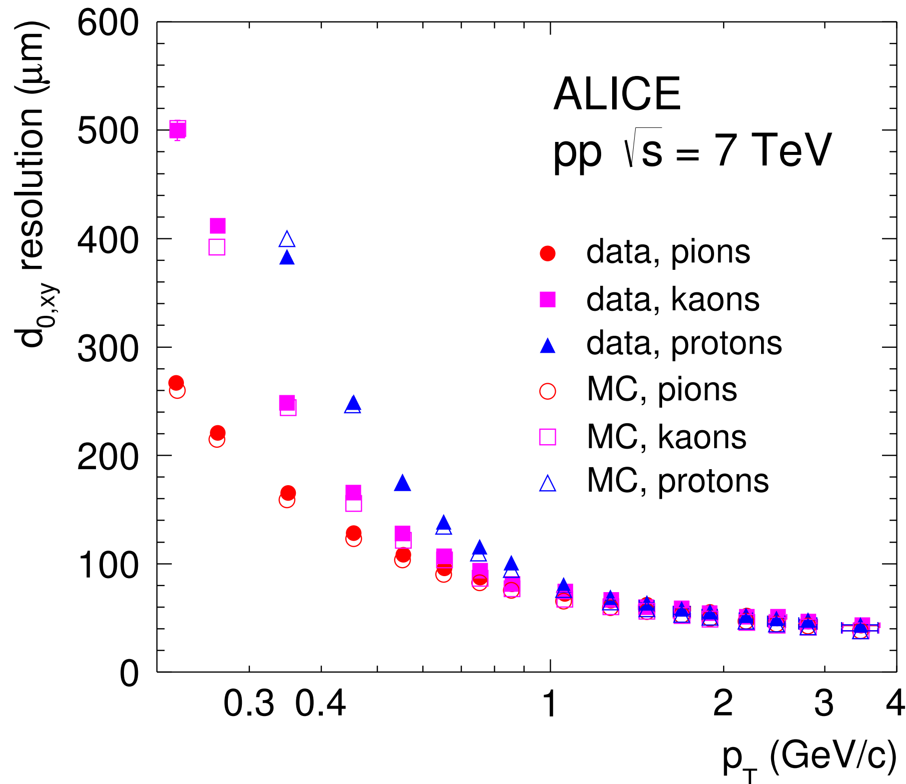
Open charm

Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

How precisely is d_0 measured with the current ITS detector?

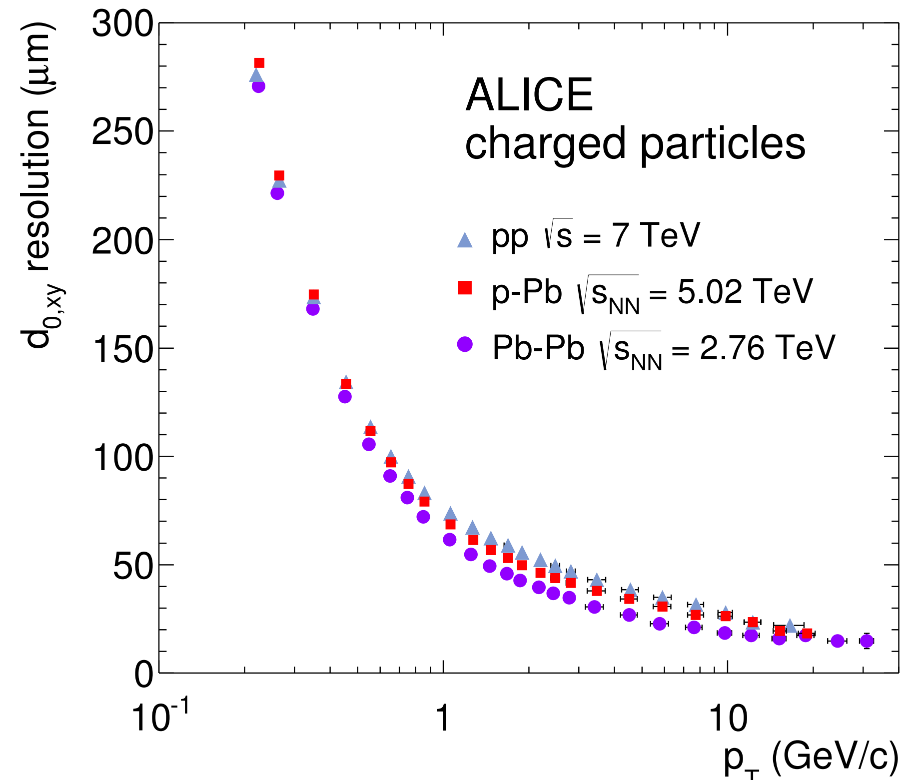
ALICE ITS Upgrade – Impact parameter resolution

Very good MC description



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

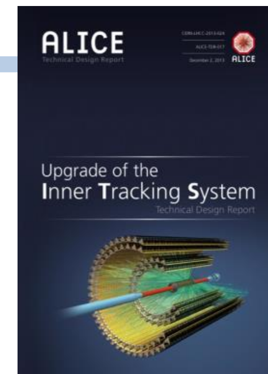
Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

110 - 120 μm at p_T = 500 MeV/c

Upgrade design objectives



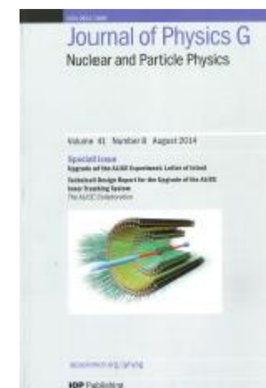
CERN-LHCC-2013-24

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡ 22mm
- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50µm x 425µm ➡ 28µm x 28µm

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers ➡ 7 layers
  - silicon drift and strips ➡ pixels



J. Phys. G (41) 087002

3. Fast readout

- readout Pb-Pb interactions at > 50 kHz and pp interactions at ~ 2 x 10^5 Hz (currently limited at 1kHz with full ITS and ~3kHz without silicon drift)

4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera
(~10 m^2)

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

r coverage:
22 – 400 mm

Outer layers

Middle layers

Inner layers

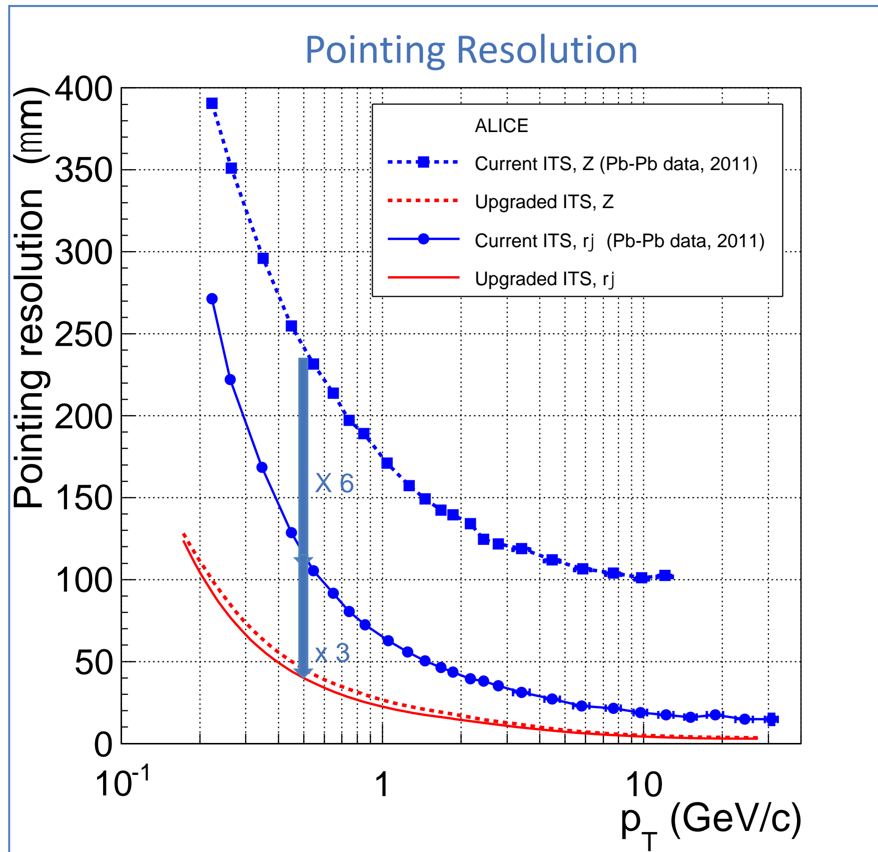
Beam pipe

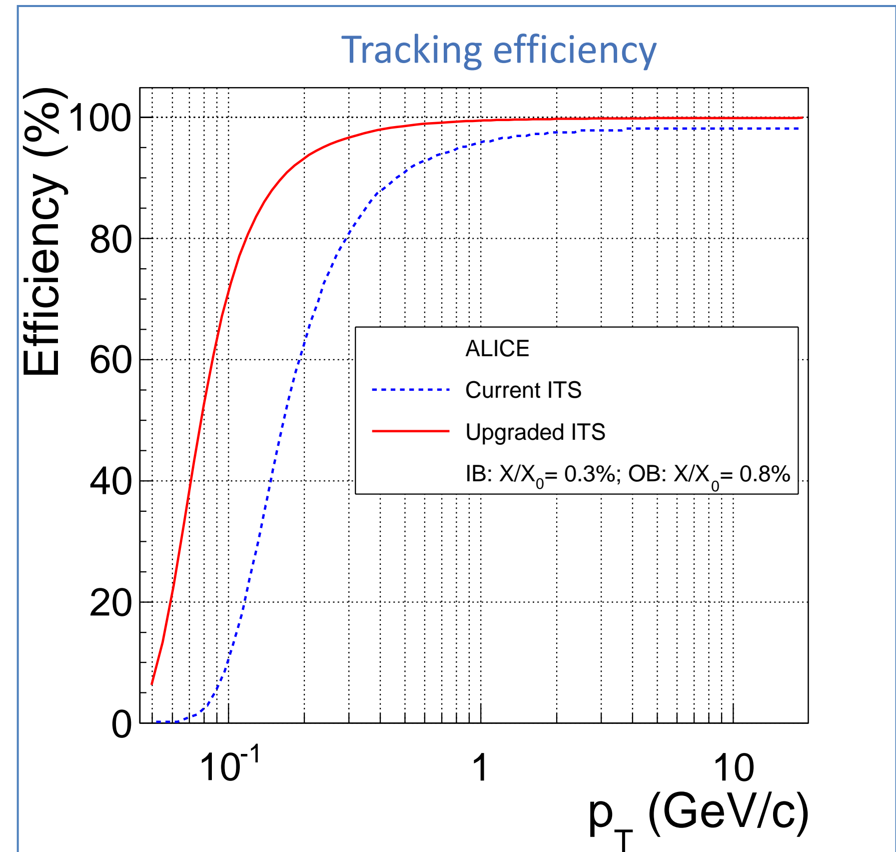
7 layers of MAPS

700 krad/ 1×10^{13} 1 MeV n_{eq}
includes safety factor 10

Inner Barrel = Inner Layers
Outer Barrel = Middle Layers + Outer Layers

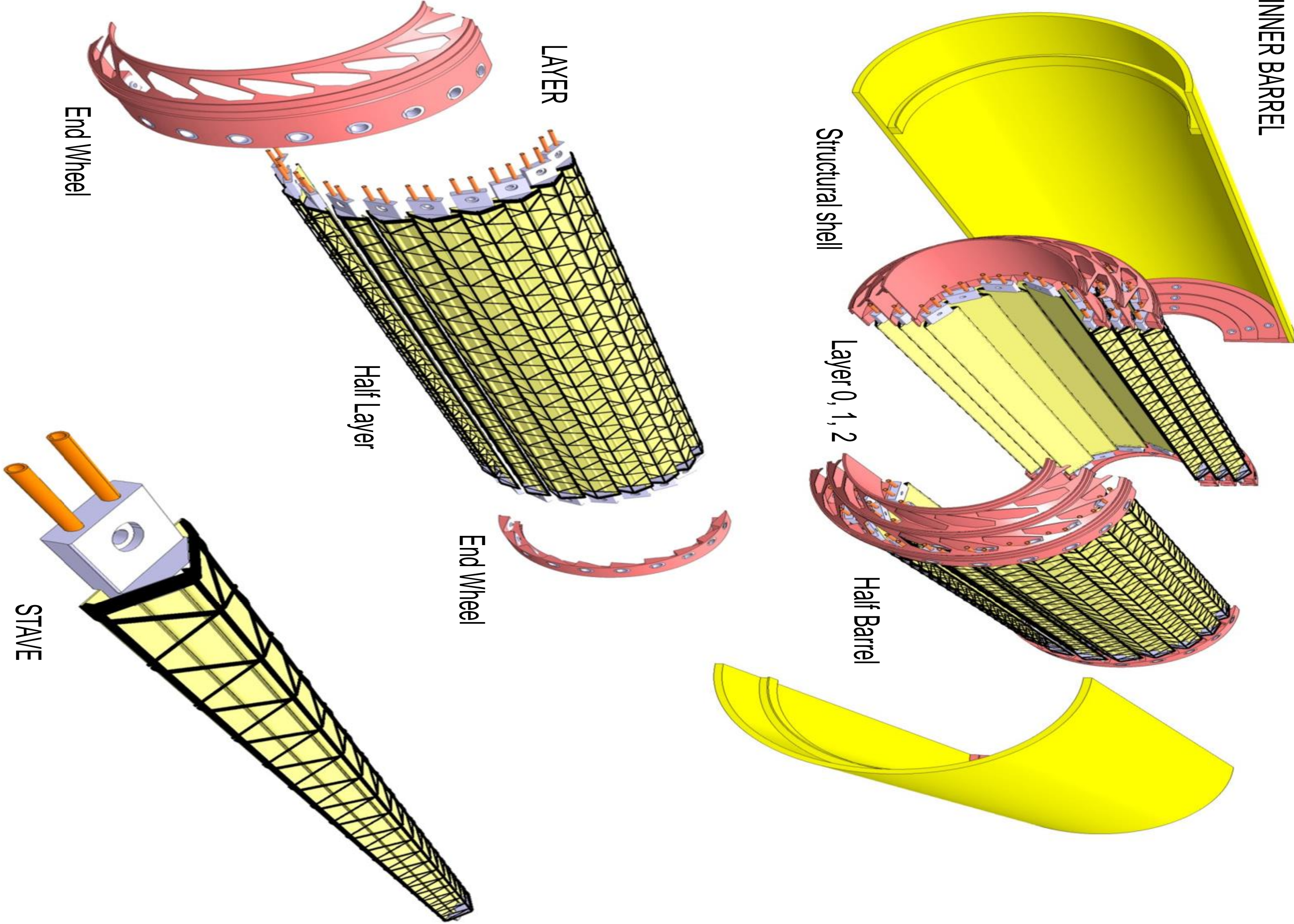
Performance of new ITS



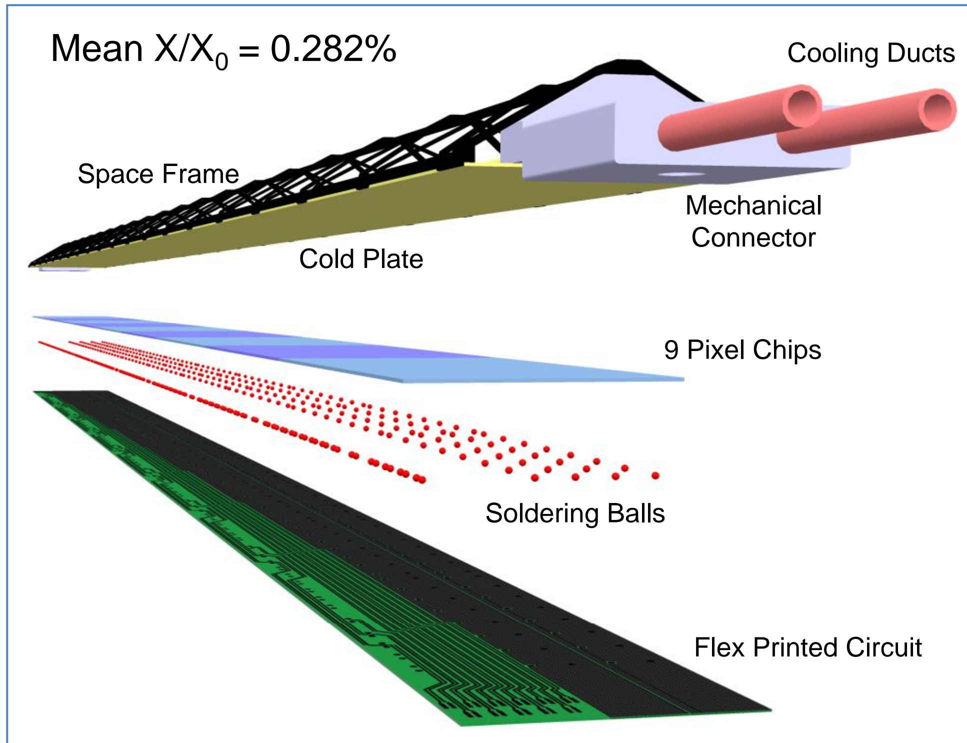


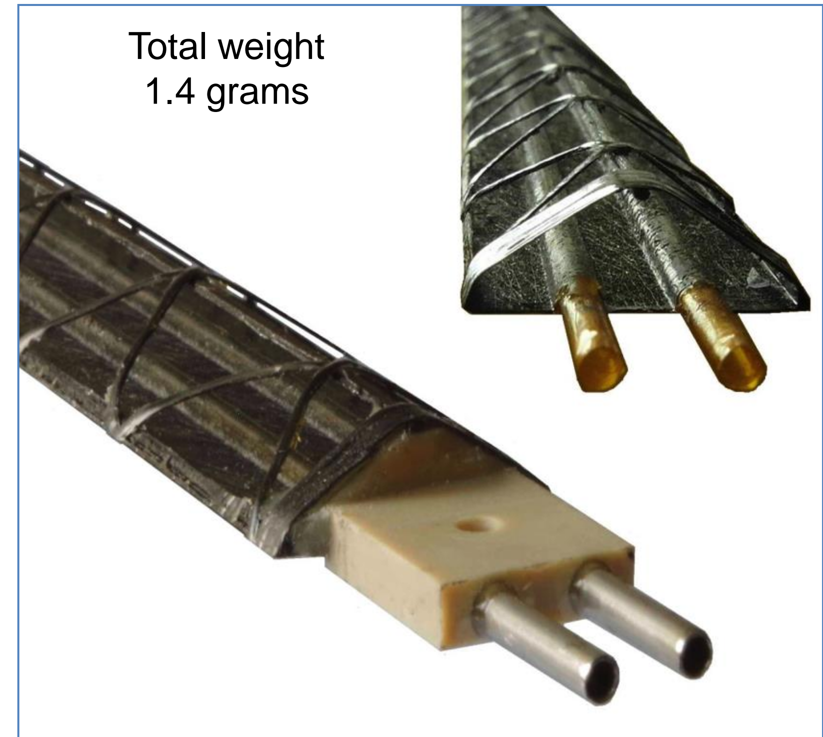
~40 µm at p_T = 500 MeV/c

Inner Barrel



New ITS Layout - Inner Barrel





<Radius> (mm): 23,31,39

Length in z (mm): 270

Nr. of staves: 12, 16, 20

Nr. of chips/stave: 9

Nr. of chips/layer: 108, 144, 180

Material thickness: ~ 0.3% X_0

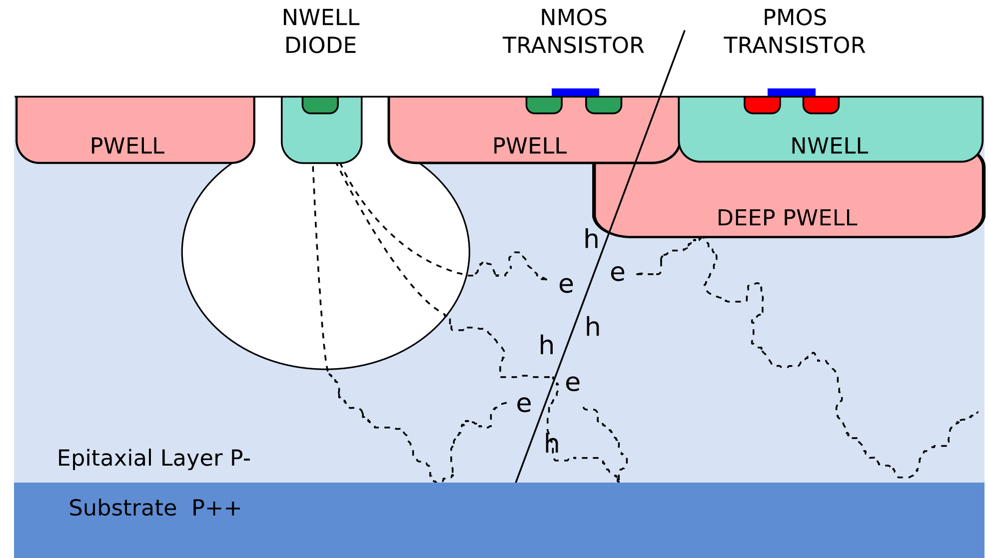
Power density: < 100 mW/cm^2

Throughput (@100kHz): < 80 Mb/s × cm^{-2}

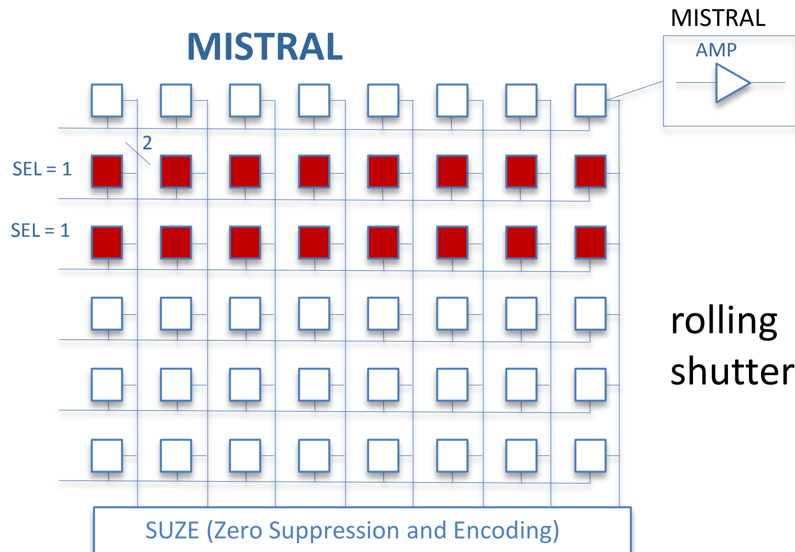
PIXEL Chip

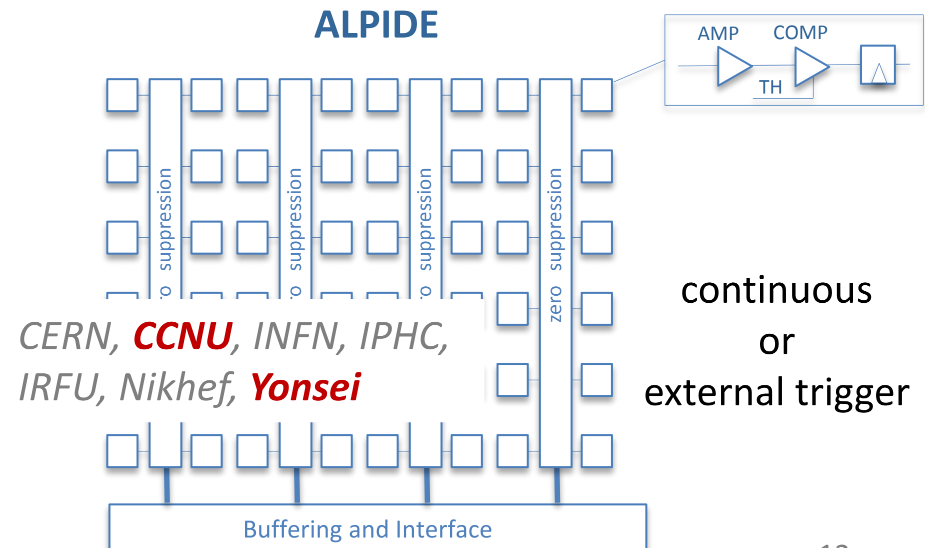
Monolithic PIXEL chip using Tower Jazz CMOS 0.18 μm

- Chip size: 15mm x 30mm
- Pixel pitch ~ 30 μm
- Spatial resolution ~ 5 μm
- Power density < 100 mW/cm^2
- Architectures: MISTRAL, ALPIDE



Deep p-well allows truly CMOS circuit inside pixel





Pixel Chip - ALPIDE and MISTRAL full-scale prototypes in 2014

MISTRAL FSBB-M0 (Full Scale Building Block Mistral 0)

- **About 1/3 of a complete sensor** (approx. **9mm x 17mm**)
- 416 x 416 pixels of **22μm x 33μm** (final chip **36μm x 62μm**)
- **40μs** integration time (final chip **~ 20μs**)
- Full chain working (front-end, discr., zero suppression)
- Chips (non irradiated) characterized at SPS

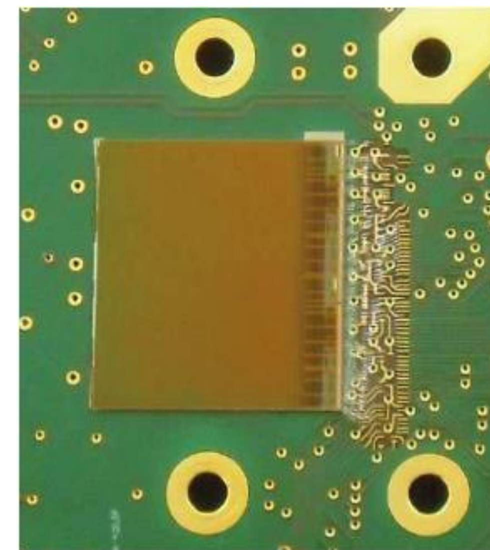


Figure: Two FSBB M0

ALPIDE Full Scale prototype

- Dimensions: **30mm x 15 mm**
- About 0.5 M pixels **28μm x 28μm**
- **40 nW front-end (4.7mW / cm^2)**
- ~40mW/cm^2 total
- Pulse width ~5 μs

Figure: picture of pALPIDEfs

Chips characterized at PS, SPS, Frascati
⇒ Results presented by Magnus
⇒ Characterization at Korea test beam, analysis ongoing

Pixel Chip – plans till production (1/2)

ALPIDE: baseline solution

- Based on the results obtained in about 8 months of characterization, the current version of ALPIDE (p-ALPIDE1) represents already a suitable solution for the detector construction
- Completion and optimization of the chip via three new iterations

Version	**Description**	**Subm (to TJ)**	**Delivery**	**Test**
pALPIDE-2	final interface but no HSO	Dec 14	Feb 15	Feb – Jun 15
pALPIDE-3	Pixel FEE optimization, HSO (1.2 Gbit/s), in-pixel multi-event buffer, standard-cell version of matrix readout	Apr 15	Jun 15	Jun - Oct
ALPIDE final	Possible minor improvements	Aug 15	Oct 15	Nov - Jan

- Production (~1400 wafers) starts Feb '16
- Module and stave development programme in 2015 based on ALPIDE prototypes => *presentations of Petra, Antonello and Vito*

Pixel chip – plans till production (2/2)

MISTRAL-O (optimized for the Outer Barrel): fallback solution

The development of MISTRAL-O will be brought to completion, including the integration in the detector module and stave

- Mature architecture: based on the MIMOSA family
- Pixel pitch ~36μm x 62μm for a power of ~100mW/cm^2
- The characterization of MISTRAL (22μm x 33μm) FSBB in 2014 produced good results
- The basic building blocks have been qualified as standalone circuits in ‘13 and ‘14

Version	Description	Subm (to TJ)	Delivery	Test
MISTRAL-O	(first) prototype with all final functionalities	June ‘15	Sep ‘15	Oct – Dec ‘15

- Qualification of OB modules and stave based on MISTRAL-O: Jan ‘15 – Apr ‘16

Plans for 2015 (and 2016) – Pixel Chip

Production and test of pixel chips

- Procurement of high resistivity silicon wafers (1500 wafers): 2015
- QA of raw silicon wafers (~10% of the total number): Jul ‘15 – Feb ‘16
  - Verification of physical and electrical properties (measurement of resistivity) => TMEC (Thailand)
- CMOS Manufacturing
  - 4 lots, 340 wafers each: Feb ‘16 – Jun ’17 => TowerJazz
- CMOS QA
  - A new lot starts only after the test (wafer probe test) of about 5% of previous lot => Yonsei (Korea) (tbc)
- Ni-Au plating => (e.g. Pactech) market survey and tendering started
- Thinning & Dicing => (mechanical or Laser?) e.g. Rockwood, Stars
- Chip Test (Electrical, visual) => Yonsei, LIPI (Visual Inspection)

Plans for 2015 – Module assembly

Construction of Modules and staves for the Inner Barrel and Outer barrel

- Procurement of Module Assembly Machine (MAM) => *see Antonello*
    - First delivery (CERN): Jun ‘15
    - Others: (Bari, Liverpool, Pusan, Strasbourg, Wuhan (tbc)): Jan–Jun ’16
- Qualification of MAM and assembly procedure at CERN (participation of all teams involved in Module construction): Jul–Sep ’15
    - Qualification (acceptance test) of MAM
    - Verification and optimization of assembly procedure
    - Verification and optimization of test procedure

Plans for 2015 – Readout electronics

Readout Electronics: plans for 2015

- Electrical signaling and communication protocol between RU and detector module defined
- Test of data transmission and bit error rate: done in 2014
  - Commercial LVDS transceivers (Nikhef, Prague, Kosice)
- To be done
  - Test communication via high-speed link (400 Mbit/s, 1.2 Gbit/s)
  - Test communication using parallel bus and control lines
    - pALPIDE-3
    - Test system developed by Bari => *see Vito*
  - Develop an FPGA-based system emulator COMSATS
  - Readout Unit prototype integrating link to CRU and Trigger

Conclusive Remarks

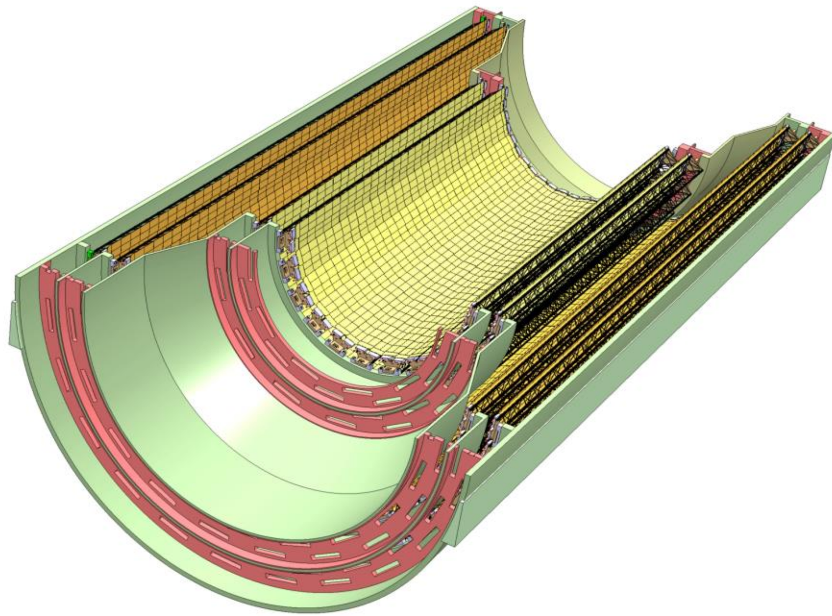
Important contribution of Asia to many critical aspects of R&D and construction.

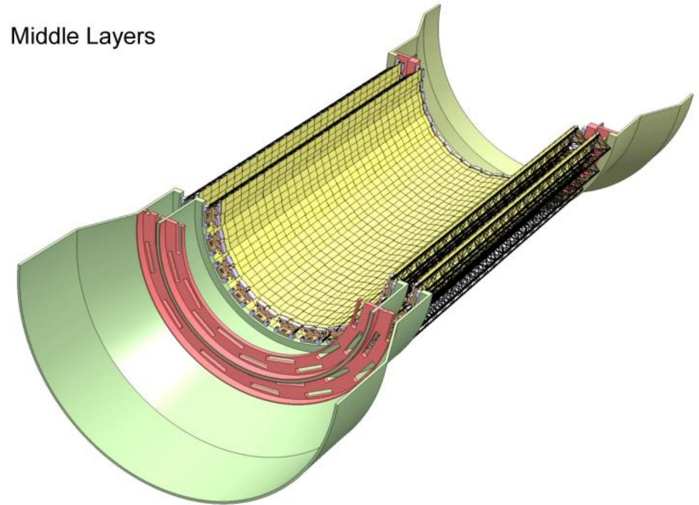
Some of the activities are well advanced (■), some are ramping-up (■), other have not yet started and need to be confirmed/consolidated (■)

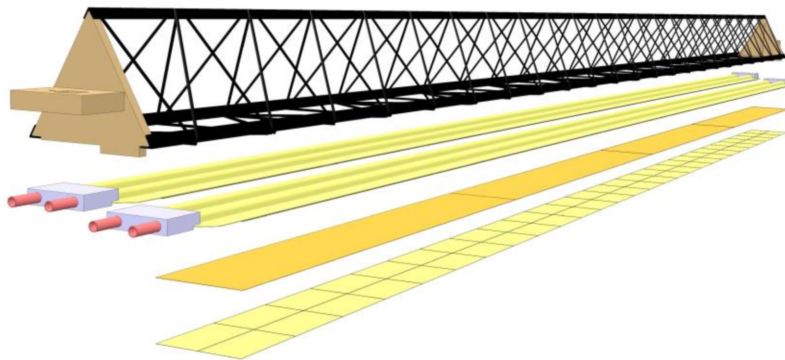
- China:
  - Pixel chip design, detector and physics simulations
  - OB module construction, readout electronics
- Korea:
  - Pixel chip design, pixel chip characterization, physics simulations
  - Pixel chip mass test, module construction, module construction QA
- Indonesia: Pixel chip mass test QA
- Pakistan: Pixel Chip TCAD simulations, FPGA-based system level simulation of stave readout
- Thailand:
  - Detector simulation, pixel chip characterization, silicon μ-channels
  - QA for CMOS raw wafers, CMOS wafers (laser) dicing

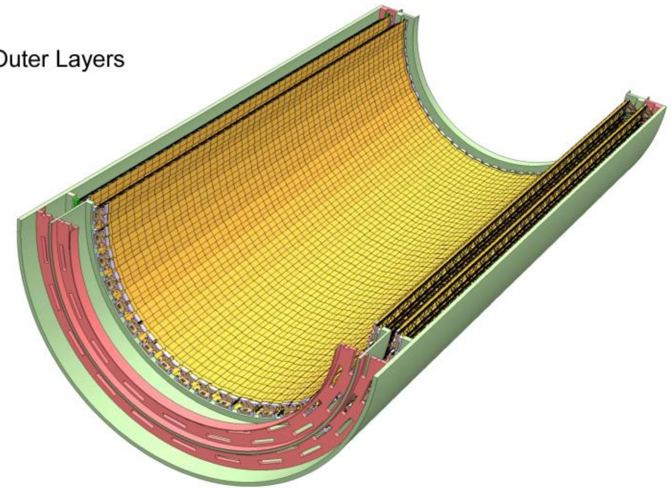
SPARES

Outer Barrel Support Structure and Assembly







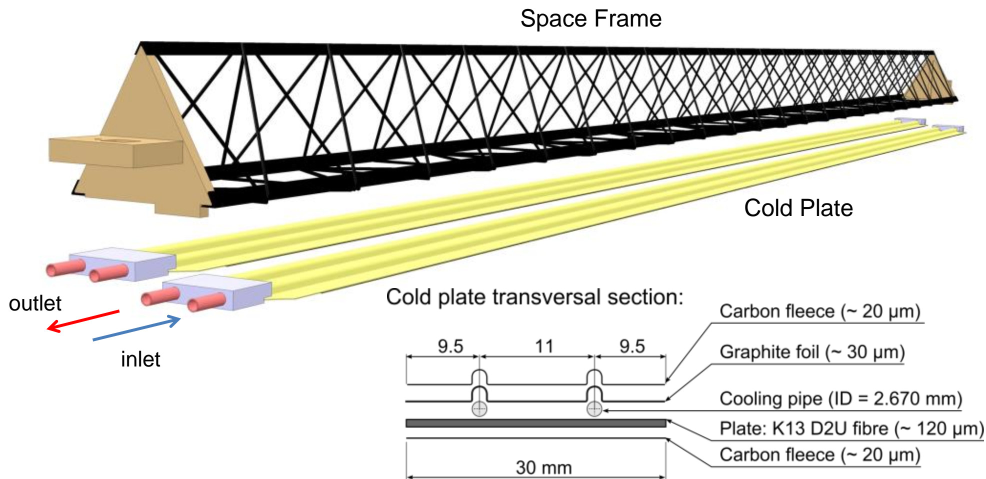


Main structural elements have been prototyped in 2014

Outer Barrel

Outer Barrel Stave

See presentation of Vito



Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Nr. staves: 22, 28, 40, 46

Nr. Chips/layer: (ML), (OL)

Power density < 100 mW / cm^2

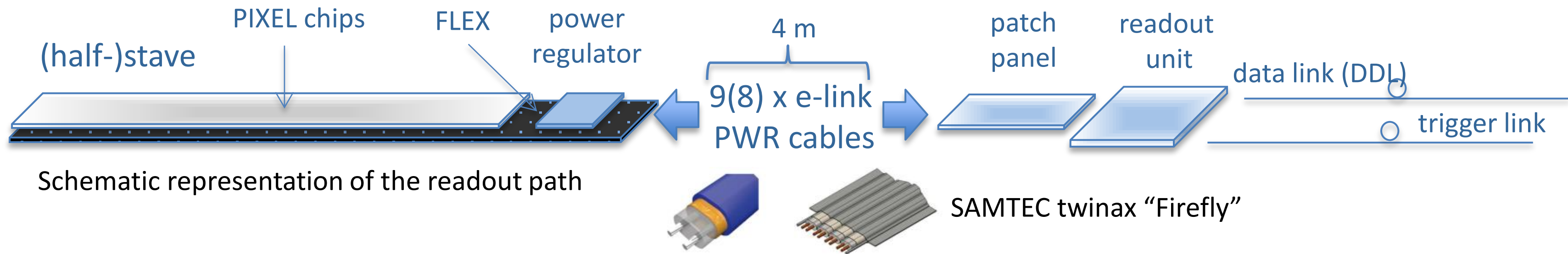
Length (mm): 843 (ML), 1475 (OL)

Nr. modules/stave: 4 (ML), 7 (OL)

Material thickness: ~ 0.8% X_0

Throughput (@100kHz): < 3Mb/s × cm^{-2}

Readout – general scheme and data throughput



Schematic representation of the readout path

Data throughput 324 Gbit/s
1008 electrical links

(184 DAQ optical links + n Trigger links)

no radiation

1 Mrad
10^{13} 1 MeV n_{eq}

10 krad
10^{10} 1 MeV n_{eq}

Trigger and CLK (GBT)

Central Trigger Processor

ITS Module

ITS Module

ITS Module

electrical (1 Gbit/s, 400Mb/s)

Readout Unit

Data Acquisition & Online Processing

Data and Control (GBT)

Detector Control System

On detector

off detector (~200 m)