A Large Ion Collider Experiment

INHA University

Sensor characterization at INHA

4th ALICE ITS upgrade, MFT and O_2 Asian Workshop 2014 @ KOREA

15 - 16 Dec 2014

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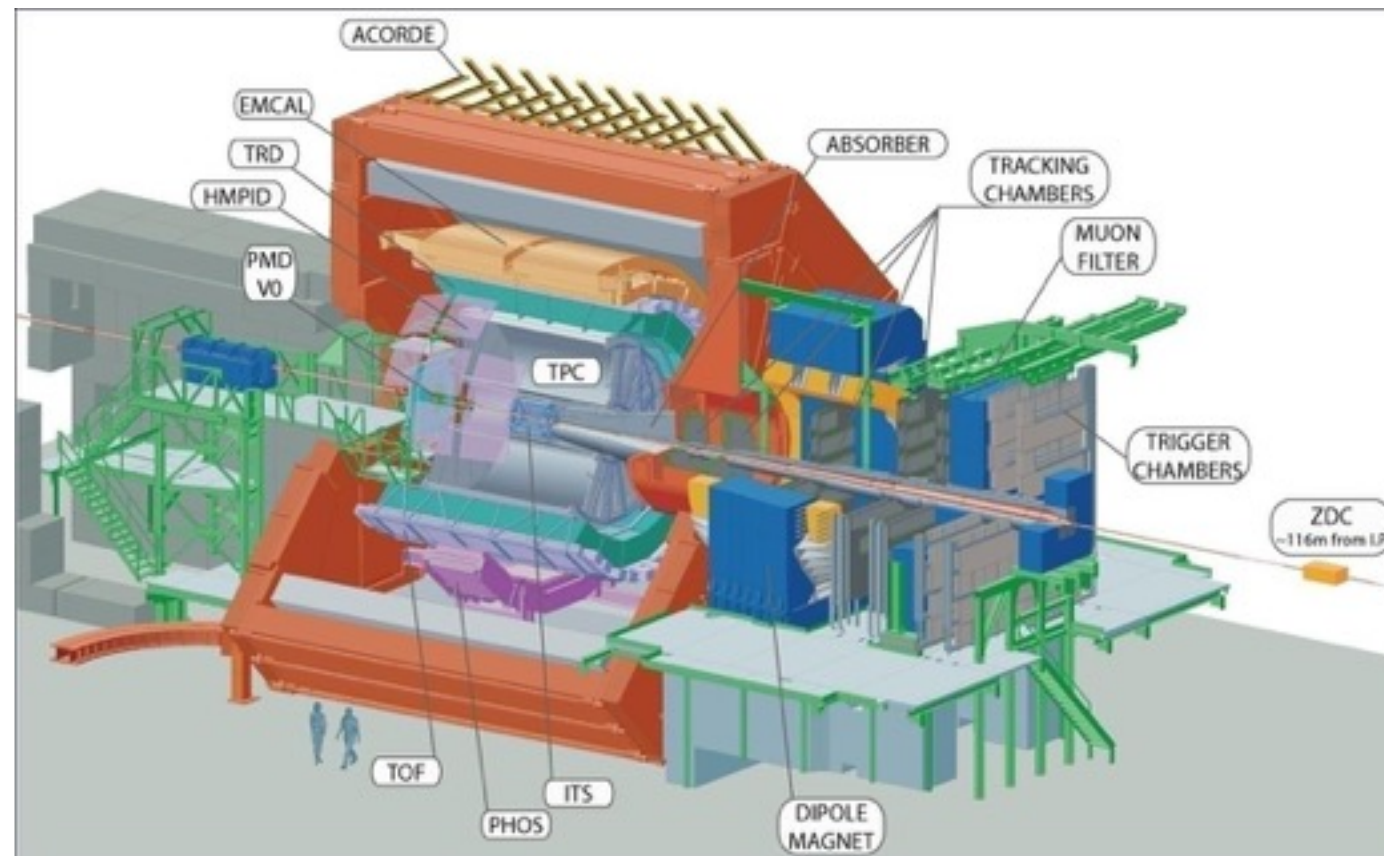
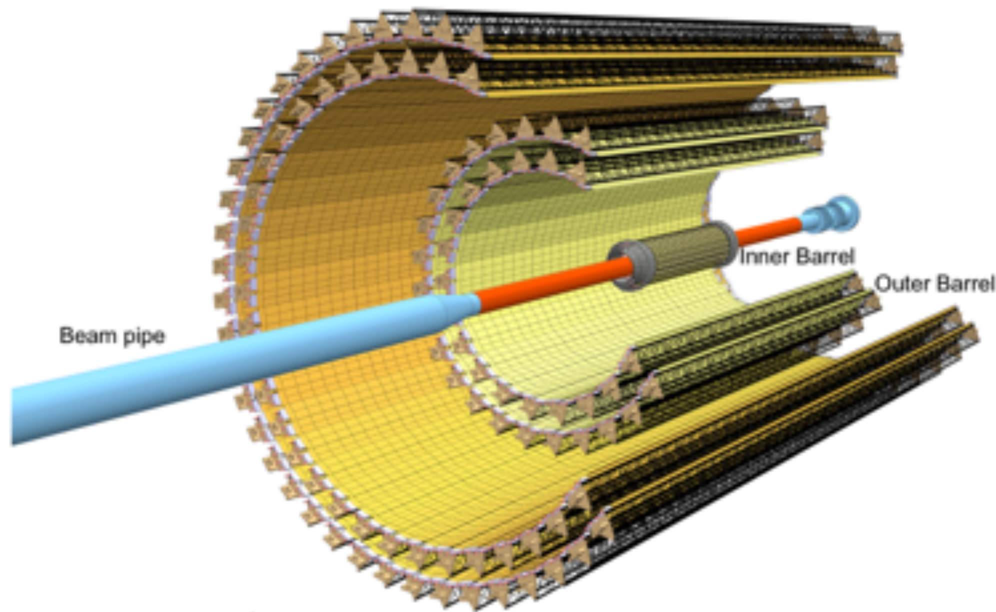
Physics Motivation



A Large Ion Collider Experiment detector

- ALICE experiment is the dedicated heavy-ion experiment at the LHC.
- Characterization of QGP properties is done by studying multi-differential and unique observables such as light/heavy flavours, transverse momentum, flow, exotic objects etc.
  → It requires high statistics and precision measurements.
- ITS upgrade allows us to imporve vertexing and tracking toward precision measurement.

Inner Tracking System upgrade



New ITS layout

Advantage of new ITS

1. Impact parameter resolution increase by a factor of three
   * Displacement between beam pipe and 1st layer: 39mm →22mm
   * Material budget : ~1.14% → ~0.3%
2. Improve tracking efficiency and p_T resolution at low p_T
   * Increse granularity
   * Reduce pixel size
3. Fast read out
4. Fast insertion/removal for yearly maintenance

To do list at INHA

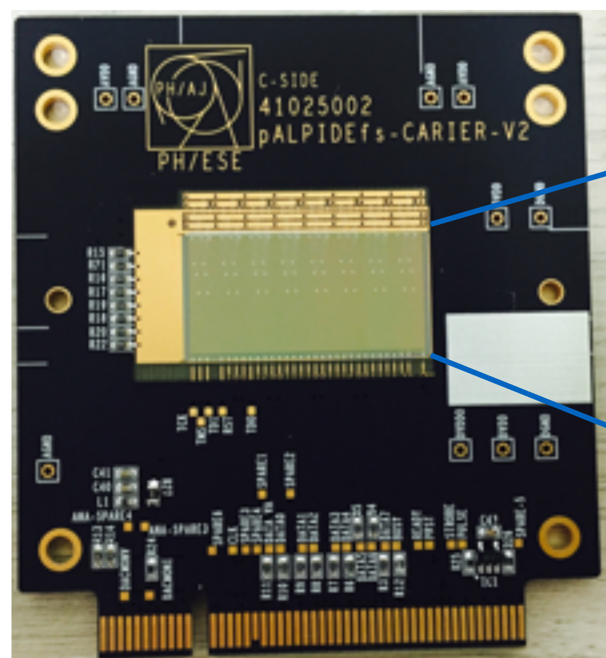
1. Chip characterization test setup - pALPIDEfs tests
   * Primary lab. test
     - FIFO, SCANDACS, THRESHOLD etc.
   * ^{55}Fe source scan
     - Chip response uniformity and cluster characteristics
2. Module assembly system setup (together with PNU in the future)

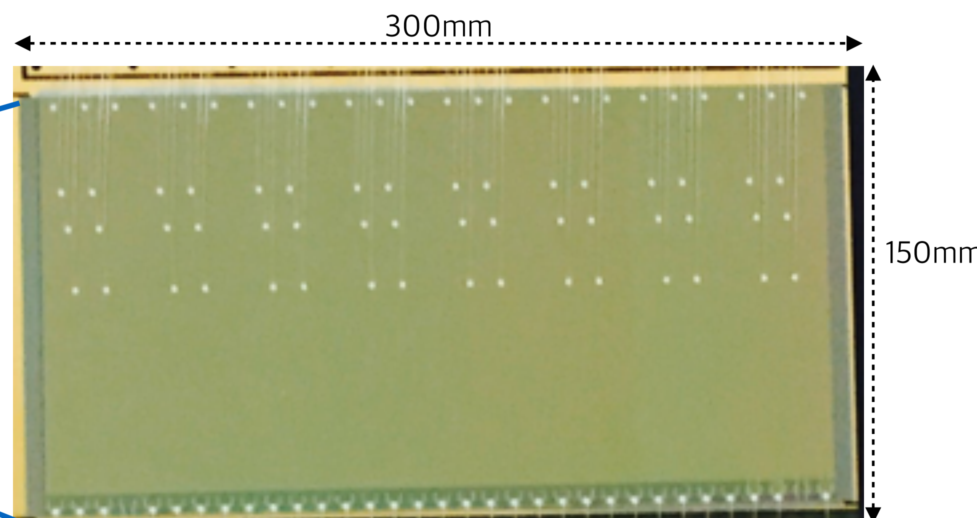
pALPIDEfs

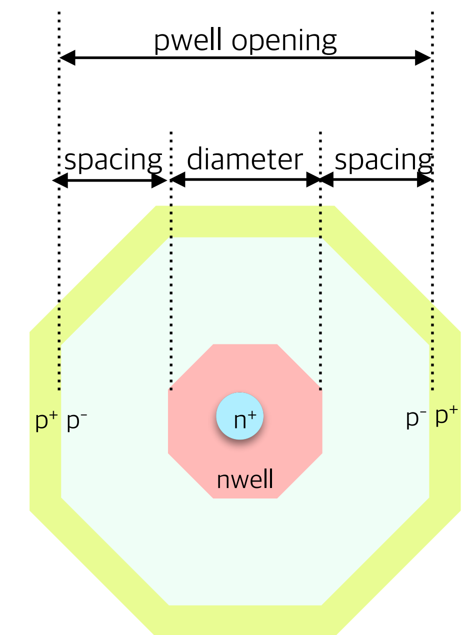
prototype ALPIDE full scale

- Based on Monolithic Active Pixel Sensor technology (MAPS)
- 1.5 × 30 cm^2
- 512 × 1024 sensitive pixels, 28 × 28 μm^2
- Four sub-matrices of 512 × 256 pixels
- Organized in 32 regions (512 × 32 pixels)
- Read out by 16 Priority Encoder circuits

Sector	nwell diameter	Spacing	pwell opening	Reset
1	2 µm	1 µm	4 µm	PMOS
2	2 µm	2 µm	6 µm	PMOS
3	2 µm	2 µm	6 µm	Diode
4	2 µm	4 µm	10 µm	PMOS







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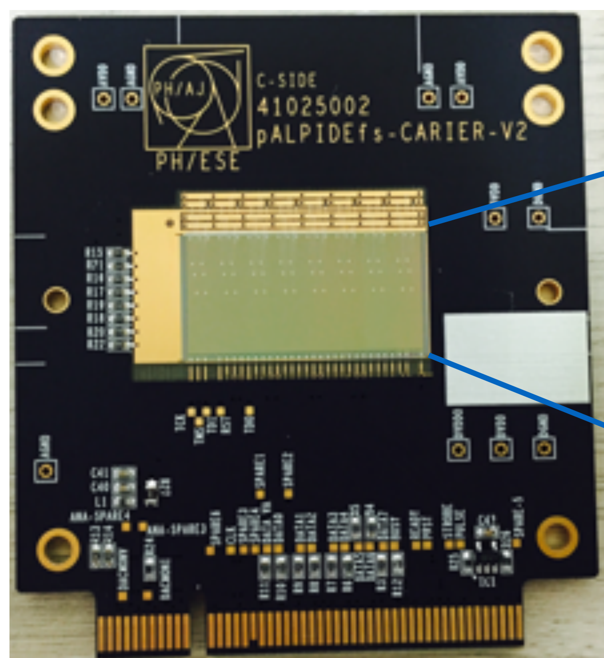

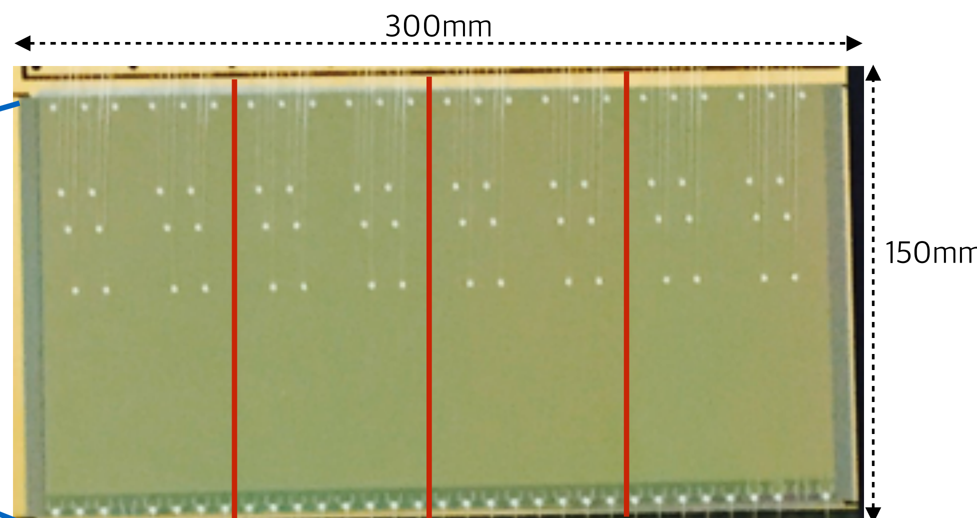

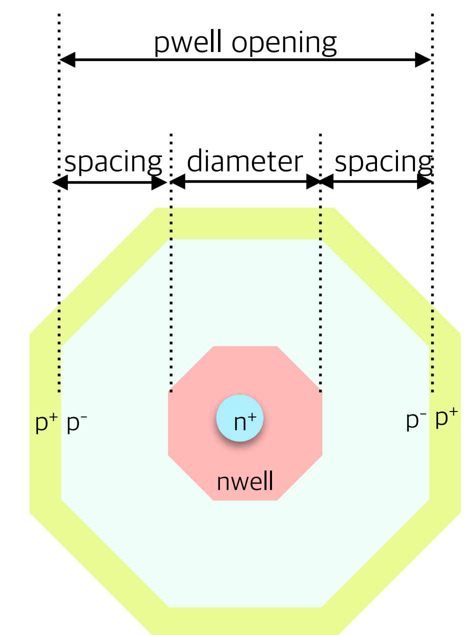

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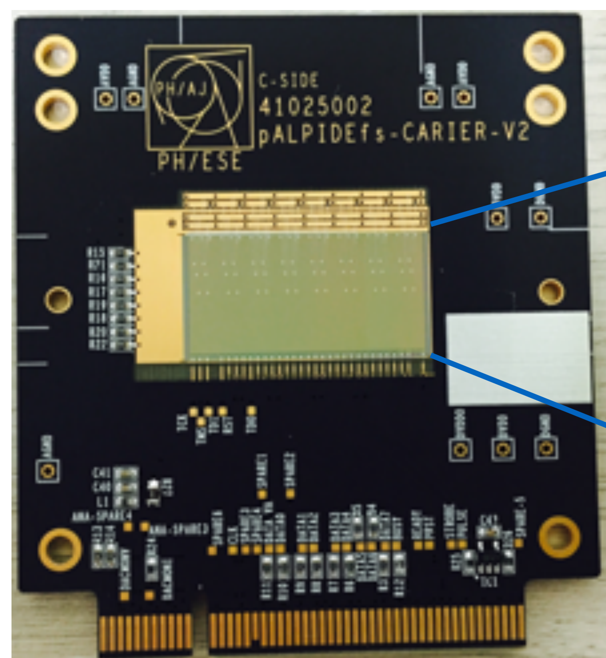
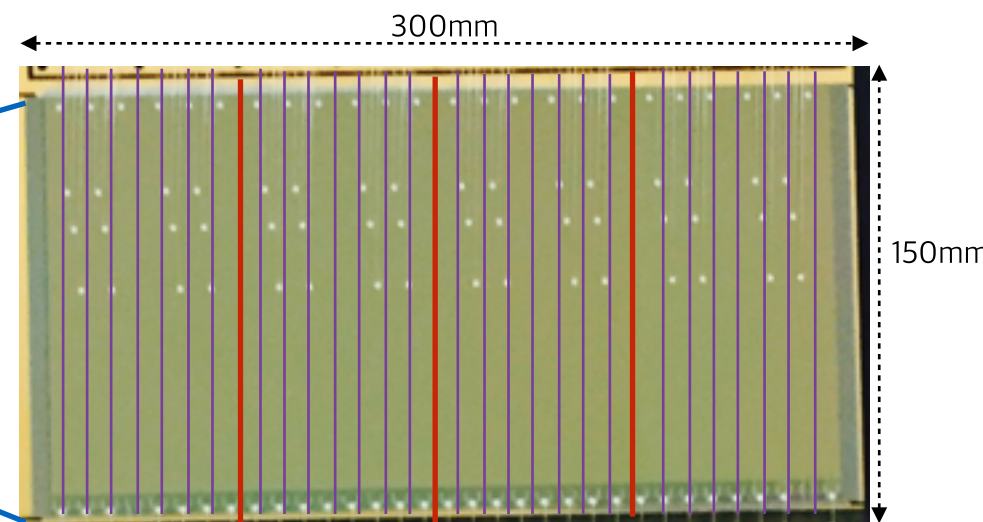
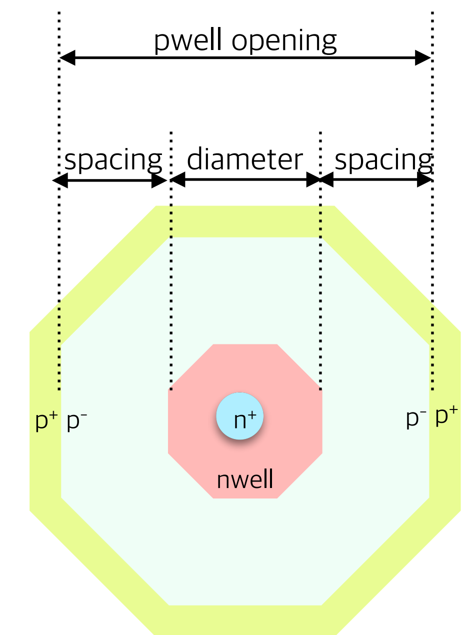
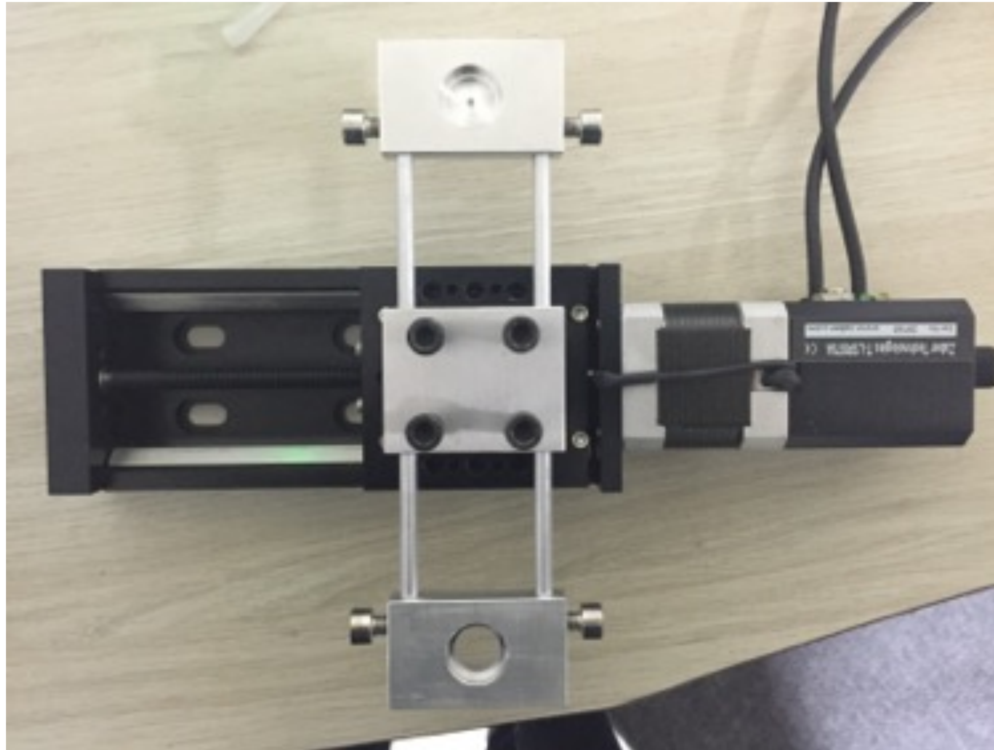
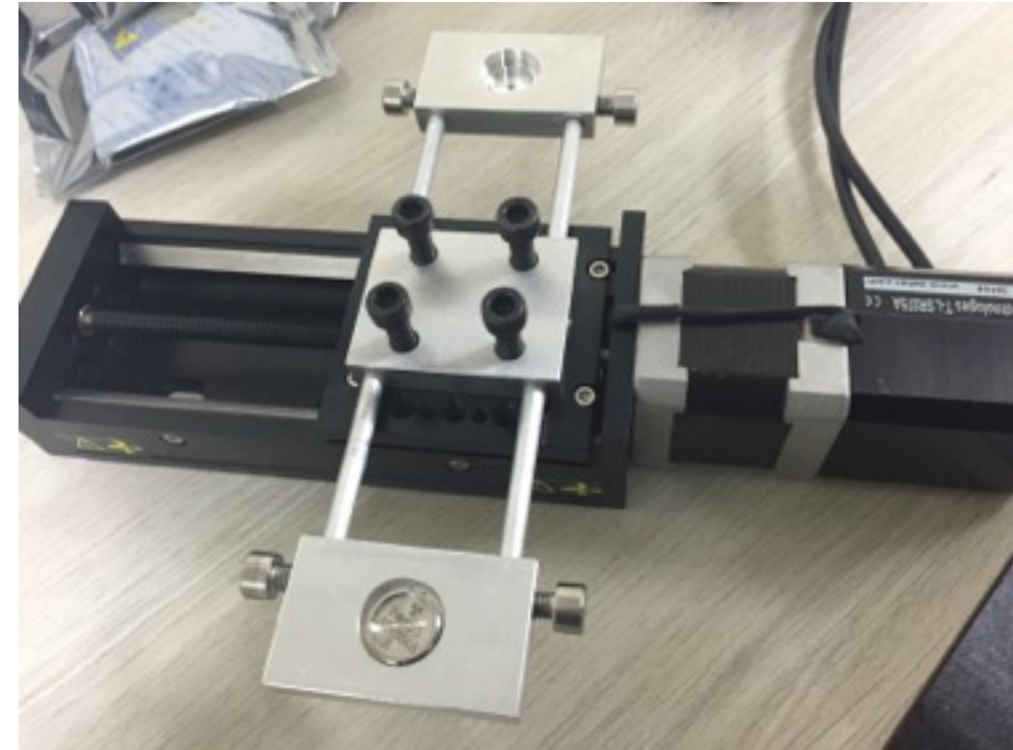


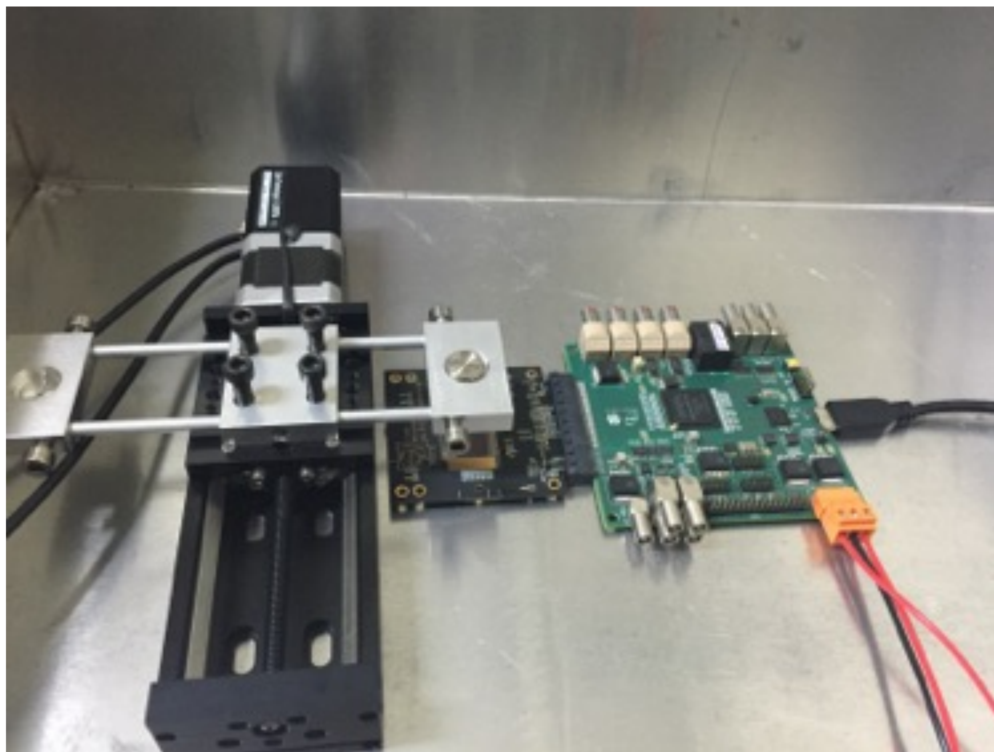




System in INHA







System in INHA

- Total 7 chips in INHA
- 1 thick chip + 6 thin chips
- Difference only wafer thickness
- DAQ board setting

Digital	1.8V	FPGA	1.8V
Analogue	1.8V	R18	500Ω

Primary lab test results for 7 chips

- All chips are performed by primary lab test (FIFO, SCANDACS, THRESHOLD)
- Checked IDD, IDDA values before and after configured

chip ID	Wafer	Die	STATUS	FIFO	SCANDACS	THRESHOLD
fs-1-39	1	39	OK	Passed	Done	Done
fs-2-20	2	20	OK	Passed	Done	Done
fs-6-17	6	17	OK	Passed	Done	Done
fs-6-22	6	22	OK	Passed	Done	Done
fs-8-29	8	29	OK	Passed	Done	Done
fs-9-20	9	20	OK	Passed	Done	Done
fs-9-21	9	21	OK	Passed	Done	Done

chip ID	nominal threshold (RMS)				noise			
	sector1	sector2	sector3	sector4	sector1	sector2	sector3	sector4
fs-1-39	189 (21)	189 (21)	166 (19)	193 (22)	9.8	7.7	3.6	6.3
fs-2-20	196 (19)	176 (17)	156 (15)	177 (17)	9.2	6.7	3.1	5.4
fs-6-17	202 (21)	178 (20)	156 (19)	177 (20)	9.8	6.8	2.8	5.6
fs-6-22	193 (18)	170 (17)	150 (16)	168 (17)	9.0	6.4	2.7	5.2
fs-8-29	169 (17)	152 (16)	135 (13)	152 (16)	7.8	6.3	2.9	5.1
fs-9-20	181 (18)	158 (17)	138 (14)	154 (16)	8.4	6.2	3.0	5.1
fs-9-21	194 (18)	171 (6.3)	149 (2.9)	163 (5.1)	8.8	6.3	2.9	5.1

Compare Threshold

Threshold

chip
fs1-39
fs2-20
fs6-17
fs6-22
fs8-29
fs9-20
fs9-21

240
220
200
180
160
140
120
100

1
2
3
4
Sector

Compare Noise

Noise

14
12
10
8
6
4
2
0

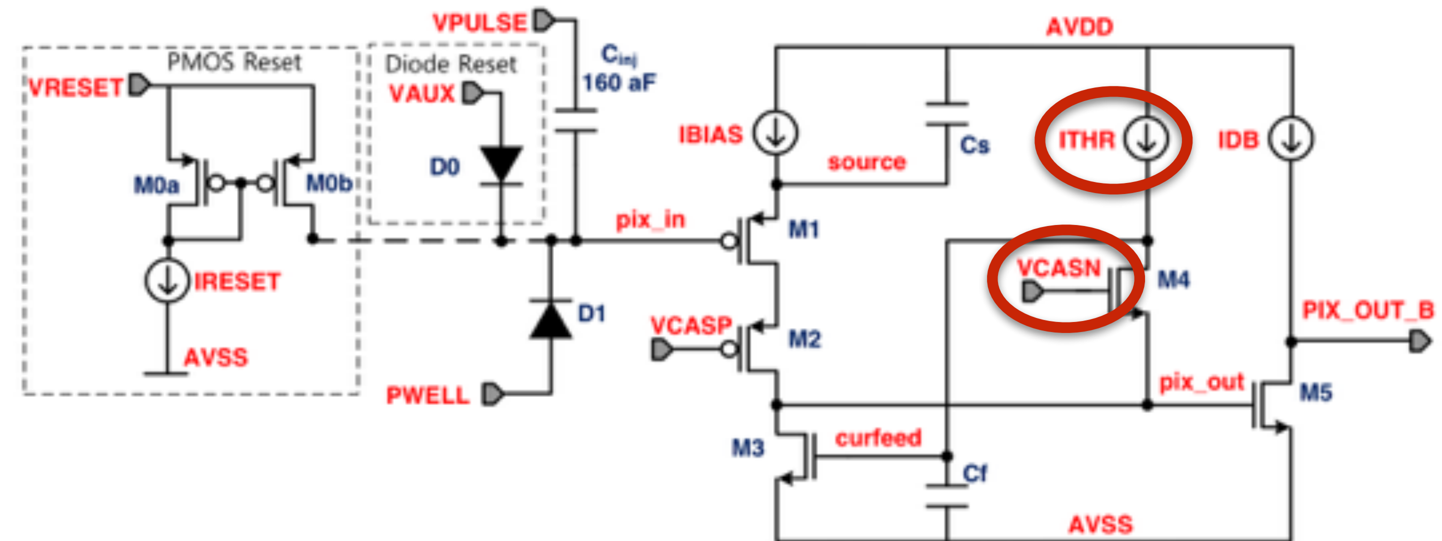
chip
fs1-39
fs2-20
fs6-17
fs6-22
fs8-29
fs9-20
fs9-21

1
2
3
4
Sector

Characterization test

- **Test setting**

Chip ID	fs-2-20
V_{BB}	No insert
ITH / VCASN	51 / 57



- **Determine threshold and noise by S-curve**

S-curve

Threshold map

Row

500
400
300
200
100
0

196 176 156 177

0 200 400 600 800 1000

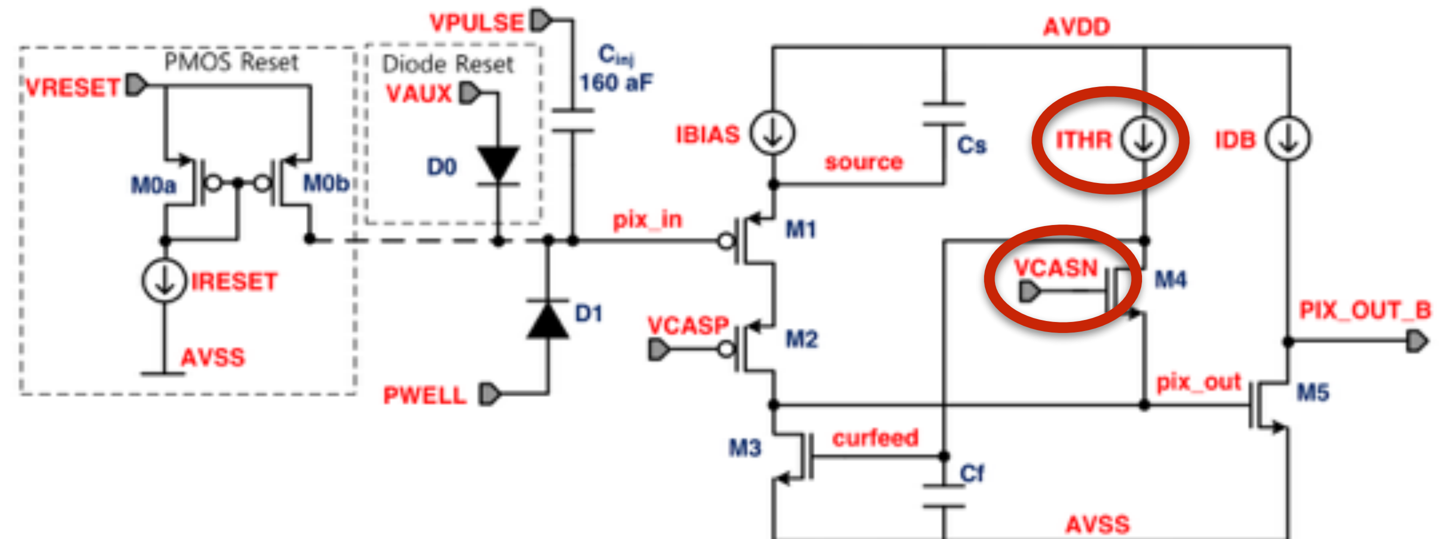
column

4000
3500
3000
2500
2000

Characterization test

- Test setting

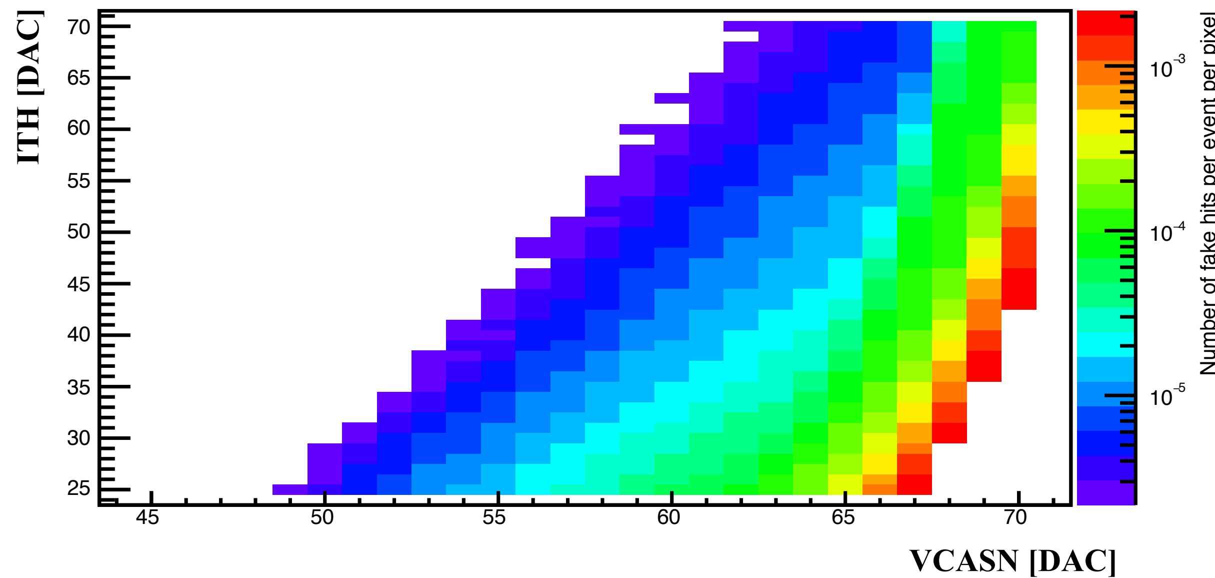
Chip ID	fs-2-20
V_{BB}	No insert
ITH / VCASN	51 / 57

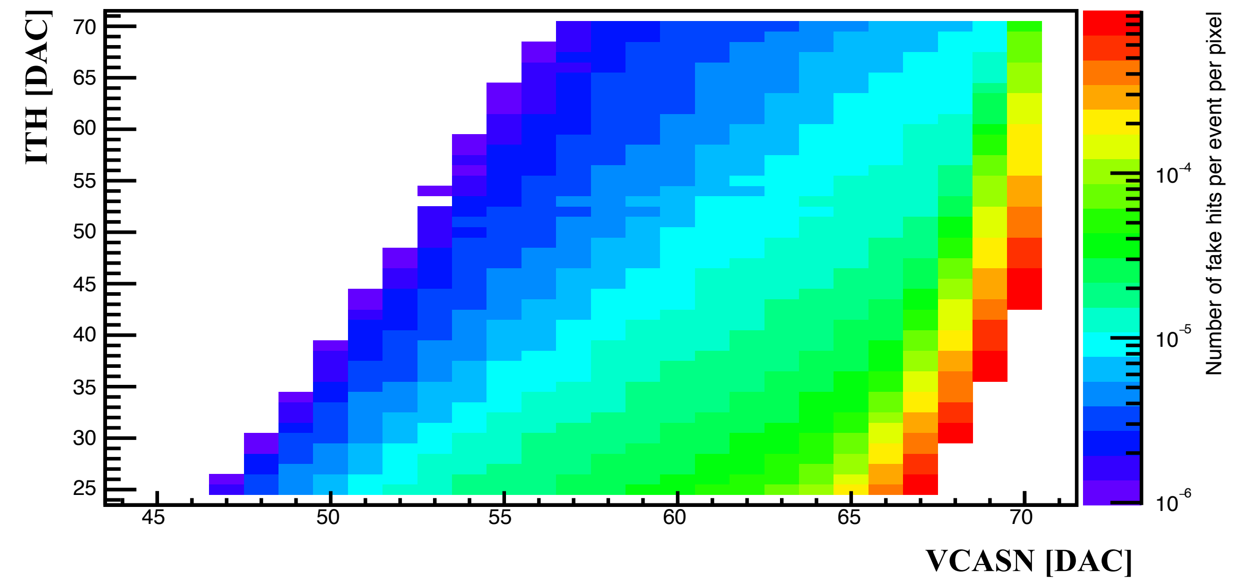


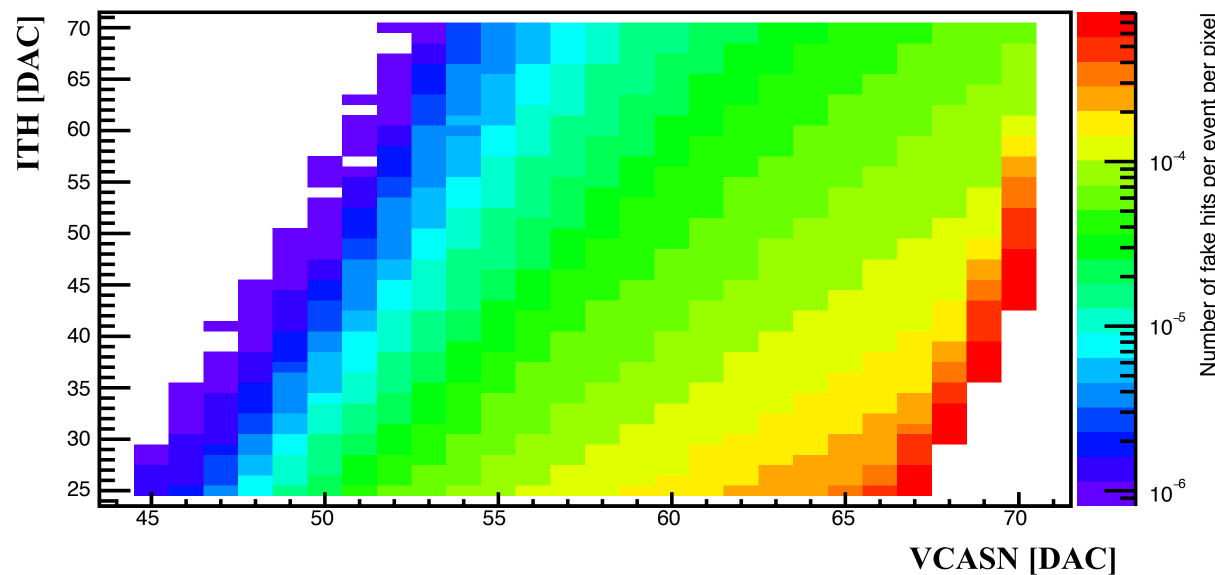
- Determine threshold and noise by S-curve

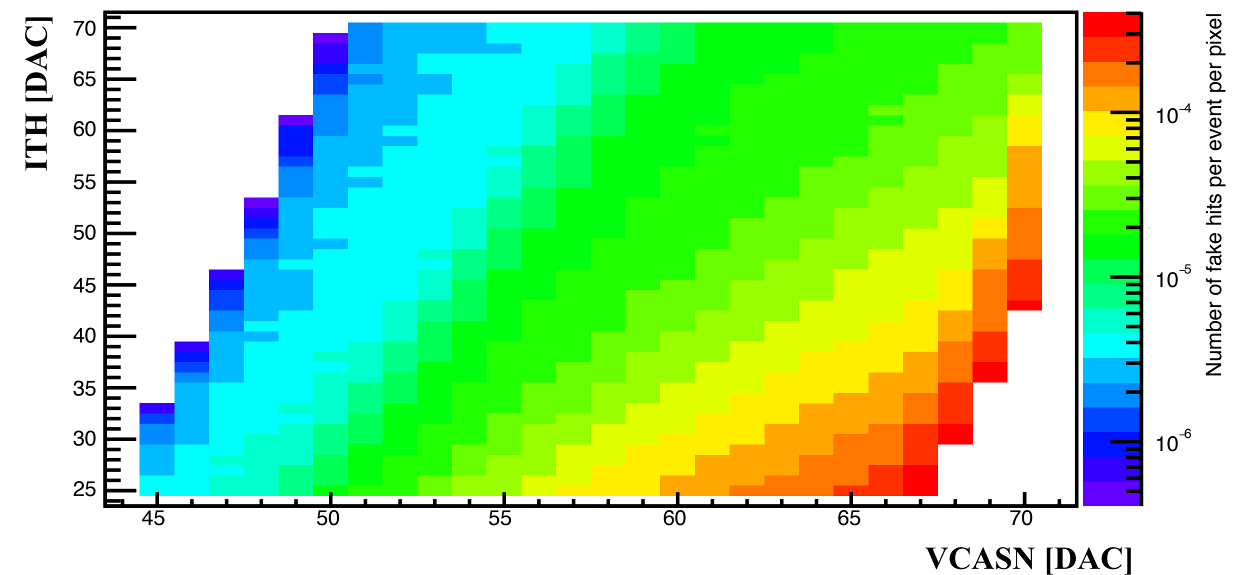
- **Noise occupancy scan**
  - ✳ **The charge threshold varies by two parameter : ITH / VCASN**

Noise occupancy without noise masking

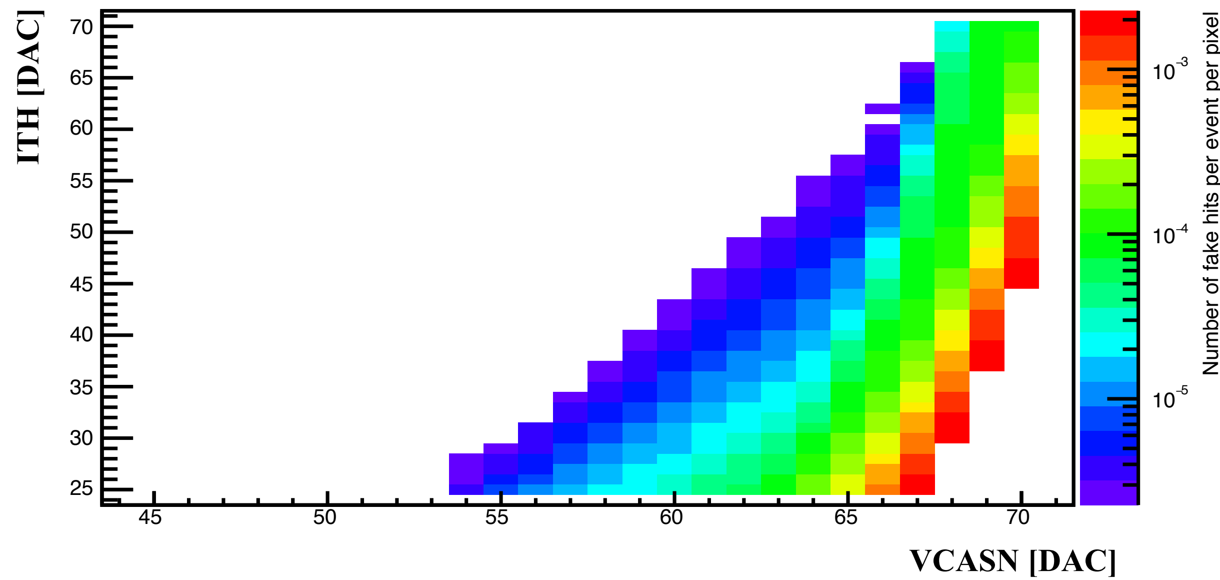


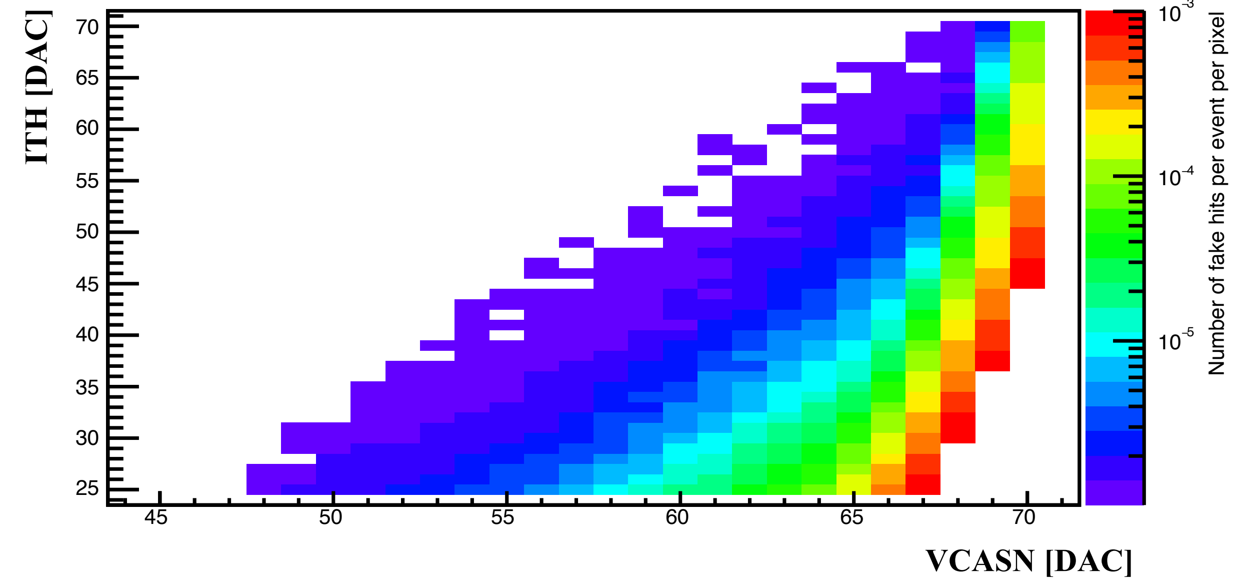


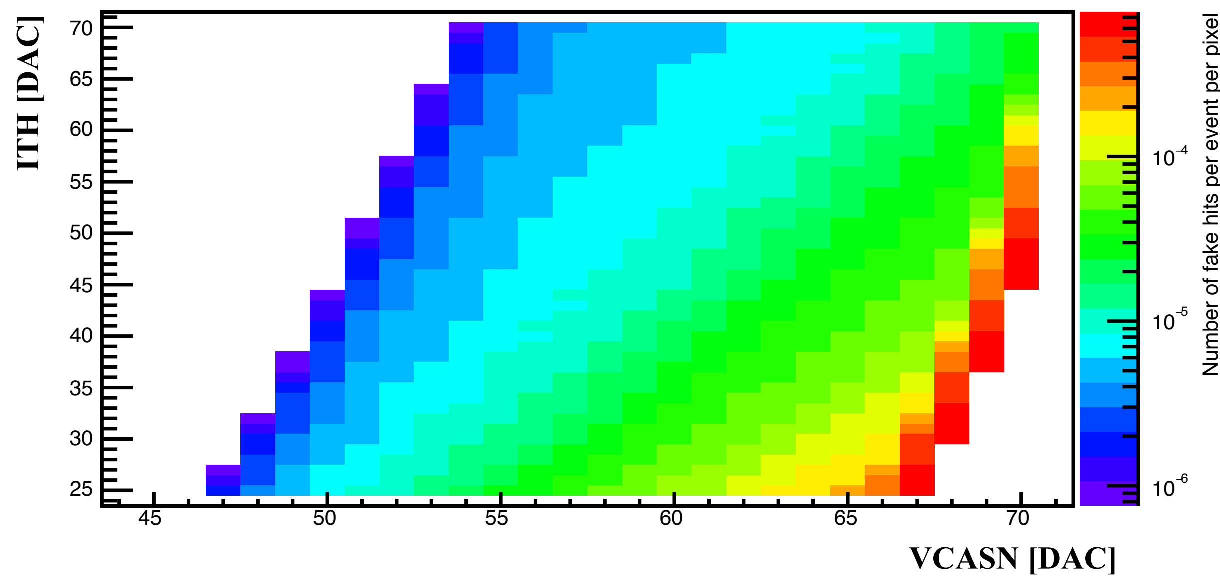


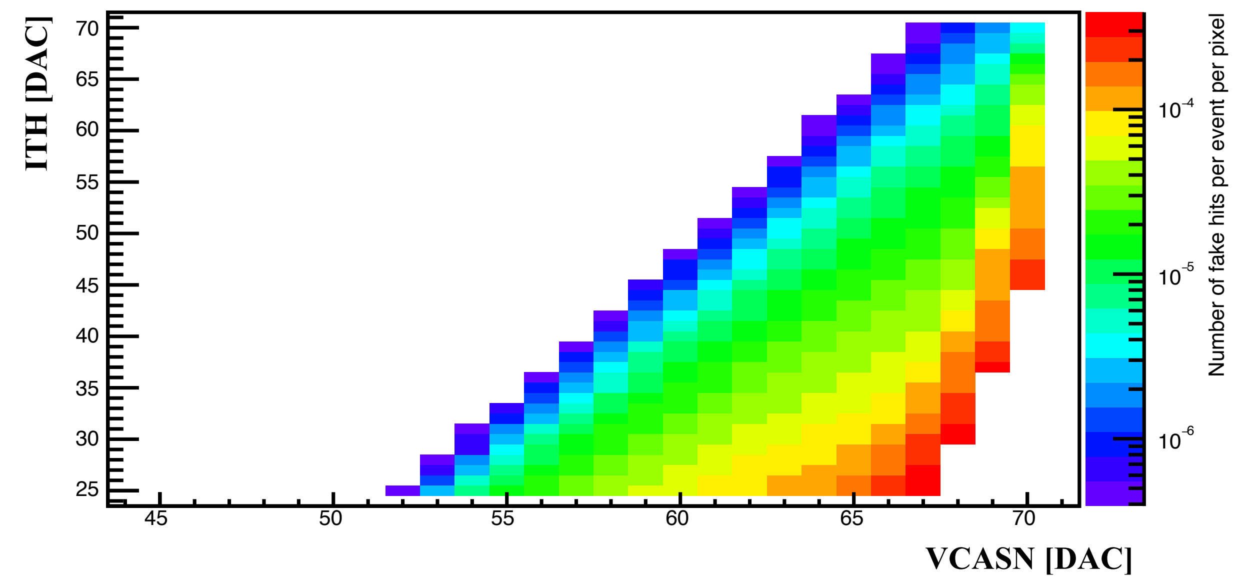


Noise occupancy with noise masking









Characterization test

- Test setting

Chip ID	fs-2-20
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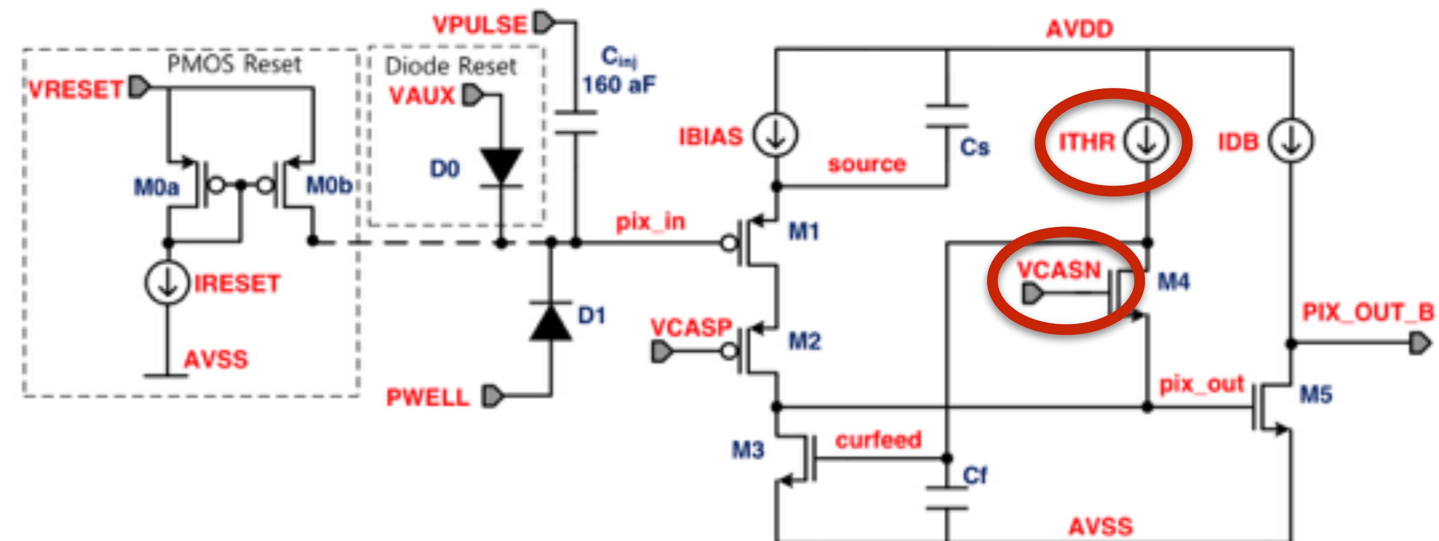
ITH / VCASN	51 / 57



- Determine threshold and noise by S-curve
- Noise occupancy scan
  - The charge threshold varies by two parameter : ITH / VCASN
- **Source scan**
  - **using ^{55}Fe source : around 6 keV**
  - **with noise masking**

Source scan

Hit map

Row 500 400 300 200 100 0

0 200 400 600 800 1000 column

250 200 150 100 50 0

Radiation circle

Source scan

Hit map

Row

500
400
300
200
100
0

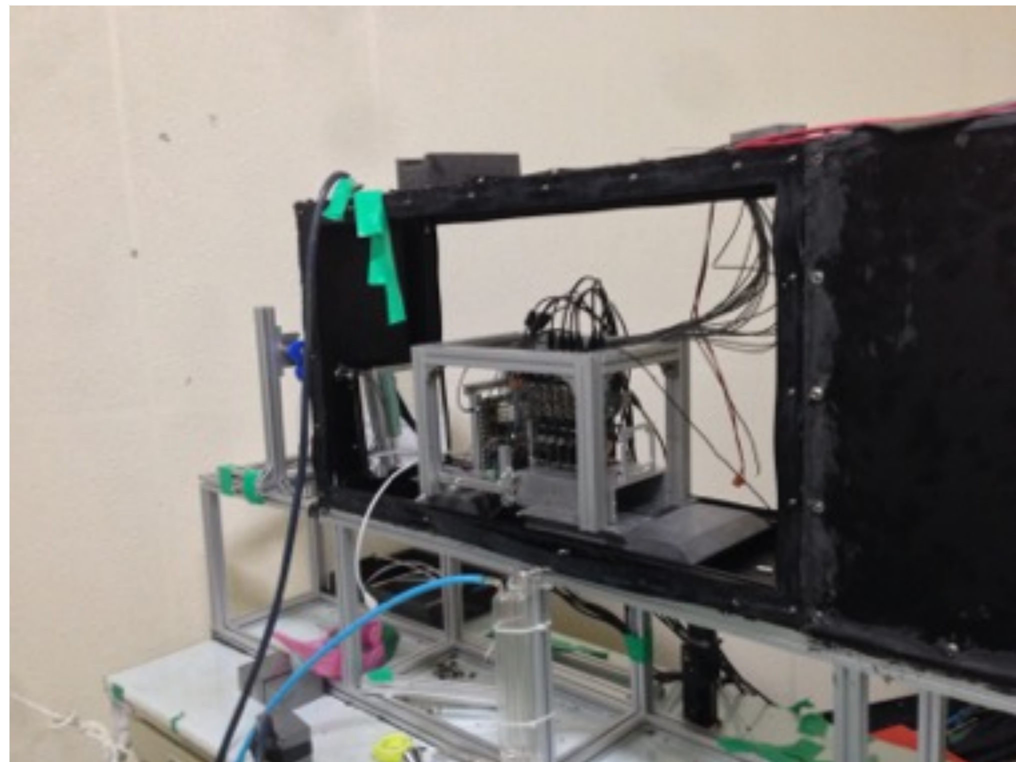
196
176
156
177

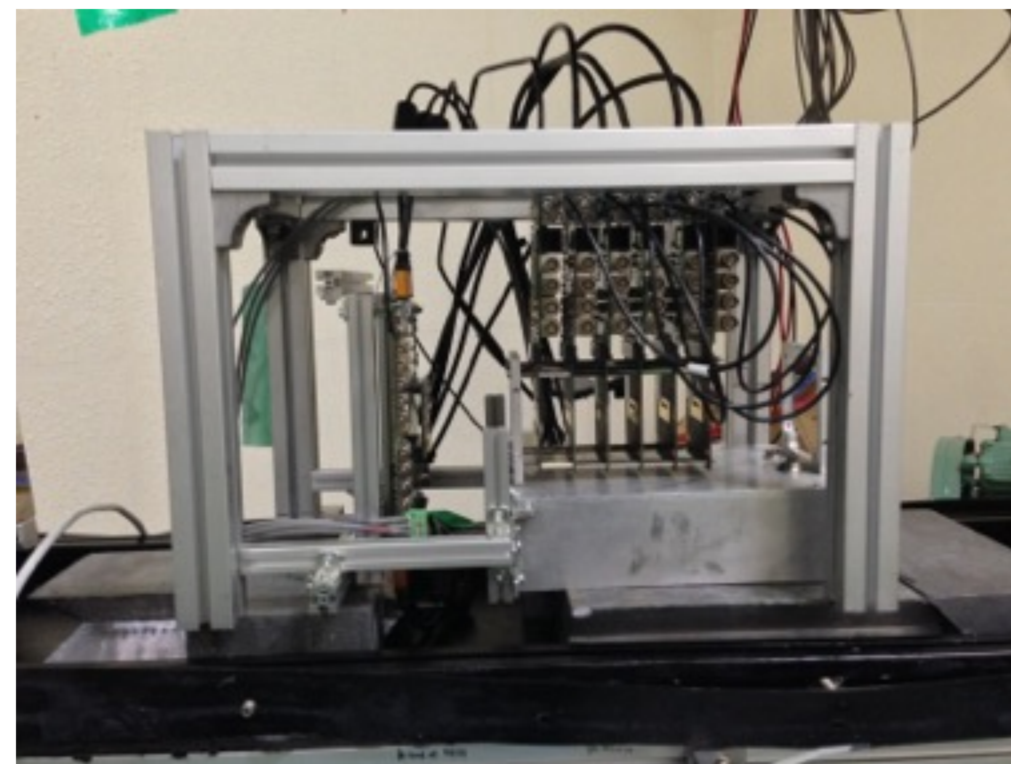
0
200
400
600
800
1000

column

160
140
120
100
80
60
40
20
0

Beam test





Summary & Outlook

- Primary lab test for 7 chips are done.
- Check the trend of threshold and noise following each sectors over all chips.
- Noise is decreased by masking.
- Check the chip response using ^{55}Fe.
- Participated the beam test at Pohang with PNU
- Todo list
  - Source test and analysis over all chips
  - Source scan analysis
  - V_{BB} (back-bias voltage) dependency

Thank you for your attention!

Back up