WP4:
Sensor Post Processing, Mass Test and Interconnection R&D

1. Wafer procurement and QA

Procurement

- Variety of custom epi wafers used in ITS1 and ITS3 run
- **Epi wafers for the production** → ramping up production of custom wafers could be i.O. of 6 months (tbc)

QA (measurements by TMEC) procedure

- Tests (destructive) to be done on an additional 10% of production wafers → 130 wafers
- Procedure will include 3 tests:
    - Surface resistivity measurement
    - SRP measurement of the epi layer
    - XSEM inspection of the cross-section cut, i.e. epi thickness

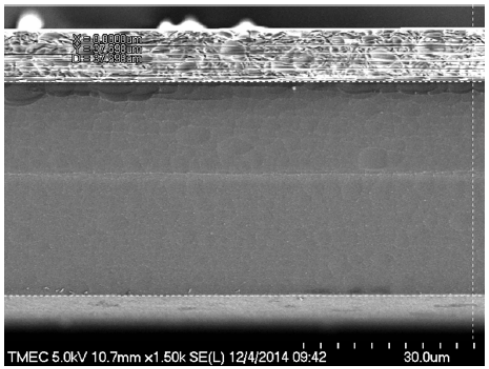
Example of QA done at TMEC

Prototype dies from ITS1 run (A1_CERN) with different starting material sent to TMEC forX SEM and SRP measurement: characterization of epi layer

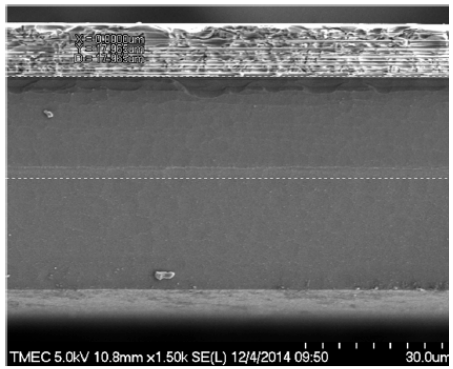
ITS1 dies : SRP & XSEM

2. W5: 18 um epi layer, >1kOhmcm, 50 um thick

XSEM : thickness



Wafer thickness : 37.69 um

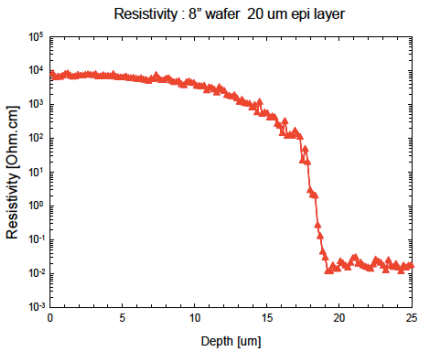


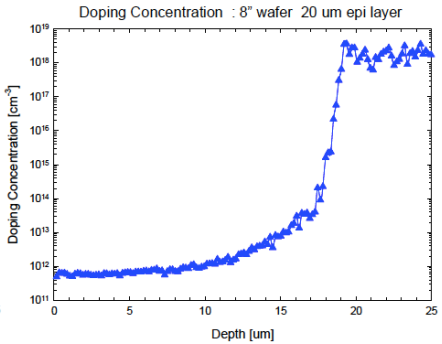
Epi layer thickness : 17.96 um

ITS1 dies : SRP & XSEM

1. 8" wafer : 20 um epi layer , average epi resistivity 6.284 kohm.cm

SRP : depth profiler





Epi layer thickness ≈ 19 um

See presentation by Jirawat!

2. Wafer post processing

a. Plating

Ni/Au plating necessary for laser soldering to provide a wettable surface for the solder ball

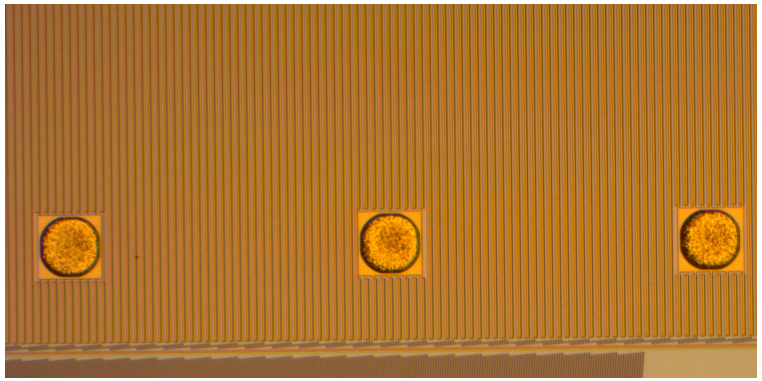
Chips with plated connection pads used from

- IZM (electro-plating)
- TMEC (ENIG)
- PacTech (ENIG)

Example of Ni-Au plating line

Process steps:

1. Passivation of all areas outside the contact pads
2. Ni deposition (typically 3-5 um)
3. Au deposition (~50-100 nm)



Ni/Au plated pads on pALPIDEfs

Process for market survey started (Invitation to Tender IT-4067/PH/ALICE); first draft of documents;

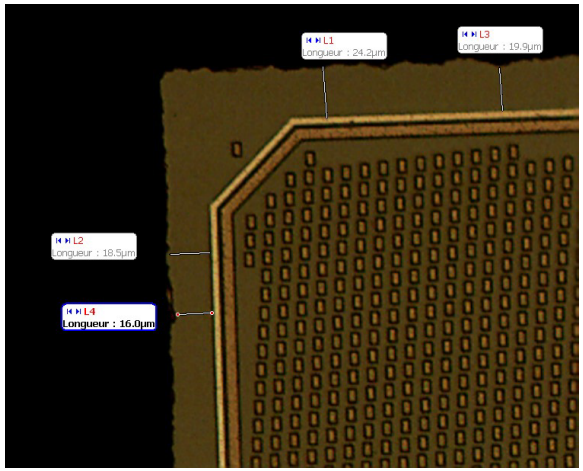
2. Wafer post processing

b. Thinning and dicing

Thinning & Dicing

Definition of the criteria for thinning and dicing:

- Thickness: 50 um +/- 5 um
- Max. extent from sealring: +/- 30 um (is 20 um needed?)
- Other?



2. Wafer post processing

b. Thinning and dicing

Two dicing methods:

- Diamond wheel pre-dice before grind (DBG)
- Laser dicing after grinding

Rockwood: DBG
STARS: laser dicing

Main issue in both cases: die picking after dicing and grinding

A. DBG

Extensive experience now with DBG (CMOS wafers and pad wafers).

Changed to new dicing blade on the last wafer (ITS2) to study edge quality:

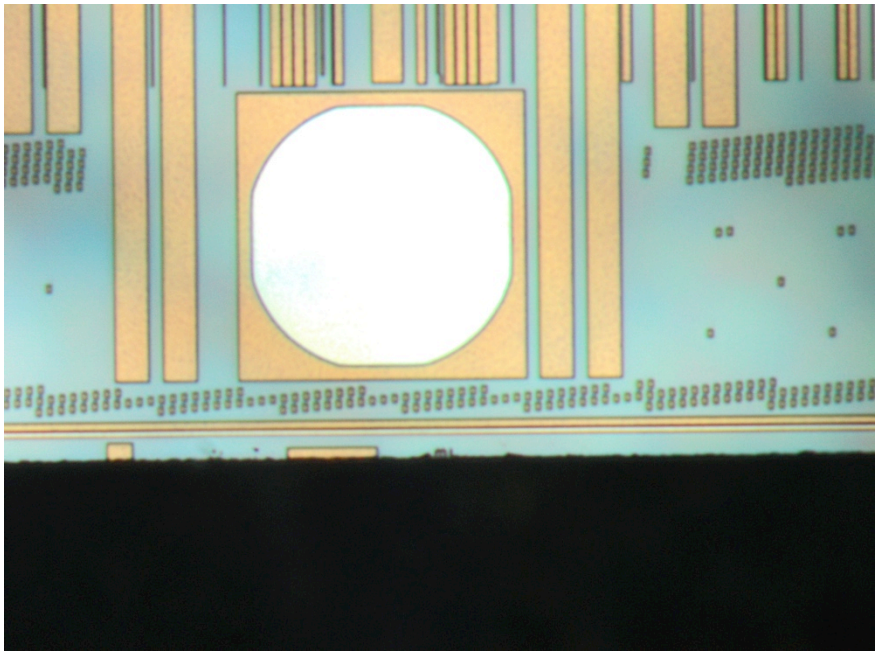
- Result is good on 3 sides out of 4, 4th side shows chipping (dense structure in the dicing lane)

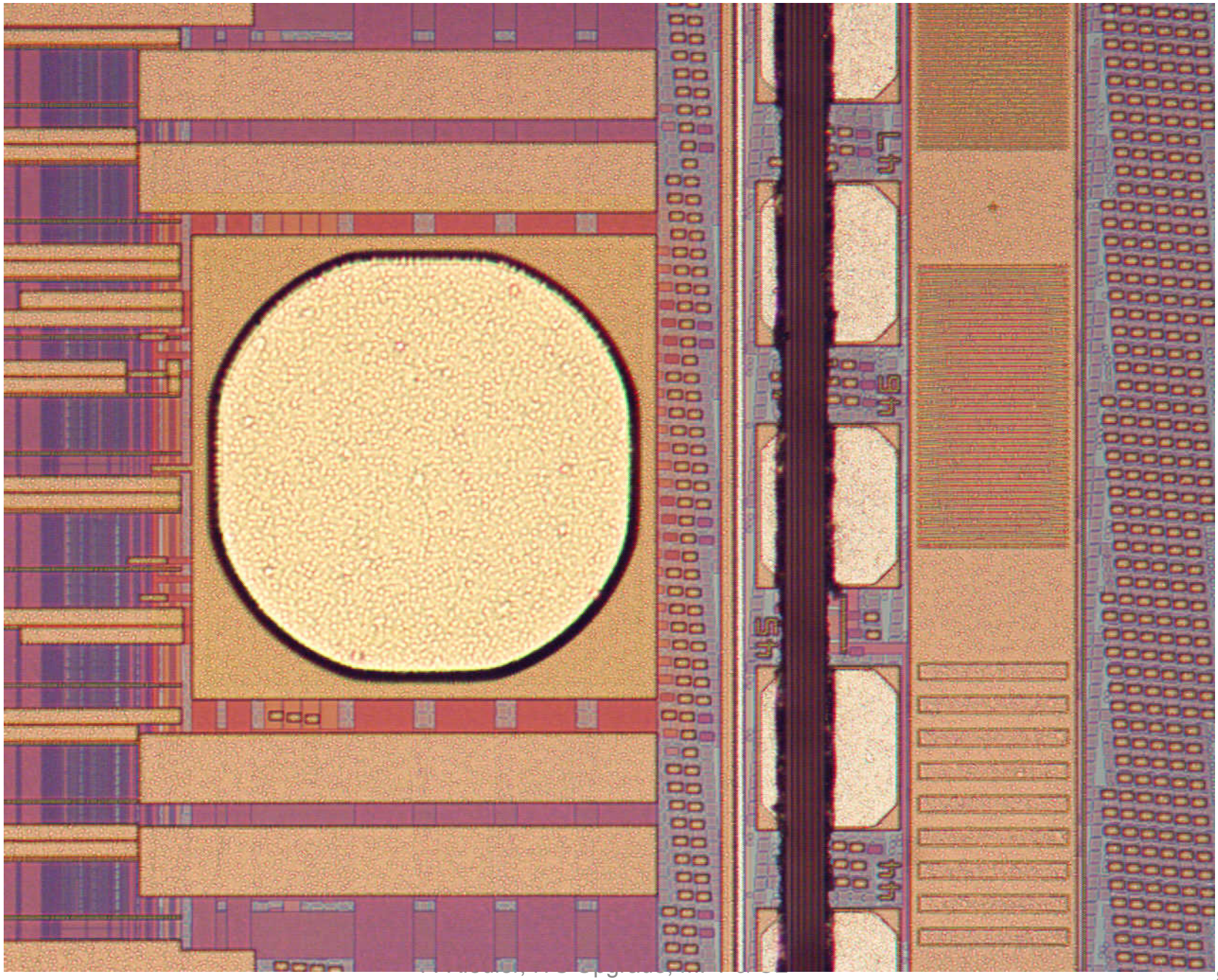
2. Wafer post processing

b. Thinning and dicing

Systematic investigation of dicing edge quality on chips from 14 wafers diced using DBG:

- Extension between sealring and physical edge contained between 15 and 25 um
- Tape whiskers
- Chipping and bent over metal/passivation in dense structure regions possible
- Overall quality good




Ddd
Lth
5th
5th
4th

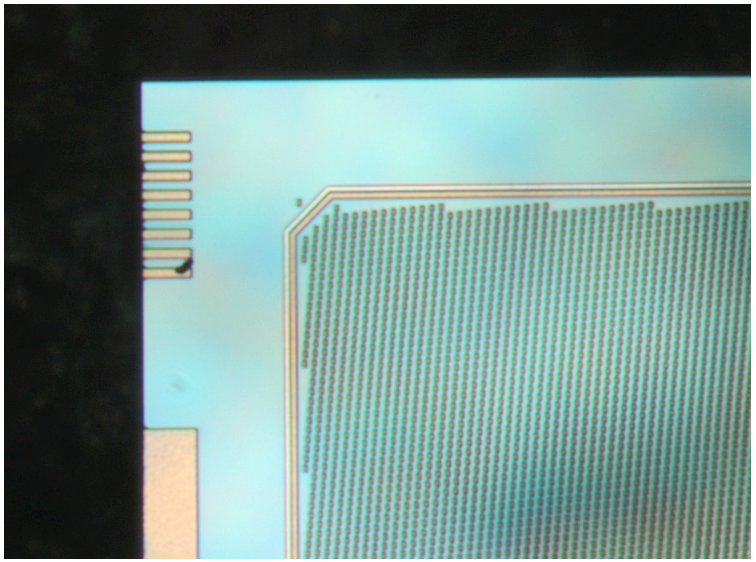
2. Wafer post processing

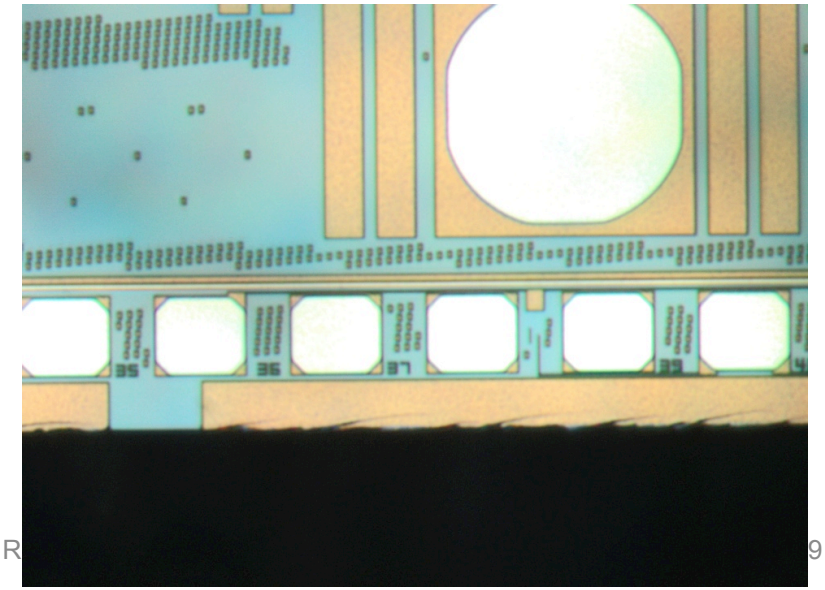
b. Thinning and dicing

Sent 3 ITS2 pad wafers (last metal layer+passivation) to STARS to test laser dicing using new pick-up tool

Die picking after thinning and dicing – two options:

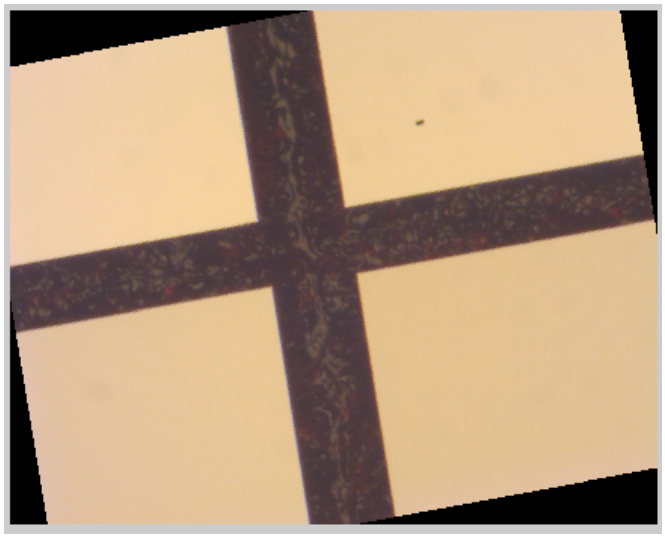
- specially developed die pick up tool (intended to do automatic die picking→4/26 dies picked
- Delamination and die picking fully manual → 51/52 picked

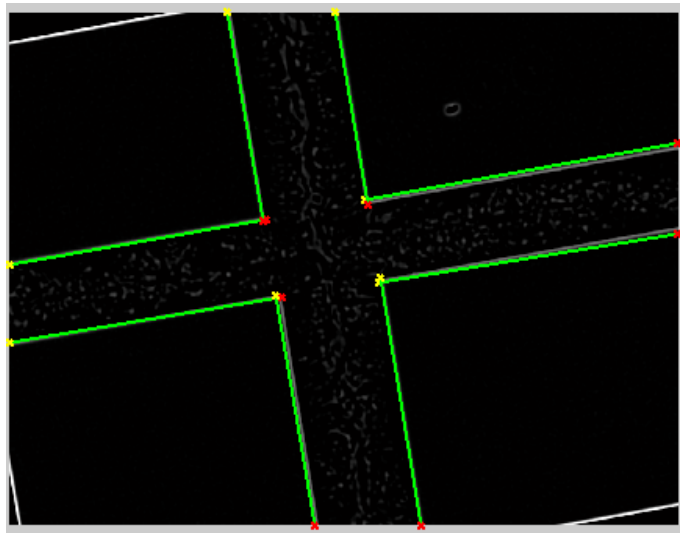




3. Visual Inspection - QA

- Work carried out by LIPI colleagues (Edi Kurniawan, Esa Prakasa, Adi Nurhadiyatna – see related presentations) – see dedicated presentations!
- **Chip spacing measurements using image analysis** and fits to lines using Hough transform
- More images to be analysed
- Geometrical dimension, edge defect detection?

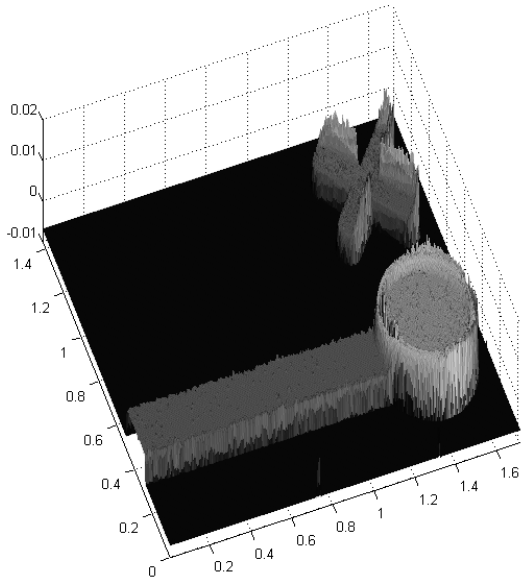


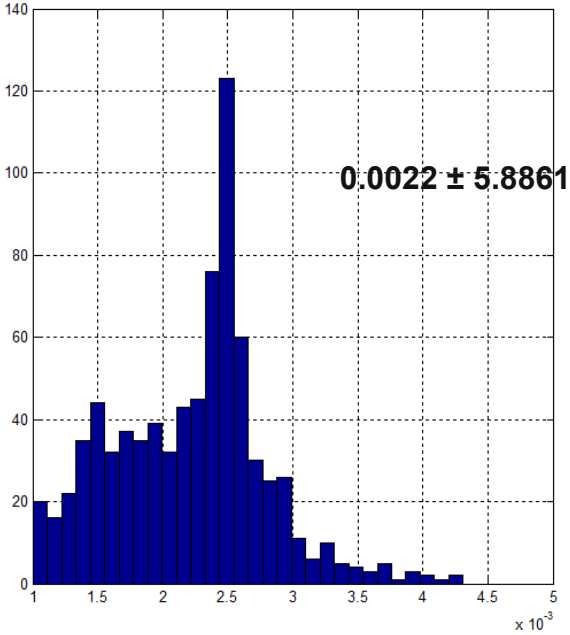


E. Kuniawan, WP4, 2.12.2014

3. Visual Inspection - QA

- Work carried out by LIPI colleagues (Edi Kurniawan, Esa Prakasa, Adi Nurhadiyatna – see related presentations) – see dedicated presentations!
- **3D microscope image of the chip surface**
- Pad dimensions, quality, surface defects,….



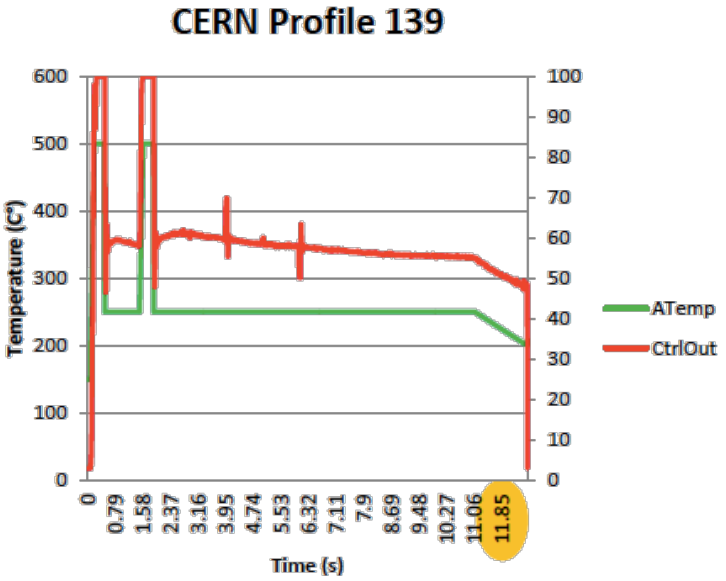


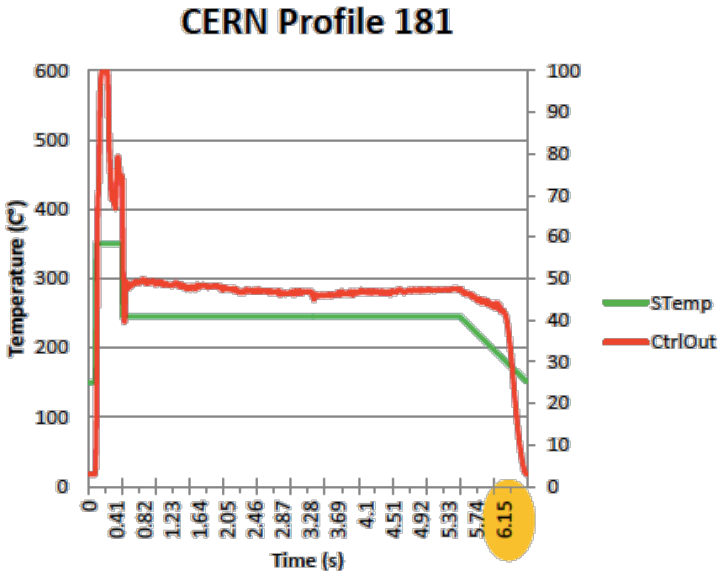
Thickness of pad edge:
$0.0022 \pm 5.8861\times10^{-4}$ mm = 2.2 ± 0.6 µm

E. Prakasa, WP4, 2.12.2014

4. Lasersoldering

- **Continuous progress in refining the parameters** (i.e. reduction of soldering time)
- Adaptation to different chips (pad chips vs. CMOS chips)
- Tests of FPCs from different suppliers
- Soldering of real pALPIDEfs chips
- Implementing process details, i.e. cleaning procedure of FPC





A. Junique, G. Fiorenza, P. Barberis

4. Lasersoldering

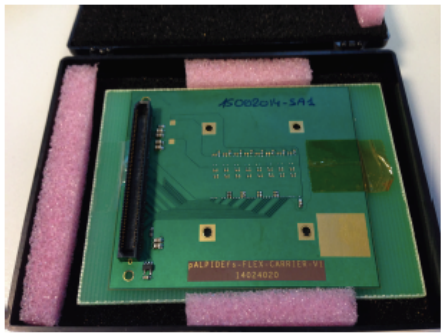
Intensive efforts to classify soldering contacts using and cross-correlating various methods:

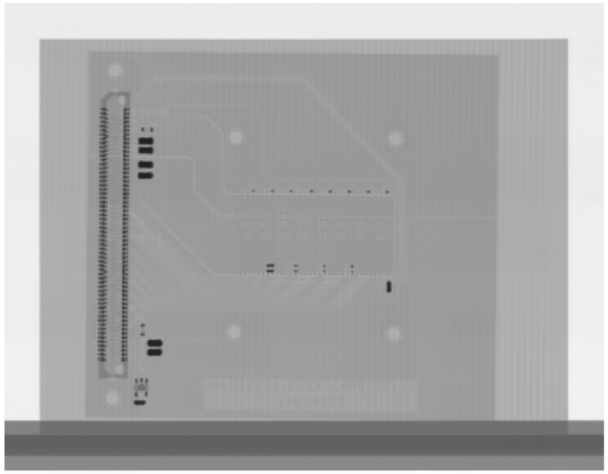
- Parameters registered during soldering process (integrated power, temperature, ..)
- Electrical test (daisy chain, functionality)
- Metallurgical cross section view
- Xray imaging

Goal: Define a classification scheme for soldering contacts based on non-destructive tests

→ See presentation by Bong-Hwi Lim (Pusan)

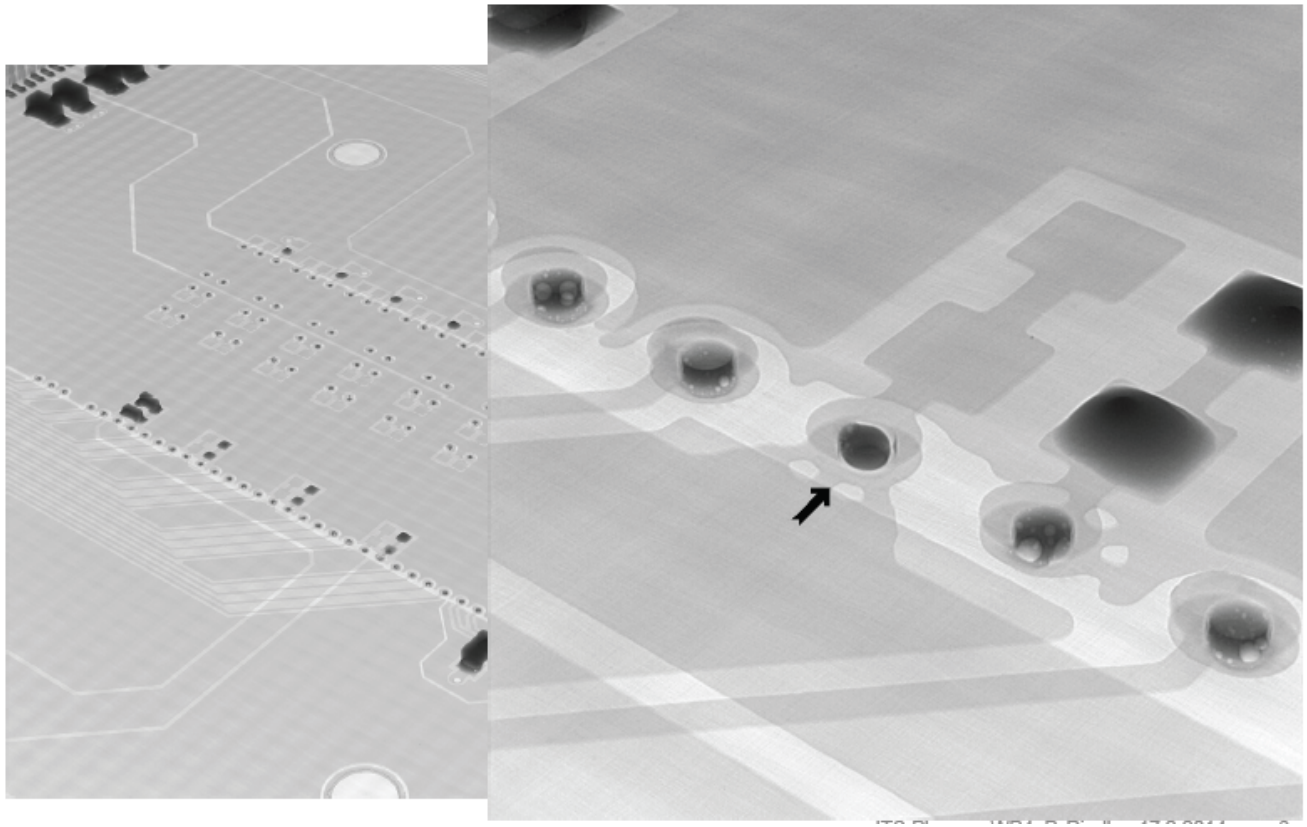
Implement this scheme as soon as possible and further refine it over the next months





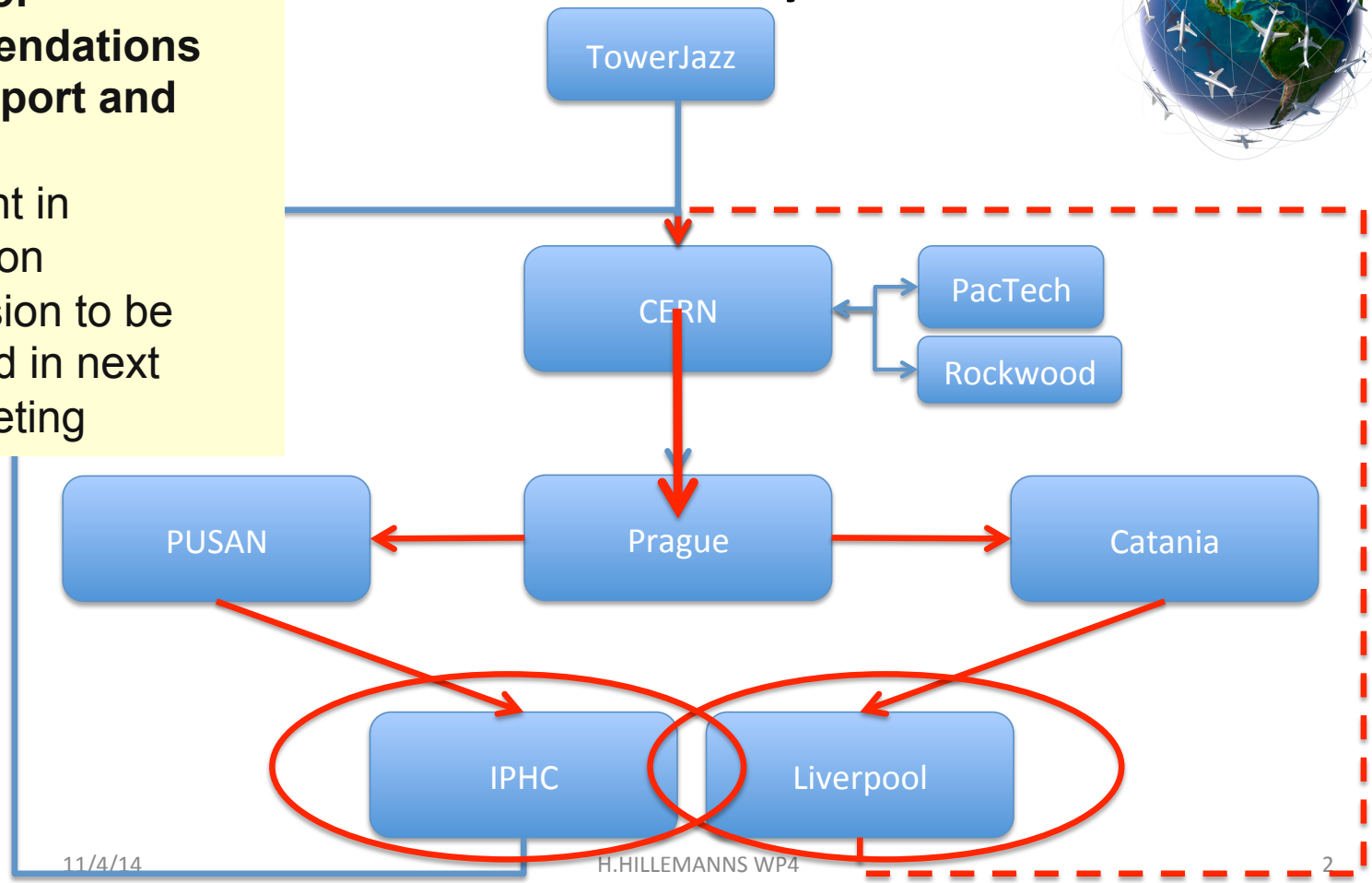
pALPIDEfs pad chip soldered on Cu FPC

2D X-ray analysis
(GE inspection)



5. Transport test

- **Developing protocol and list of recommendations for transport and storage.**
- Document in preparation
- First version to be discussed in next WP4 meeting



Summary

- Lots of progress in many different areas (please see dedicated presentations here and also in past WP4 meetings)
- Focus on “final” solutions in the next months
- Close interactions with the other work packages

- Next WP4 meeting will be on January 14, 2015!