High-speed link evaluation at CCNU

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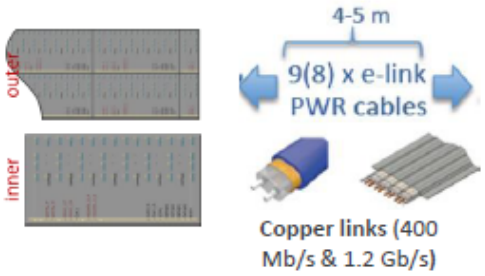
The readout Unit

WP10 – Readout electronics

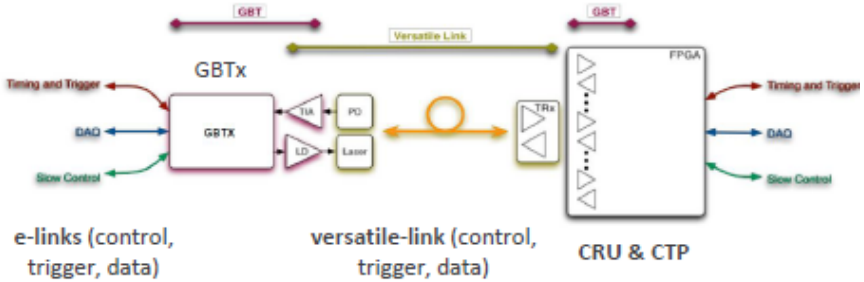
WORK IN PROGRESS

Readout electronics – links

- Up to the end of the copper links everything reasonably defined.
- The GBTx links number (intended as optical lane/GBTx equivalent) is reasonably identified.
- What we must decide, is what goes between copper and GBTx.



readout electronic



Copper links/data rate

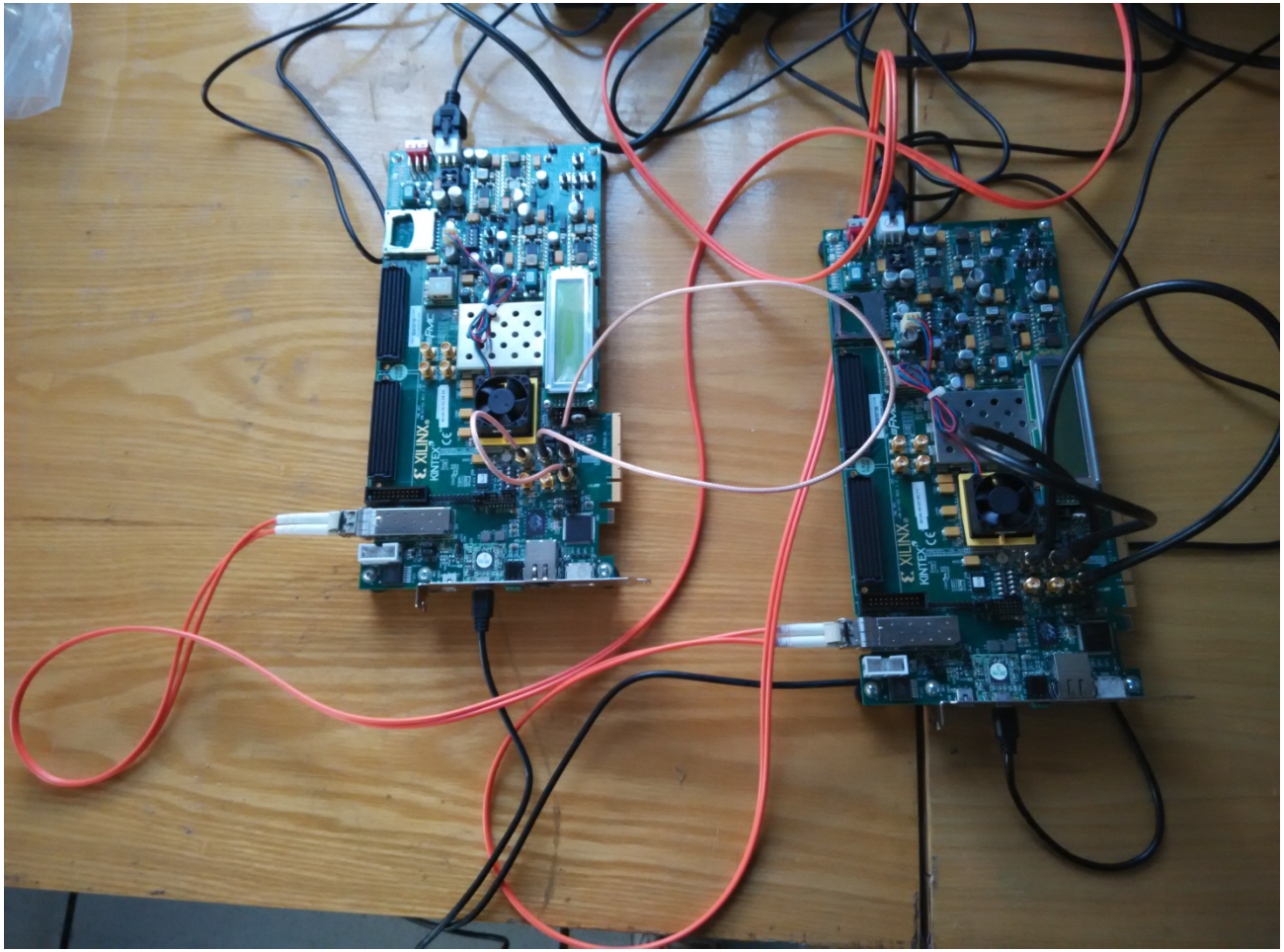
Layers	Staves count	Copper links	Data load per link
0-2	48	432	0.96 GB/s
3-4	54	864	0.32 GB/s
5-6	90	2520	0.32 GB/s
		3816	

SERDES lanes

FPGA 8 lanes	FPGA 16 lanes	GBTx upstream	GBTx chips
144	96	2.88 Gb/s	144
108	54	2.56 Gb/s	108
360	180	2.24 Gb/s	360
612 (86 kUSD)	330 (146 kUSD)		612 (---)

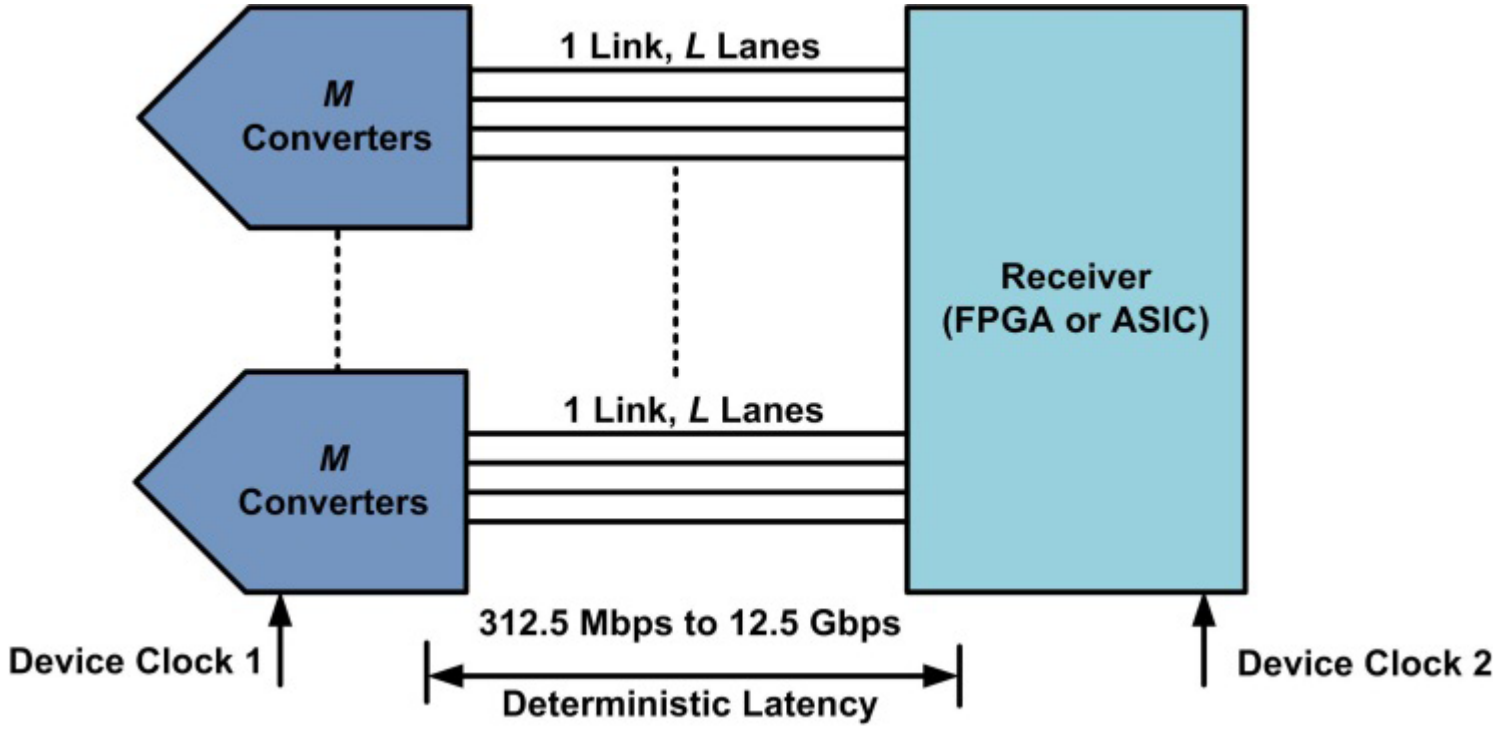
This page is from the ITS 2014 Planary talk

The GBT link evaluation based on Xilinx KC705 board



- The FPGA based GBT protocol is under evaluation between two KC705 board.
- The GTX port is used for evaluation
- It is under going!

The High Speed Jesd204b standard evaluation



- The high speed standard for connection between ADC/DAC and FPGA
- the highest link speed can reach up to 12.5Gbps per link
- Clock Data Recovery for high speed link
- 8b/10b encode and decode
- scrambling
- fix latency time alinement

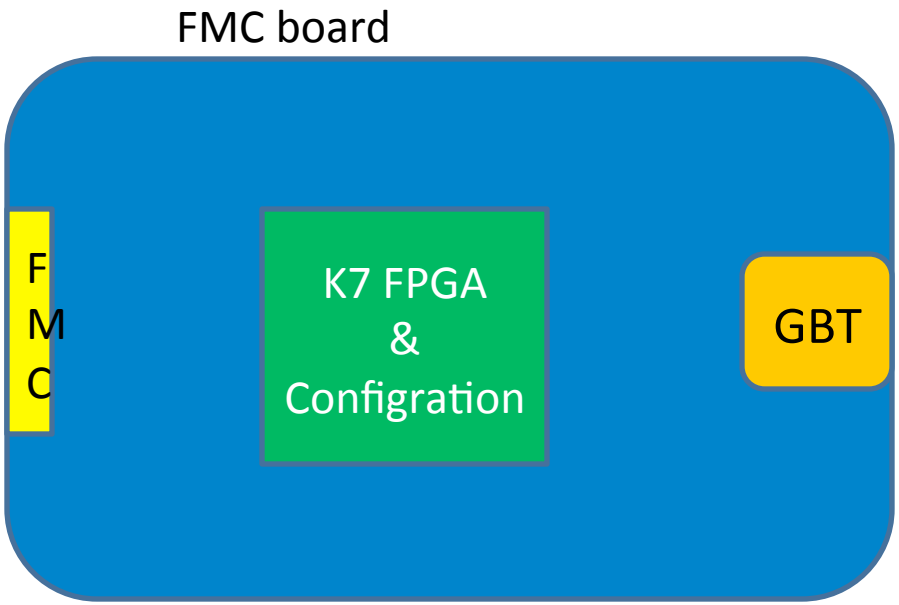
The High Speed Jesd204b standard evaluation

- ADC board: AD9656
- 4 channel
- 125Msps
- 16 bits resolution
- Using FMC-HPC for connection
- 10Gbps after 8b/10b encode need to be transferred
- 2 GTX links working on 5Gbps per link
- The firmware for ADC data taking is working!

PCB level High speed evaluation

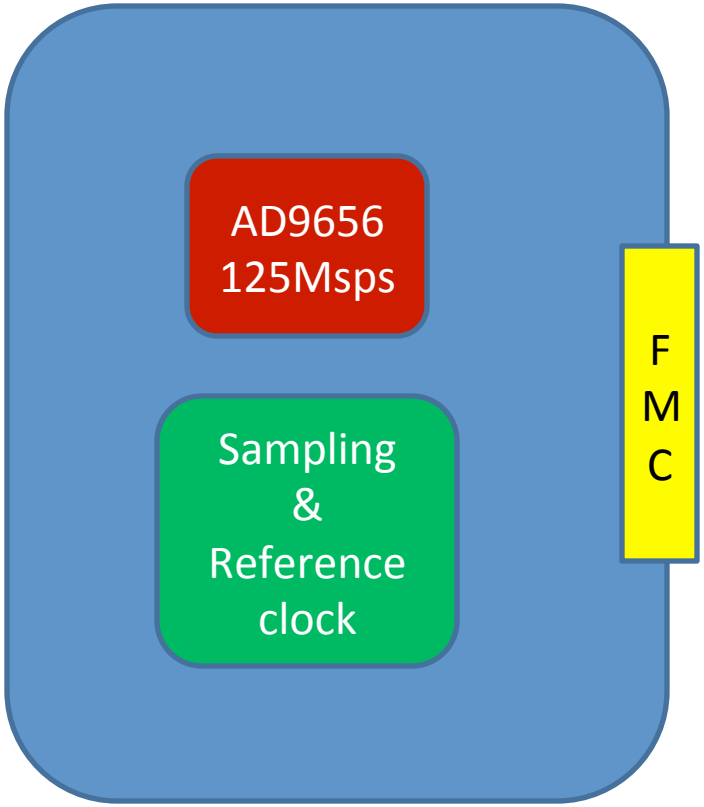
- An FMC loop back board has been made to test the parameter of the high-speed GTX link.
- The IBERT will be used to test the PCB layout performance.
- The standard KC705 board will be used.
- The layout of the loopback card has been down, and we will get the board soon.

An FMC board is under develop



- XC7K70T FPGA
- 1 FMC with 4 GTX port
- 1 SFP port based on GTX link for GBT evaluation
- The max speed of GTX port is 12.5Gbps
- The schematics has been down and PCB layout is undergoing..

AD9656 ADC-FMC board



- 2 AD9656
- 8 channel
- 125Msps, 16bit
- One sampling and reference clock
- 4 GTX links, 5Gbps per link
- FMC-HPC compatible
- Schematic is down
- PCB is ongoing..

Next Step

- Complete the GBT protocol evaluation.
- Complete the FMC high speed link board.
- GBTx chip evaluation?...
- elink chip evaluation?...