Activity II: ALICE ITS Readout Electronics
Serial Link Characterization

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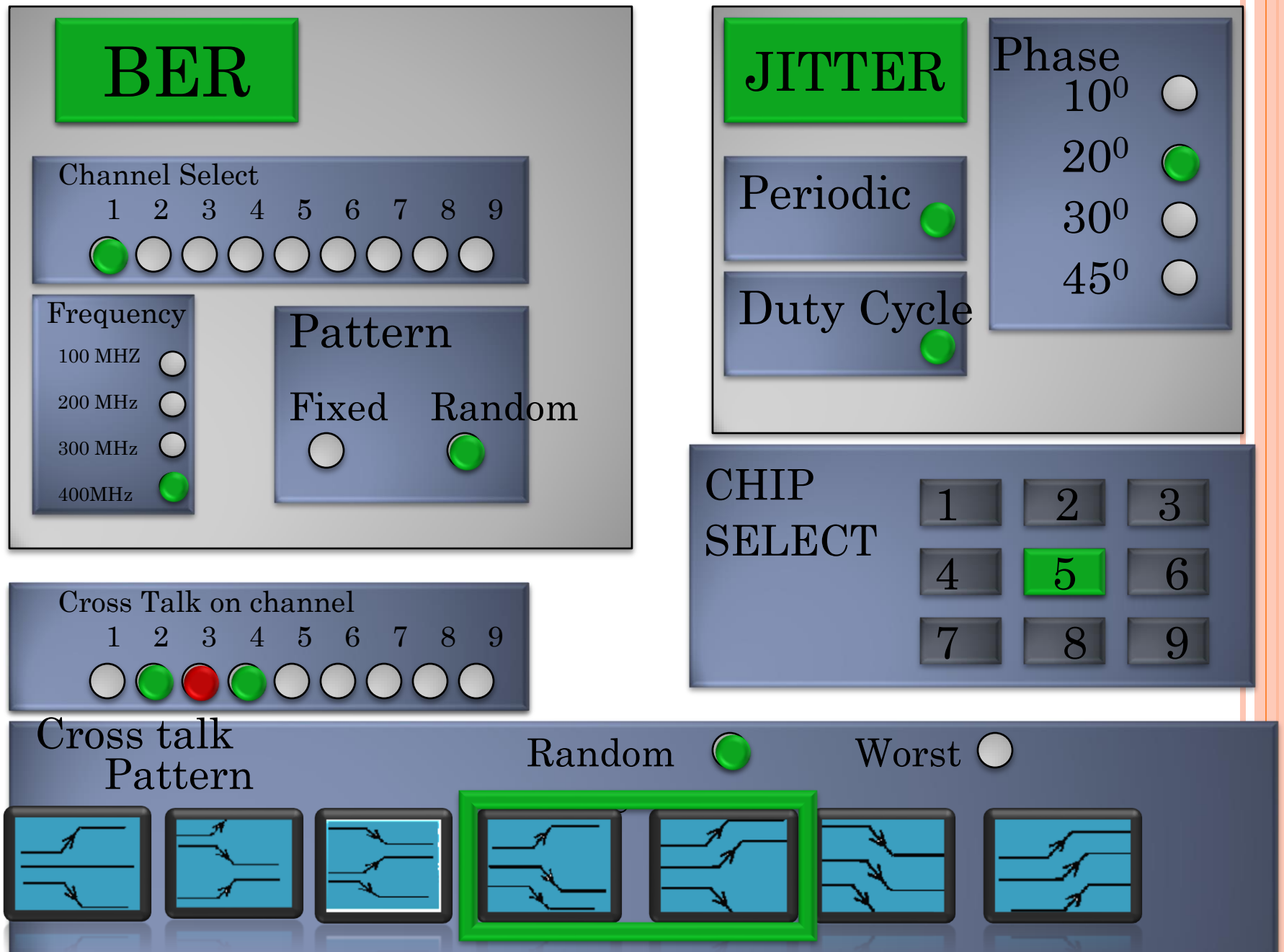
Tasks

- Firmware development for serial link characterization
  - GUI
  - BET
  - Crosstalk analysis
  - Jitter analysis
- Carrier board schematic and layout (possibly)
- Hardware testing

GUI Layout


BER
Channel Select
1 2 3 4 5 6 7 8 9
Frequency
100 MHZ
200 MHz
300 MHz
400MHz
Pattern
Fixed
Random
JITTER
Periodic
Duty Cycle
Phase
10^0
20^0
30^0
45^0
CHIP SELECT
1 2 3
4 5 6
7 8 9
Cross Talk on channel
1 2 3 4 5 6 7 8 9
Cross talk Pattern
Random
Worst

Design of a test set-up for the characterization of high speed ITS serial data links

Objectives

- Bit error rate evaluation at various data rates
- Cross talk analysis between data links
- Power analysis

Key Tasks

- Specification design of the test plan (can be seen in GUI)
- Schematic design of test board
- Firmware development

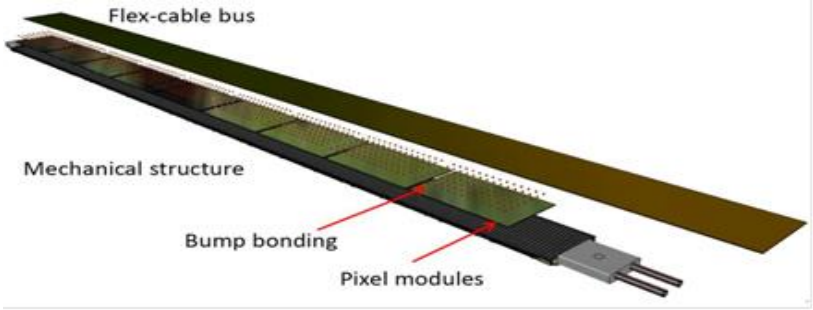
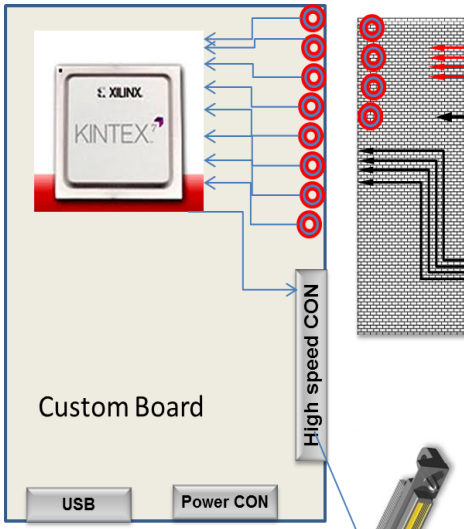
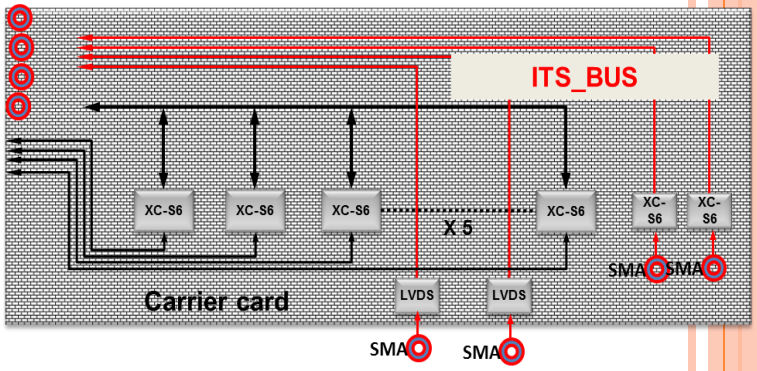


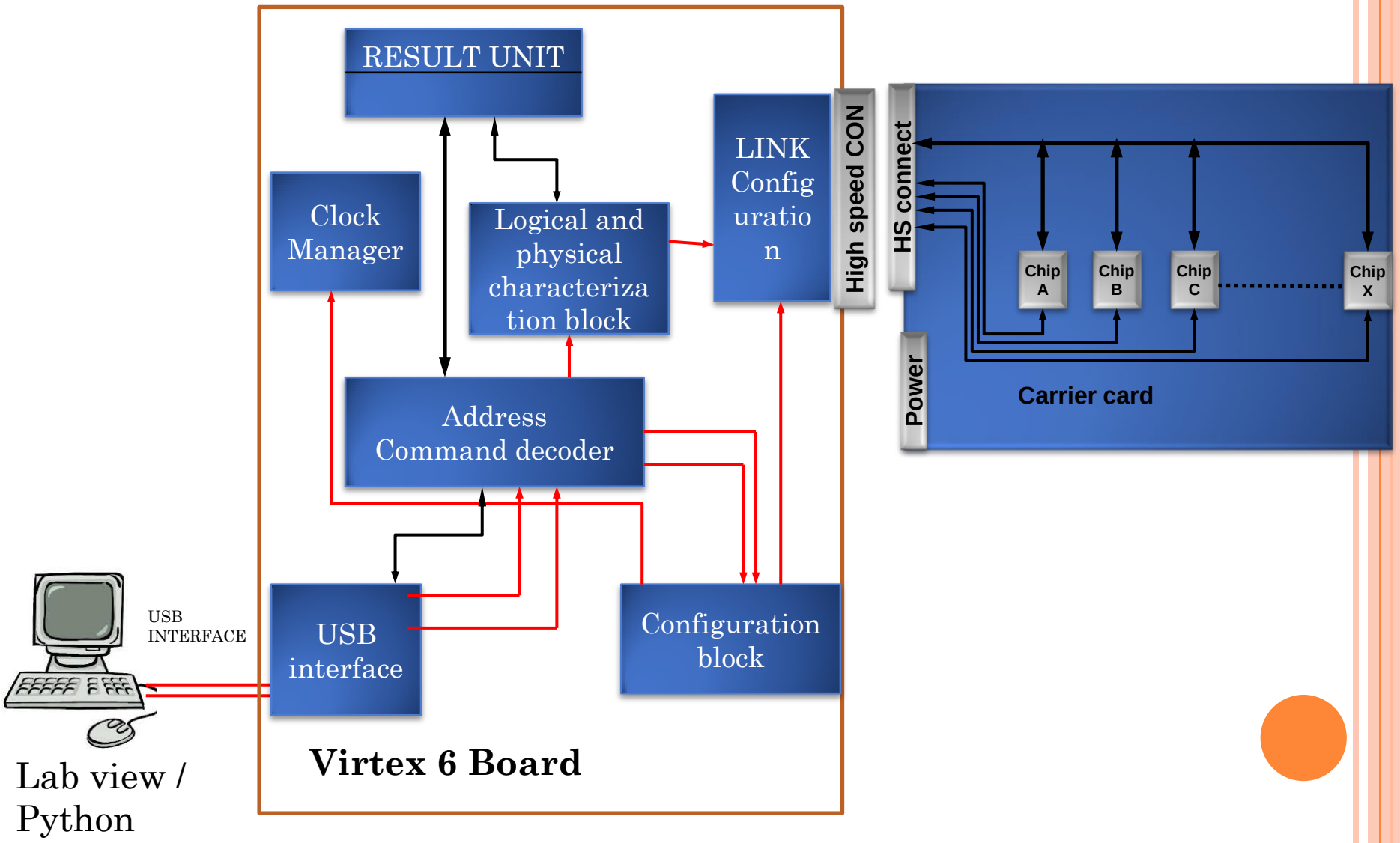
Figure 1: ITS Bus on Flex cable with 9 pixel





1) SMA connectors on test board to carrier card
2) SEMTEC connector/FMC connector to characterise data cables / loop back

Test Setup


RESULT UNIT
Clock Manager
Logical and physical characterization block
LINK Configuration
High speed CON
HS connect
Chip A
Chip B
Chip C
Chip X
Power
Carrier card
Address Command decoder
USB INTERFACE
USB interface
Configuration block
Virtex 6 Board
Lab view / Python

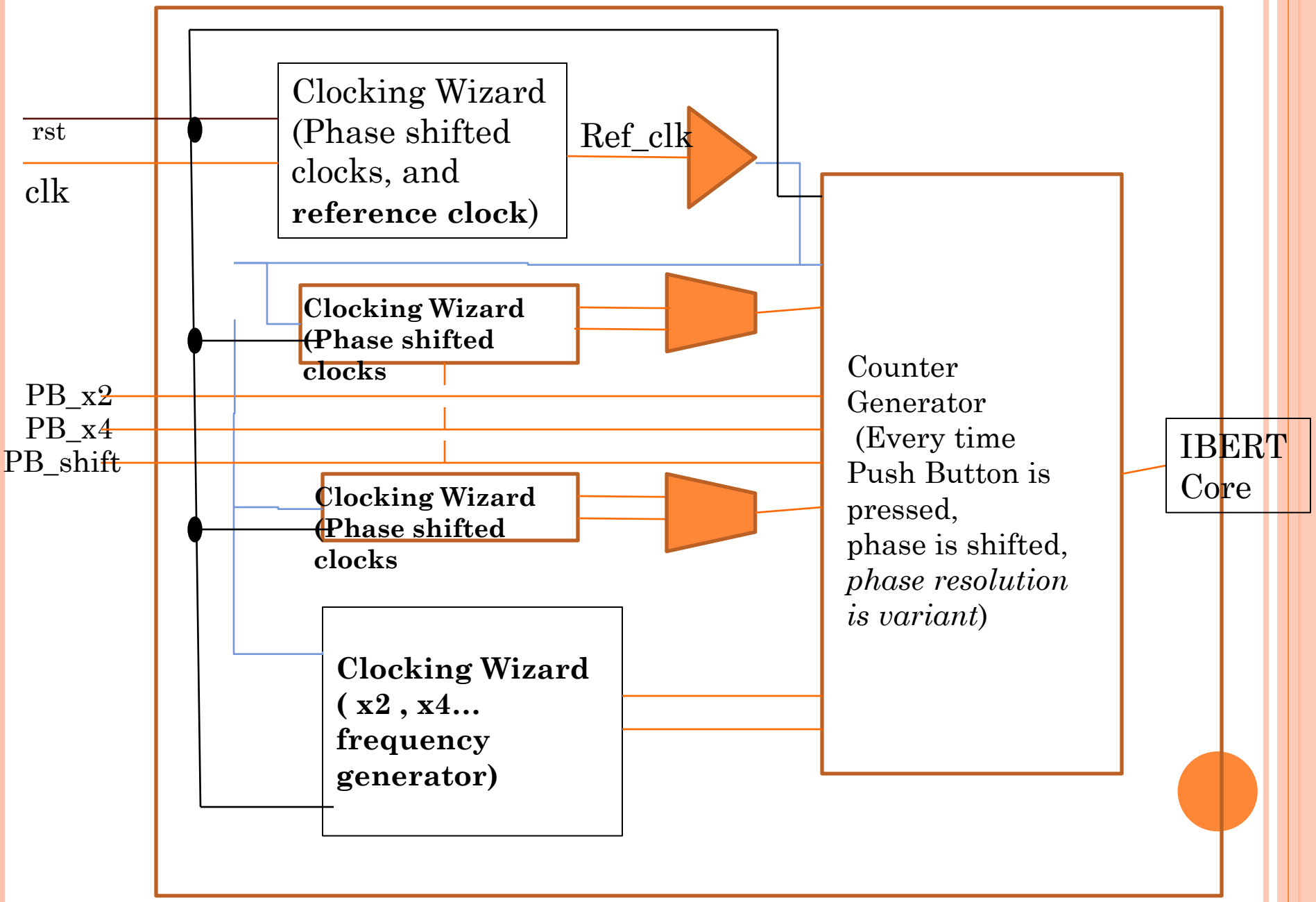
Bit error rate testing

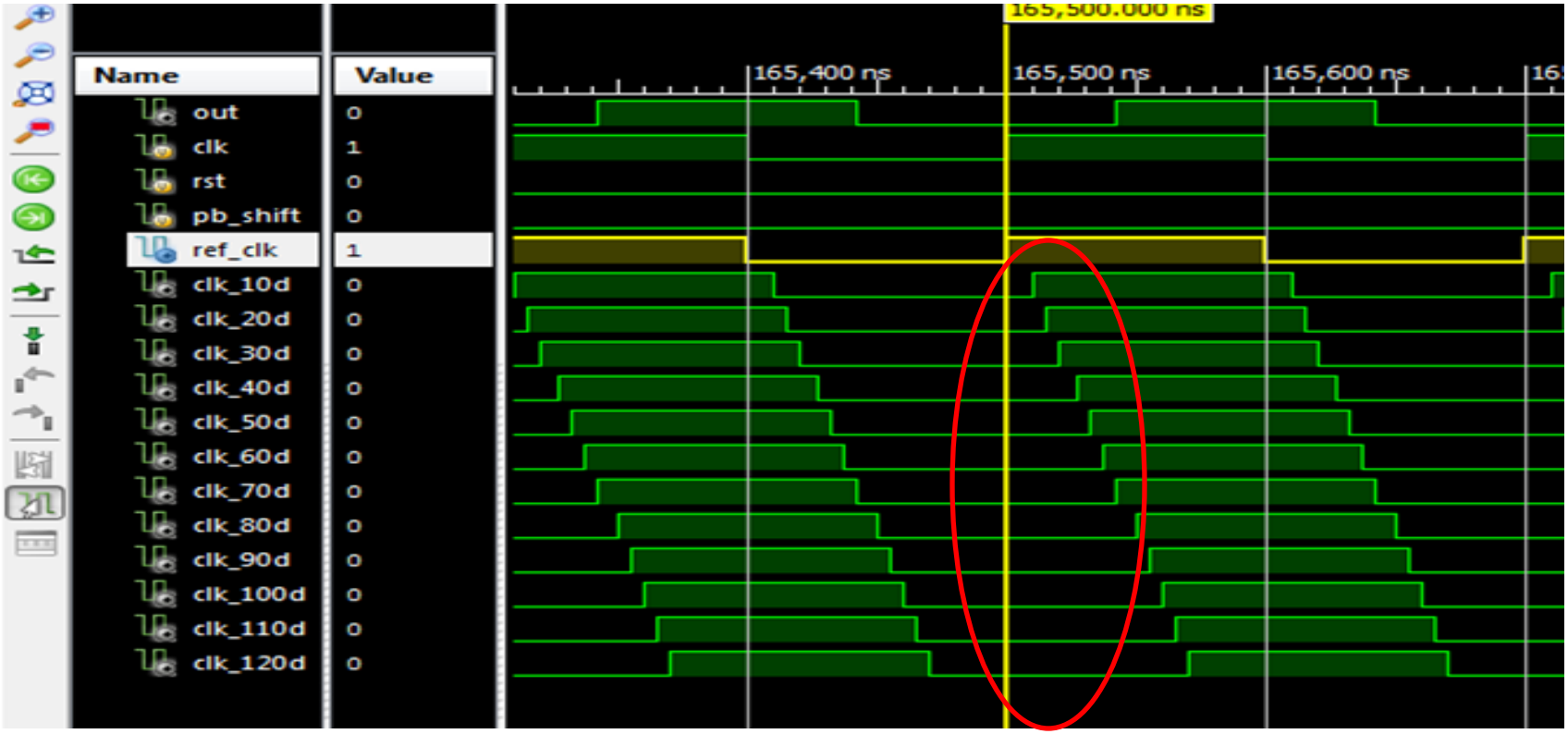
- **Generating clocks with different phases and frequencies to characterize BER.**

Using system clock as input, generating different shifts with as minimum resolution as possible.

Integrating shifted clocks to check BER

DATA FLOW DIAGRAM of Clock generation





• ref_clk is taken as input clk 50MHz upto 1GHz, rest are shifted clocks with different phase and frequency compared to ref_clk.

• shifted clocks with 50 MHz, have been generated. Each being shifted to 10^{O} (simulation, 9^{O} to 11^{O}actual) as compared to last shift.

• These clocks will now taken as input to check BER, at different phases and frequencies

Future work

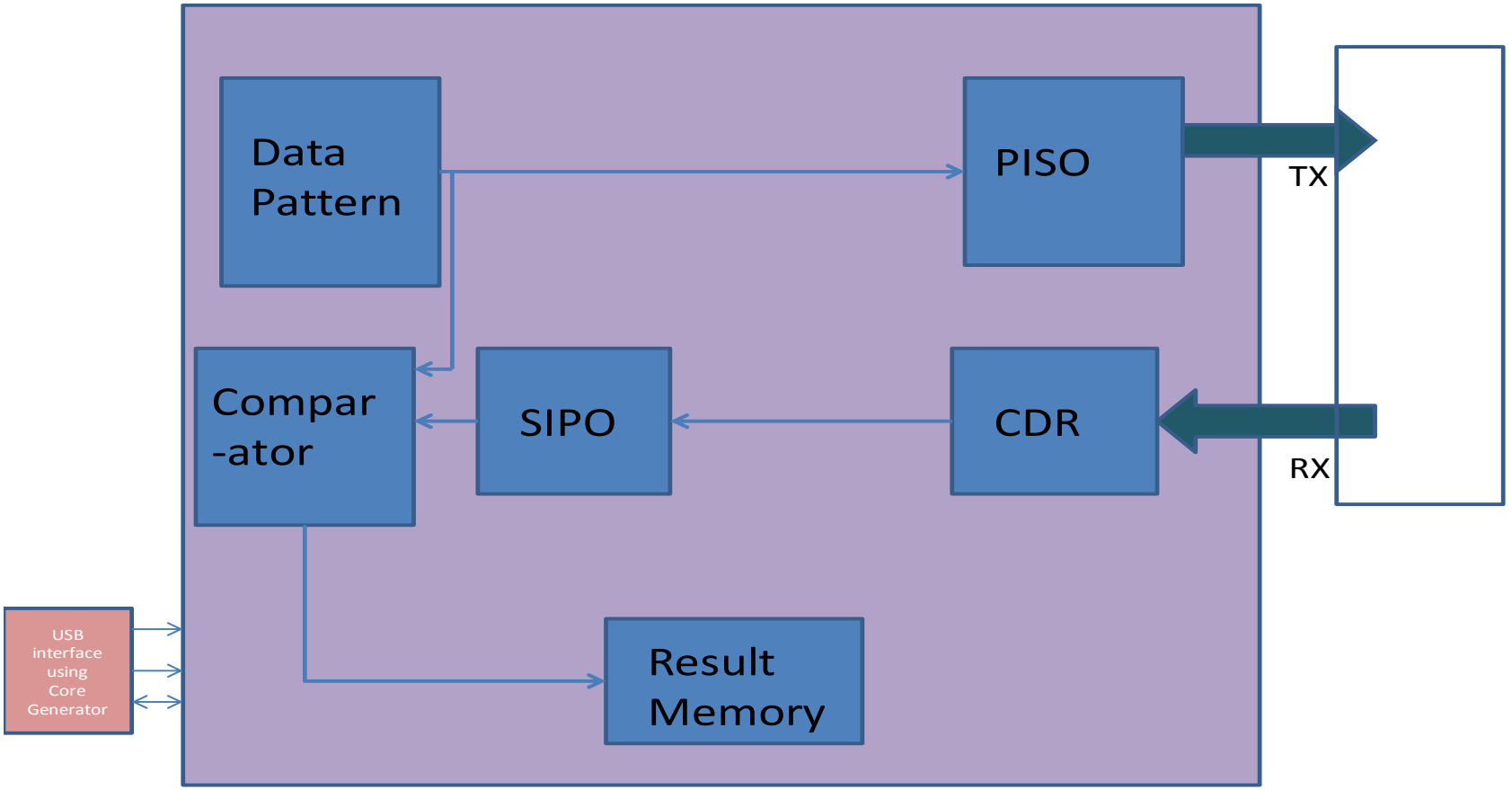
- Different data patterns are sent at different phases and frequencies.
- Jitter Analysis to be done on different clocks.
- To figure out at what phase and frequency, optimum results are achieved.

IBERT

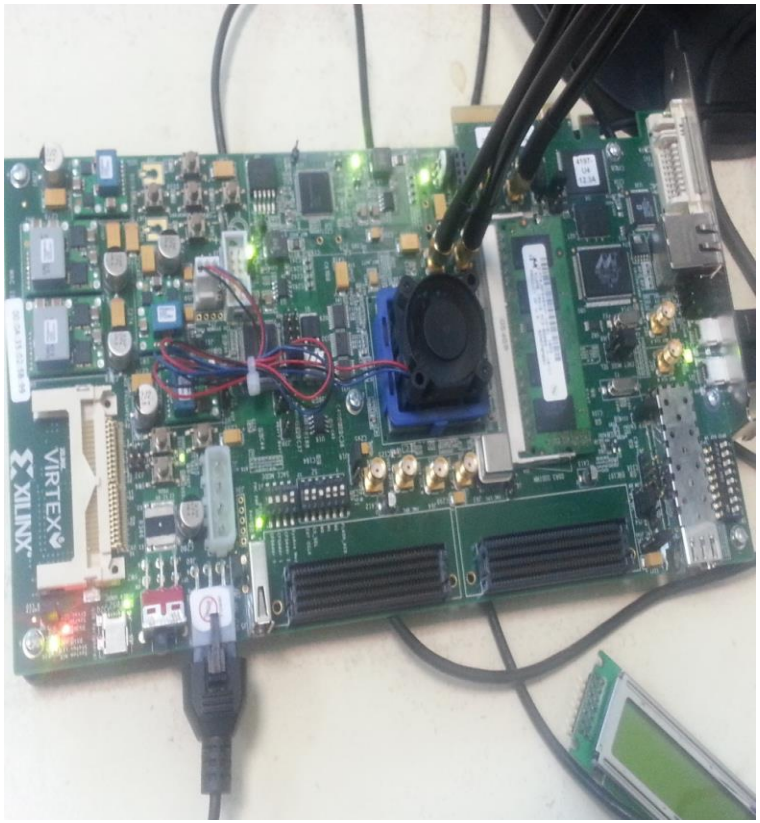
- The ChipScope™ Pro Integrated Bit Error Ratio Tester (IBERT) core for Virtex-6 GTX transceivers is a customizable core that can be used to evaluate and monitor the health of Virtex-6 GTX Transceivers.
- The design includes pattern generators and checkers implemented in FPGA logic, as well as access to the ports and dynamic reconfiguration port (DRP) attributes of the GTX transceivers.

- **Software Requirements**
  Core Generator
  Chip-scope Pro Analyzer
- **Hardware Requirements**
  Virtex-6, ML605
  SMA Cables

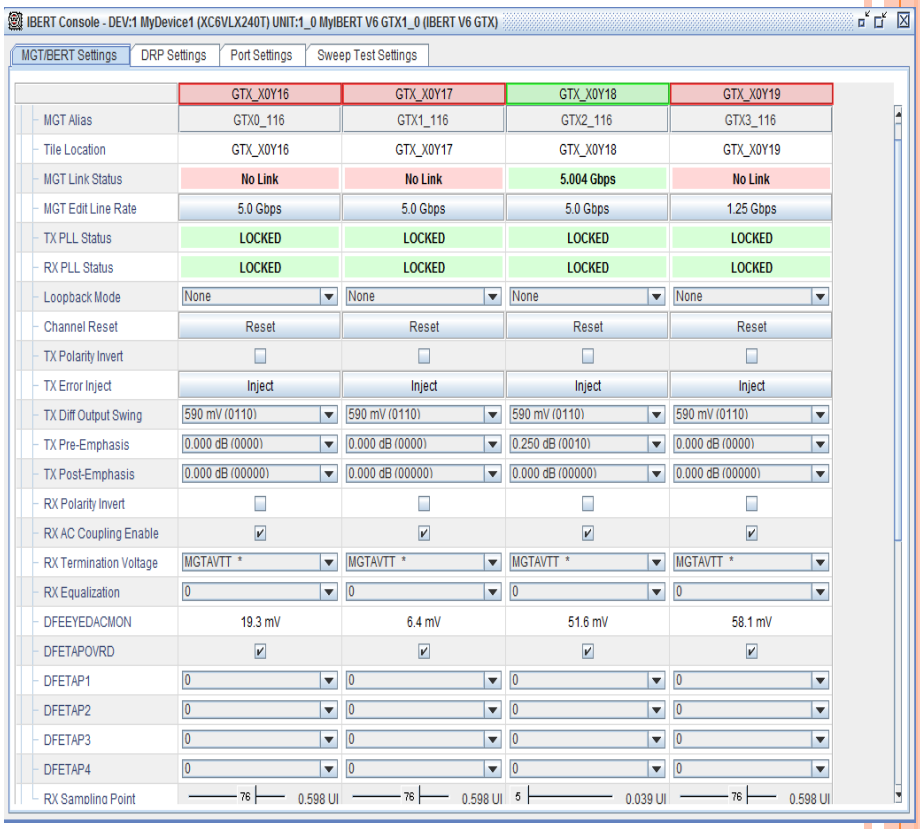
Design of Bit Error Rate Tester



Hardware Setup and Initial Settings & Results



Hardware setup

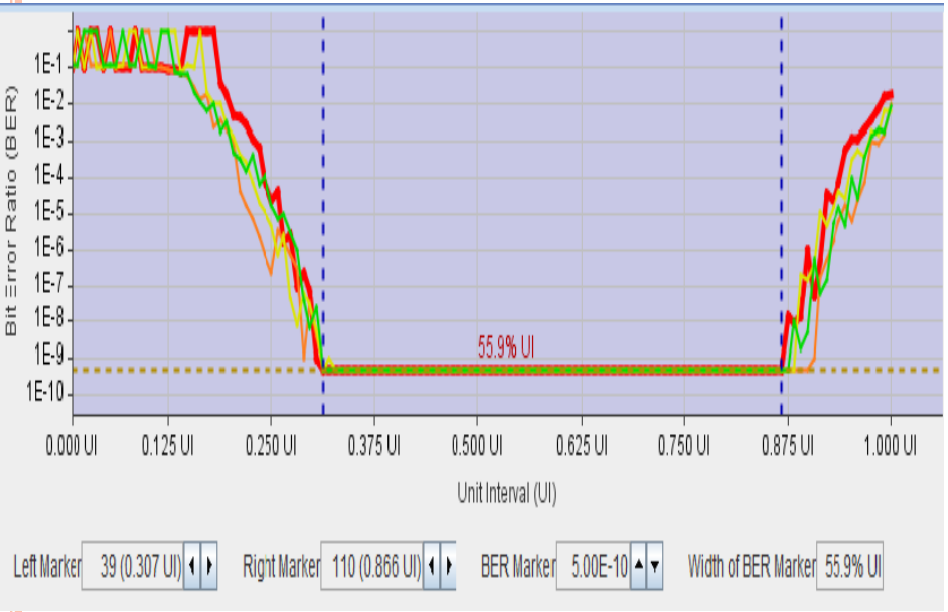


IBERT Initial Settings

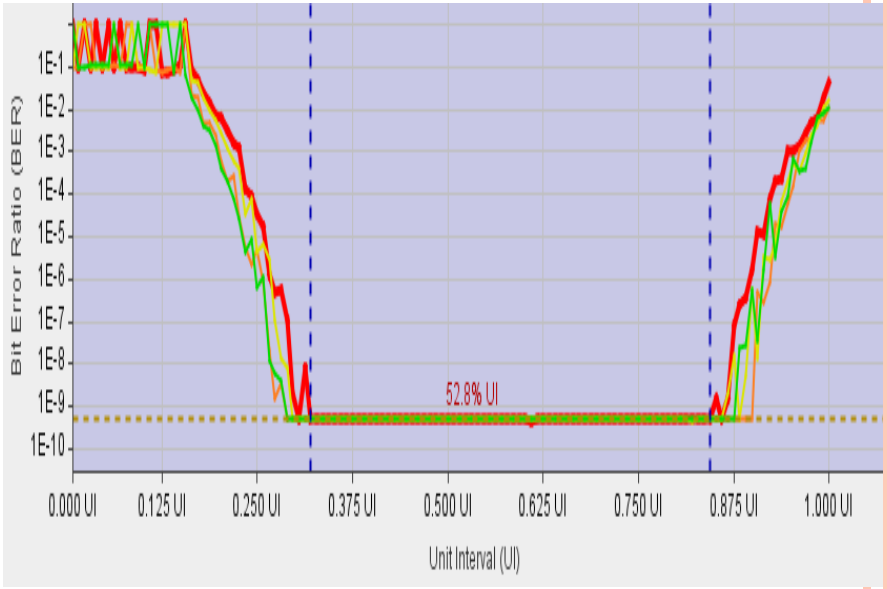
Bathtub Curve to Calculate Bit Error Rate (SMA)

- **Line rate: 2.5 Gbps. Frequency 200Mhz**

Length 1foot



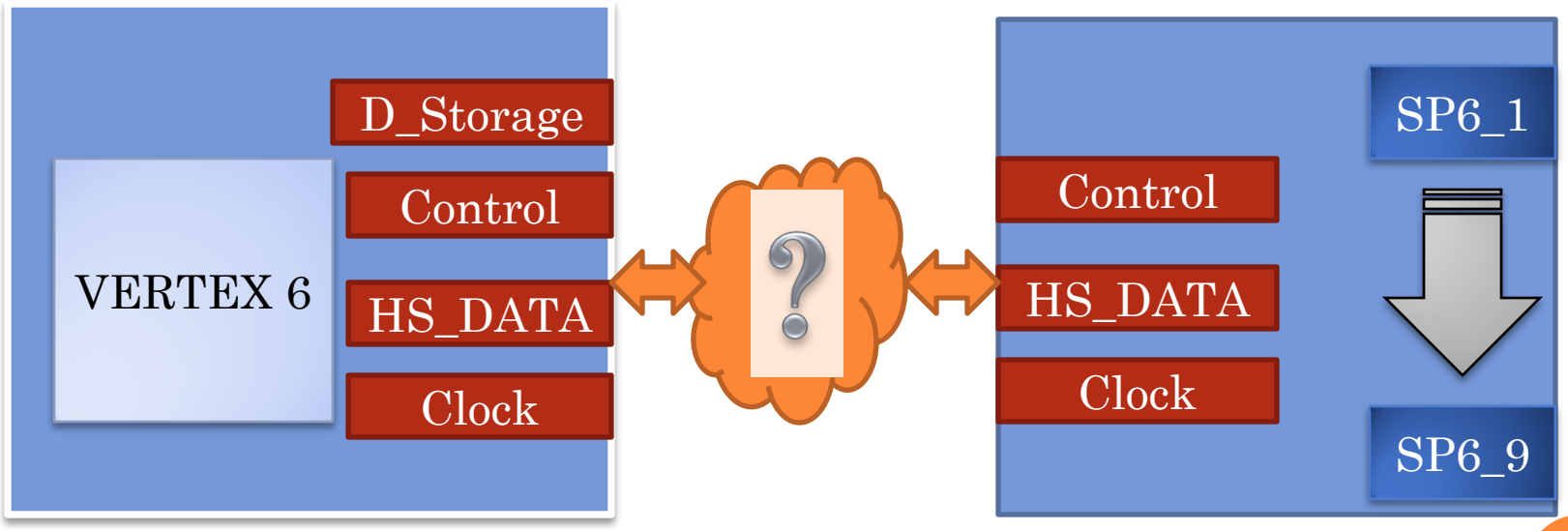
Length 2feet



UI OF BATHTUB CURVE @ SYSTEM FREQ 200MHZ

Line rate	1 Foot	2 Feet
2.5 Gbps	55.9%	52.8%
3.125 Gbps	44.5%	38.6%
5 Gbps	36.2.3%	32.3%

Board Level Compatibility Between Master Card & Carrier Card



Carrier Board Schematic and layout

CONTROL

Master Card

- Master Clock 40 MHz
- Chip Select IC
  - Controlling Carrier Card
- JTAG Header
  - External Programming

Carrier Card

- Chip Select IC
  - Enabling Spartan-6 on Carrier Card
- JTAG Header
  - Programming Through Master Card

High Speed Data

- Connector Configuration
- Routing Technique
  - Differential Pair
  - Length Tuning
  - Signal Integrity Analysis

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- Routing Technique
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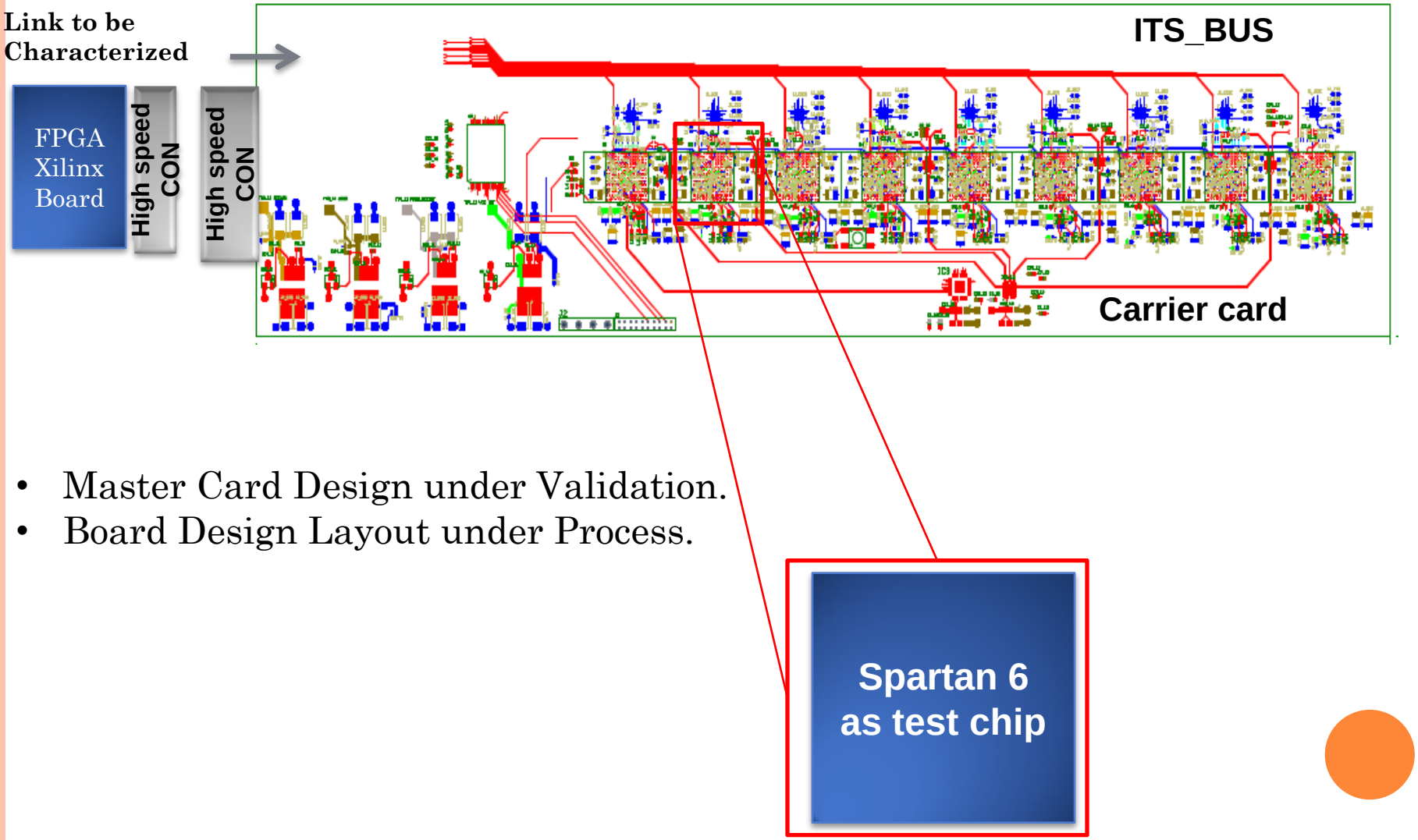
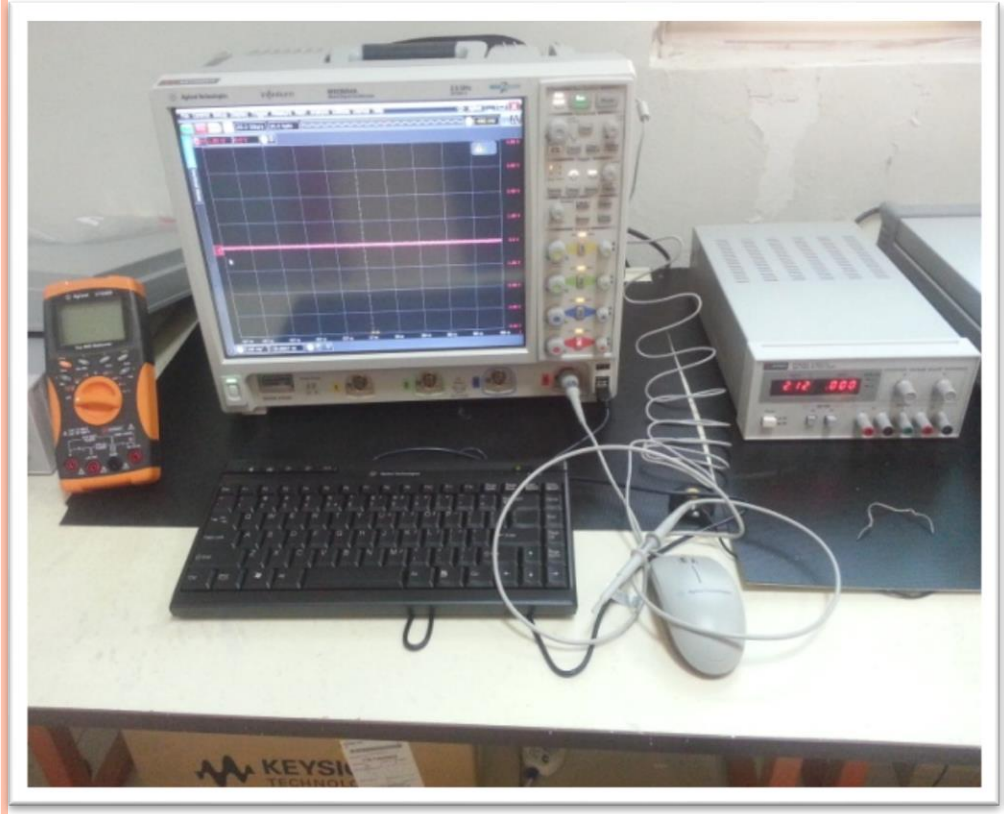
PURPOSED DESIGN TO TEST SERIAL LINK CHRACTERIZATION



- Master Card Design under Validation.
- Board Design Layout under Process.

Hardware setup



Agilent Infiniium 9000 Series Oscilloscopes

Keysight 81150A Pulse Function Arbitrary Noise Generators

ML605-Vitex 6