ALICE ITS, MFT, O2 Asian workshop 15-16 December 2015

ITS Upgrade / MFT session

L. Musa - notes => not comprehensive minutes

| Presenter | Institute | Topic | Notes |
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| Chinorat Kobdaj | SUT | Detector Geometry | - Model of Inner Barrel completed<br>- Model of Inner Service Barrel : ongoing<br>- Model of the services, in particular the power distribution module (DC-DC converters) should have priority. Target April '15 |
| Magnus Mager | CERN | Pixel Chip characterization | - MISTRAL FSBB-M0 results<br>- ALPIDE results<br>• CERN test beam<br>• Pohang test beam (Pusan)<br>- Validation of both architectures completed<br>- Work on explorer (Pusan)<br>- SEL tests |
| KyungEon Choi | Pusan | Pixel Chip characterization | - Si-Lab ready. Clean-room is being set-up<br>- Characterization of Expliorer-1 irradiated at $10^{13}$ n/cm$^2$ ongoing<br>- Test at Pohang (60MeV e) of irradiated Explorer-1 chip and pALPIDE-1<br>- Schedule for Pohang facility in 2015: first slot of one week in March/April? TBC |
| Jong-han Park | Inha | Pixel Chip characterization | - Lab test of (6 thin + 1 thick) pALPIDE-1 chips using the chip internal pulsing system (S-curve, noise, thresholds) pulse system and radioactive source ($^{55}$Fe) (Hit maps). Measurements done at Vbb=0V.<br>- Participation in the Pohang test campaign<br>- It is proposed to look at individual faulty pixels (if any) and identify the probability that the fault is related to the collection diode => does the circuit respond correctly to the pulsing system? |
| Kritsada Kittimanapun | SLRI | Pixel Chip characterization | - Availability of 1 Gev e beam for about 20h/d<br>- 1 Gev e beam is suitable for the characterization of ITS sensors<br>- current intensity too high (~mA)<br>- Short term set-up: tests with very thick lead absorber (5 – 60 mm) + lead collimator. Emerging beam non |

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| | | | monochromatic + very large background from secondary particles.<br>- Planned set-up (temporarily): use 4-degree magnet as energy selector (BTF at DAFNE). This set-up will be ready by June 2015.<br>- Long-term plan (2 years) to develop a set-up to provide low-intensity monochromatic beams. |
| Jirawat Prabket | TMEC | Post-processing | - QA of Si raw wafers<br>• 4 point resistivity measurements<br>• SEM cross section pictures<br>• SRP measurements<br>Issue: identified large discrepancy between values quoted by wafer supplier and measured values. (Discussion with Petra)<br>- Si micro-channels<br>- Coordination of STARS activities on thinning & (laser) dicing |
| Petra Riedler | CERN | Post-processing | Wafer procurement and QA<br>- surface resistivity<br>- SRP measurement<br>- XSEM inspection<br>Plating (IZM, TMEC, Pacthec)<br>- Passivation of all areas outside contact pads<br>- Ni deposition (3-5 um)<br>- Au deposition (~50-100nm)<br>Thinning & Dicing<br>- Diamond wheel pre-dicing before grinding - DBG (Rockwood)<br>- Laser dicing after grinding (STARS)<br>Visual Inspection QA<br>- Reference to Esa presentation<br>Laser soldering<br>- General optimization (refinement) of the procedure<br>- Intensive work to classify soldering contacts using and cross-correlating various methods: integrated power, temperature, electrical test, metallurgical cross-section X-ray image<br>Transport Test |
| Youngil Kwon | Yonsei | Chip series test | - Test system. Two companies contacted. Cost of the test system:<br>- EC3 (small company): 140 kCHF |

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| | | | - GENESEM (large company): 200 kCHF:<br>- position accuracy (25um x 25um);<br>- Probe card needles: maximum overdrive vs. potential damage to the pads is being evaluated;<br>- Test procedure: is the optical (laser) test needed?<br>- Specifications for test system, including test procedure, should be prepared by Feb 2015 (Yonsey+CERN). |
| Esa Prakasa | LIPI | QA | - QA for single pixel chip test<br>- Thickness of pads => is it needed;<br>- interconnection (daisy chain) lines, => not needed in CMOS chip<br>- presence of cracks on the pads<br>- missing in presentation: chip dimensions and inspection of quality of the edges;<br>- QA for modules assembly: same tests as for single chip + position of chip wrt external markers (available within field ov view centered around the chip markers)<br>- QA for FPC: not yet started<br>- Define specifications for visual inspection by Feb 2015 |
| Vito Manzari | INFN | Outer barrel | - Procedure for module assembly<br>- Chips are inspected visually before mounting them on the FPC. Can this replace the visual inspection carried out at chip series test?<br>- Test System: VME interface only for distribution of power supplies. Should we consider in the next version a standalone power block. |
| Antonello Di Mauro | INFN | Laser Soldering, Automatic assembly Machine | - Laser soldering<br>- Module assembly system<br>• Scope of the tendering<br>• Specifications<br>• Baseline + options |
| Bon-Hwi | Pusan | Module Construction | - Setting-up lab for module assembly<br>- Transport test: 6 out of 17 chips damaged<br>- Laser soldering QA<br>- Categorize soldering type<br>- Check the measured values<br>- Data analysis |
| Xiangming Sun | CCNU | Module Assembly at | - Automation of chip placement: automatize the correction of chip final |

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| | | CCNU | position.<br>- Comment: automation of any other operation is not justified |
| Arshad Bhatti | COMSATS | Pixel chip simulations | - TCAD simulations: simulations performed for ideal doping profiles (constant average doping with Gaussian spread). |
| Jibran | COMSATS | Readout Electronics | Test system for IB data transmission: board should be constructed ASAP. One PhD student from CERN will work in close collaboration with COMSATS. |
| Dong Wang | CCNU | High-speed link evaluation | - Evaluation of GBT link (ongoing) using Xilinx KC705 (ongoing)<br>- High-speed data transport (Jesd204b) evaluated using an fast ADC form Analogue Devices and the KC705.<br>=> comment: Xilink cannot be used for the implementation of the Readout Unid because sensitive to SEU. |
| Ann Silapunt | KMUTT | Electronics | - Introduction of the group and plans.<br>- Master student to work on<br>- Welcome!!! |