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Visual Metrology of Pixel Chips and Flexible Printed Circuit (FPC) for Physical Quality Assessment

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Outline

- Introduction
- 3D Chip Surface Analysis
- Chip Spacing Measurements
- Surface Cracking Identification
- Summary and Issues

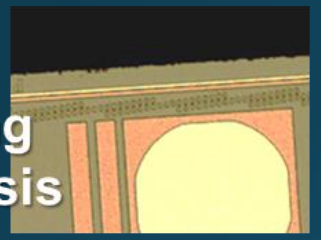
Introduction

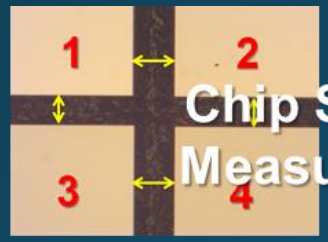
- Metrological measurements are required to ensure all of the components used in the ITS detectors satisfy the required specifications.
- Automatic vision inspection is proposed to apply in the fabrication stages of sensor chip and chip mounting on flexible printed circuit.
- The vision system aims to conduct accurate metrology measurment and objective assessment at high speed.

Action Plan Preview

Development of Testing System Based on Machine Vision

Edge Cutting Analysis

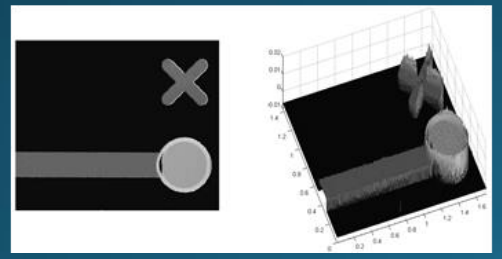




Chip Spacing Measurement

Surface Crack Identification

Impurity Analysis

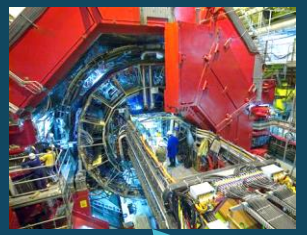


3D Chip Surface Analysis

2015

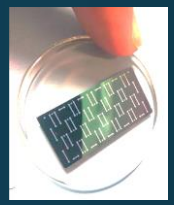
Testing of Sensor Chip and FPC

CERN, Switzerland



Component design

Mass production



Tested component

Fabricated component

Visual Testing

2016

Research Progress

Now

Task	2014				2015											
	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12
3D chip surface analysis	√	√	√	√	√	√	√	√	√	√	√					
Chip spacing measurement			√	√	√	√	√	√	√	√						
Edge cutting		√	√	√	√	√	√	√								
Surface crack identification			√	√	√	√	√	√	√	√						
Impurity analysis				√	√	√	√	√	√	√	√					
Algorithm testing								√	√	√	√	√	√	√	√	√

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- Introduction
- **3D Chip Surface Analysis**
- Chip Spacing Measurements
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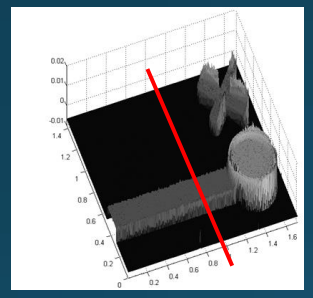
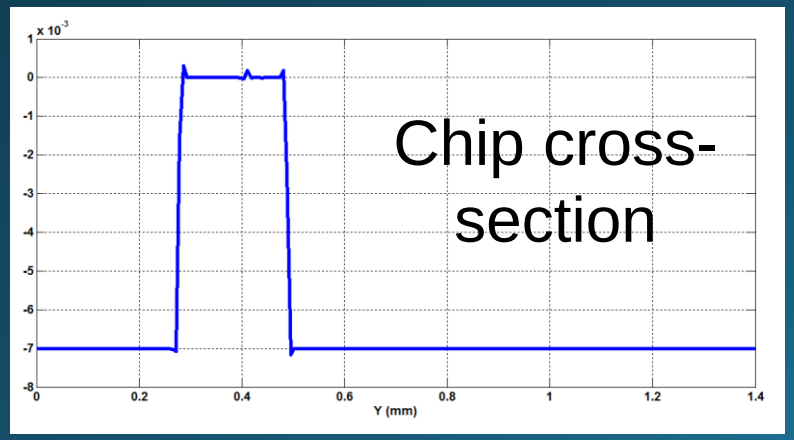
3D Measurement of Chip Surface

- 3D image acquisition is required to obtain depth information of the chip surfaces. The information is used in several analyses, such as pad thickness (sensor chip) and inner surface assessment of the solder holes (FPC).

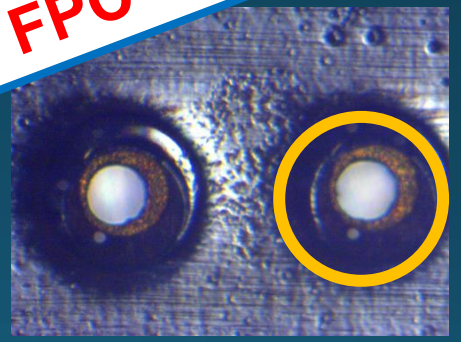
Sensor chip



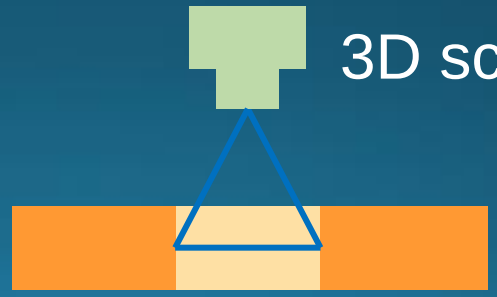


Chip cross-section

FPC



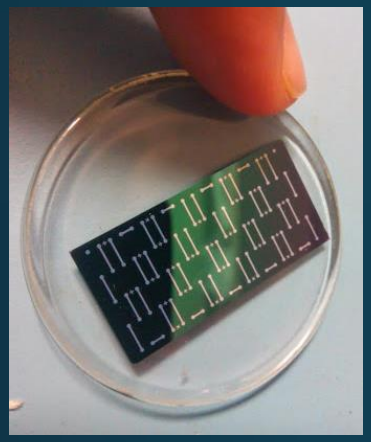
Top view of solder hole

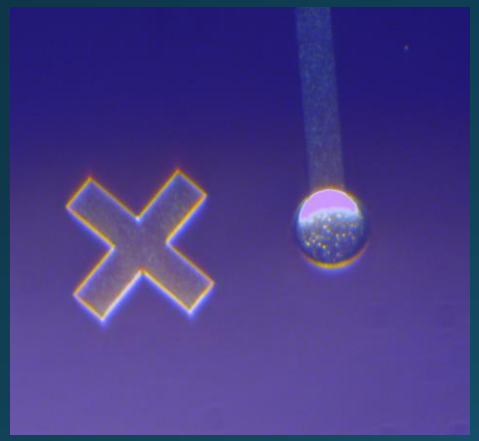


3D scanner

Side view of solder hole

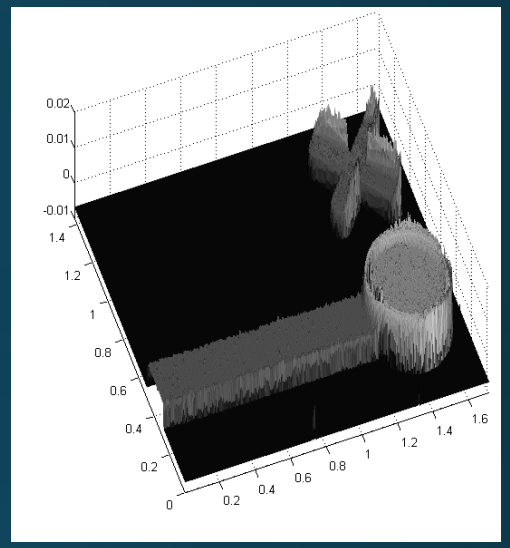
3D Surface Acquisition



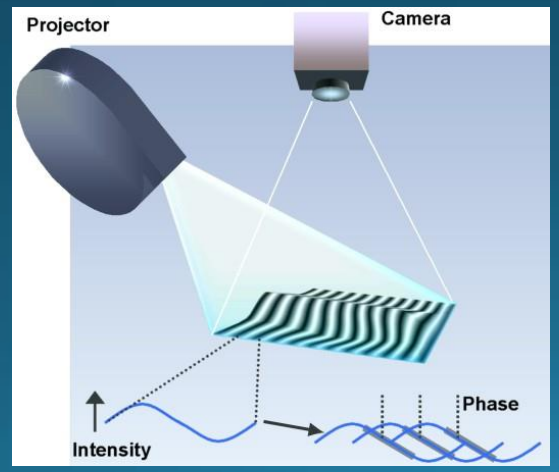


Chip sample

GFM MikroCAD is used to scan
3D surface of sensor chip



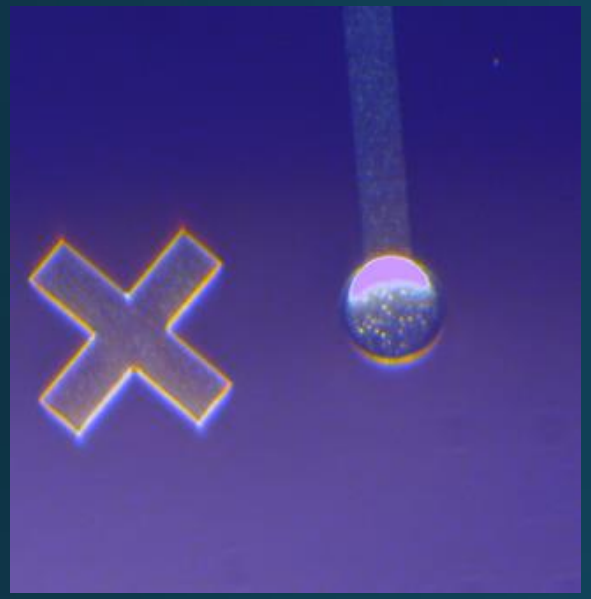
3D surface of sensor chip

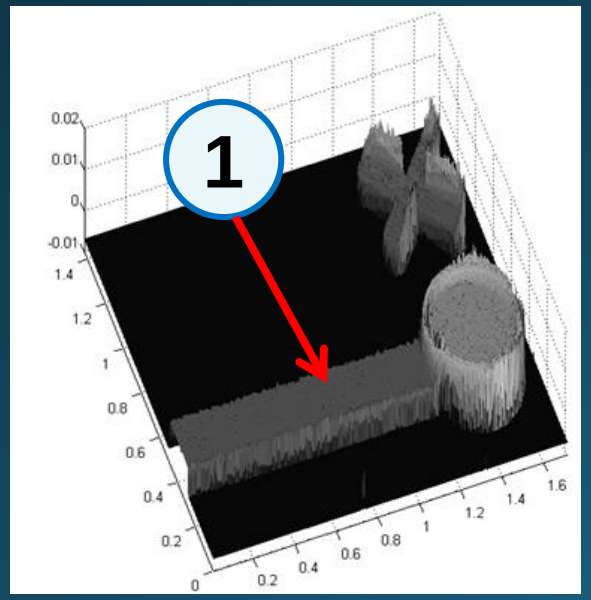


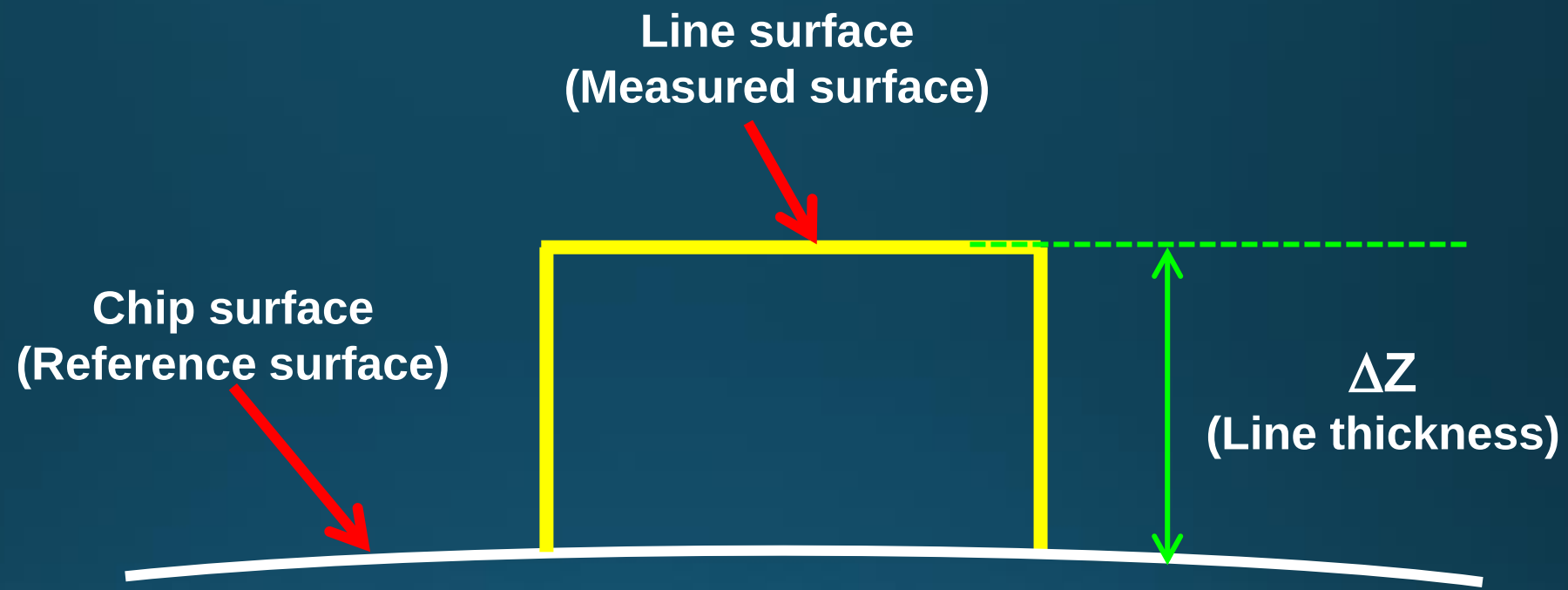
Structured Light Projection Method

Spatial resolution : 1.2 µm
Field of view: 1.6 x 1.2 mm²

Thickness of Connection Line





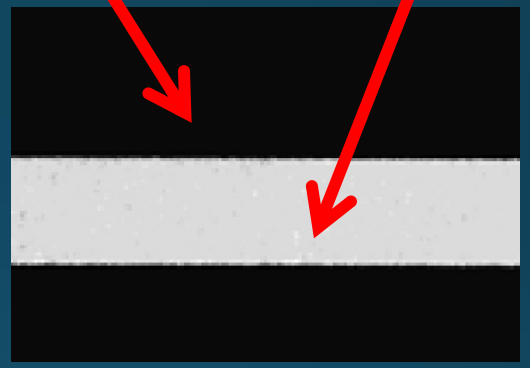


Line surface (Measured surface) — Chip surface (Reference surface) = ΔZ (Line thickness)

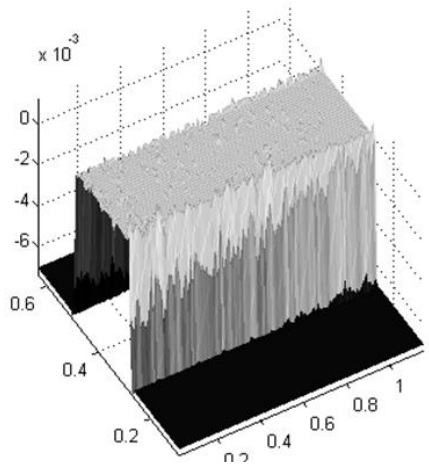
3D Measurement of Line Connection

Reference area

Line connection area

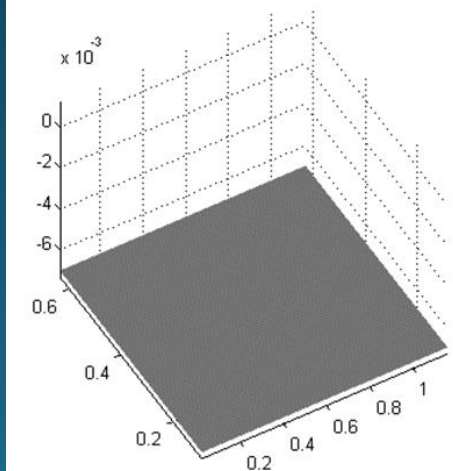


The 2nd order polynomial surface fitting is used to construct the reference area



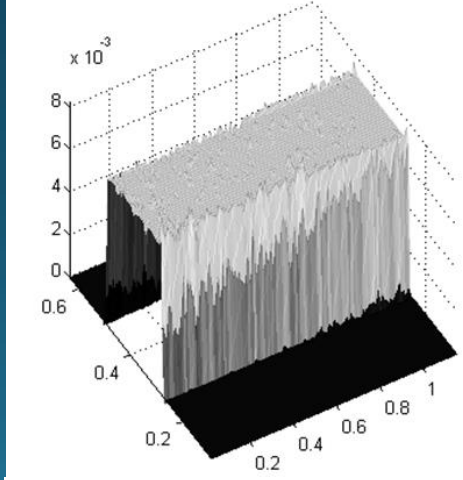
Measured area

−



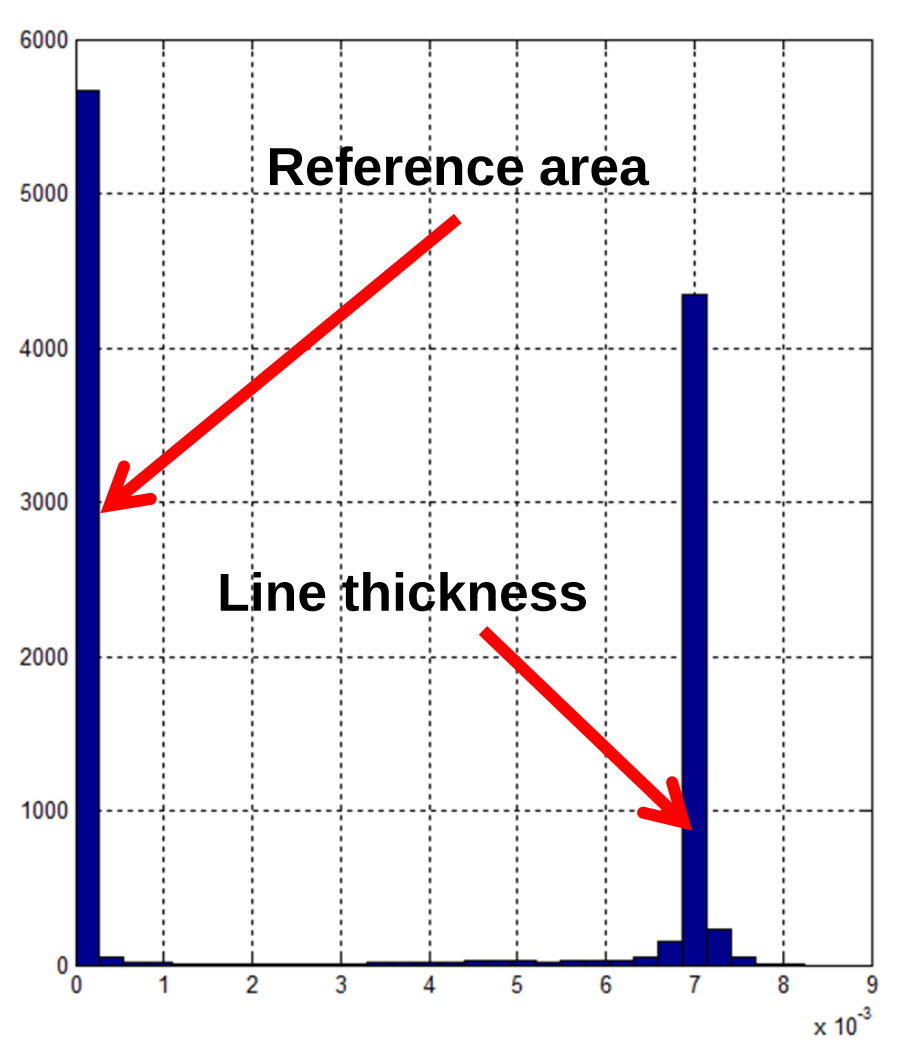
Reference area

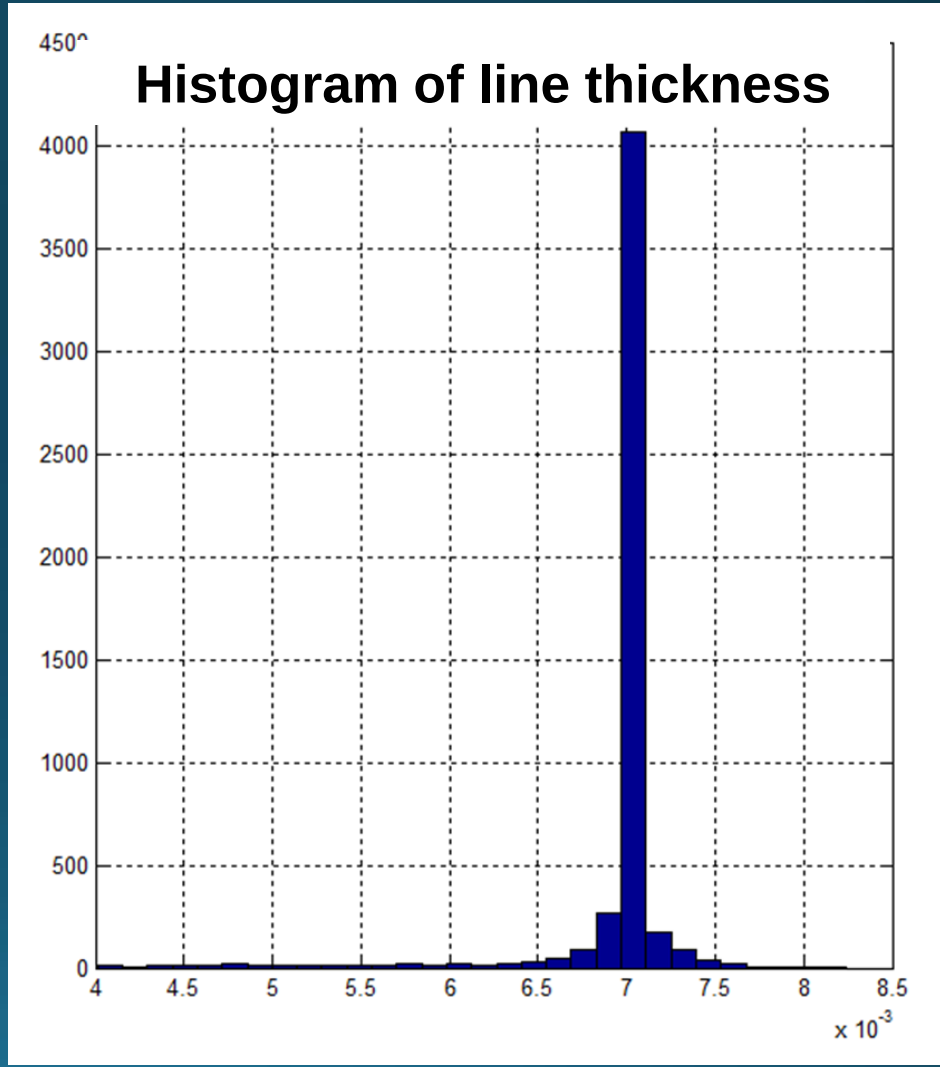
=



Deviation surface

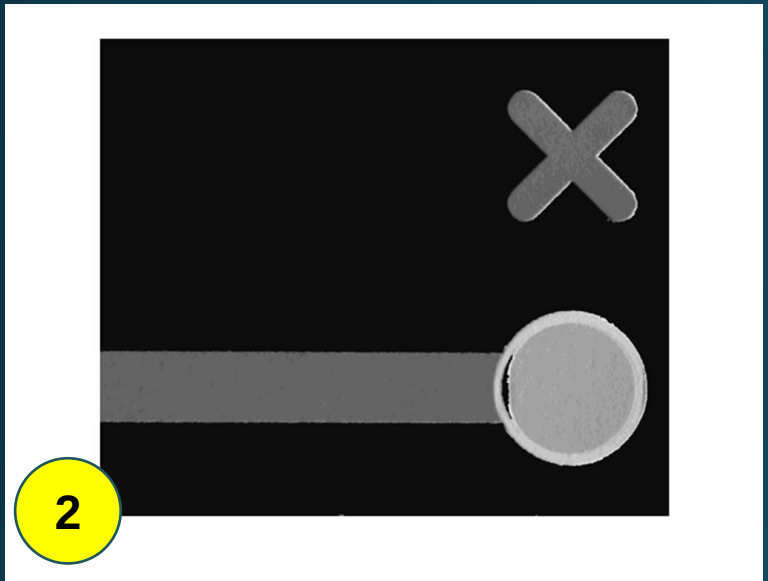
Thickness of Line Connection

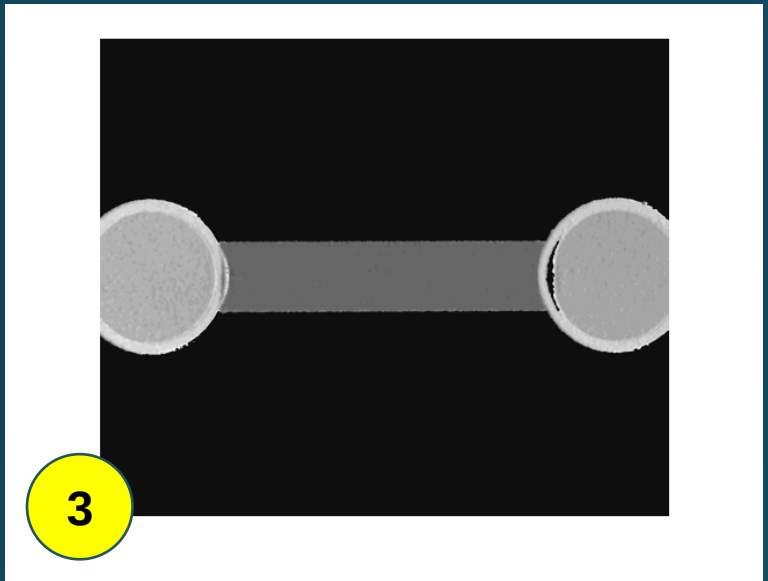


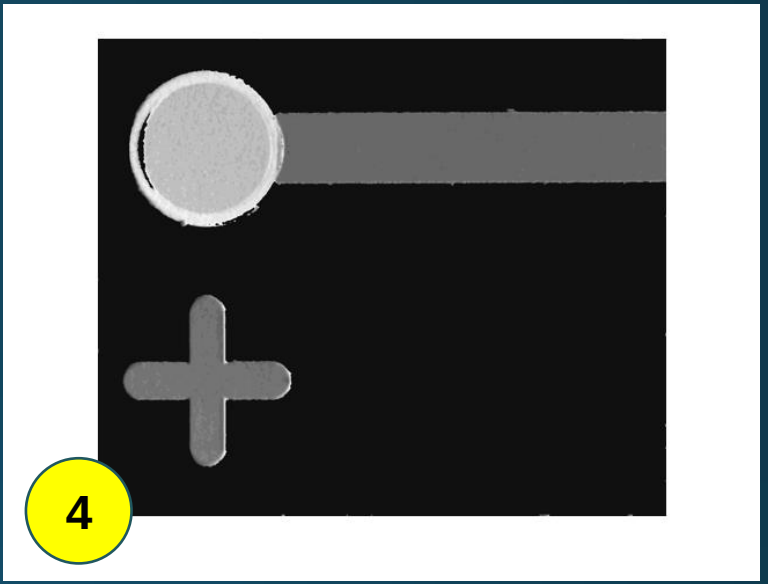


Thickness of line connection:
$0.0069 \pm 3.9888 \times 10^{-4}$ mm = 6.9 ± 0.4 µm

Measurement of Additional Samples

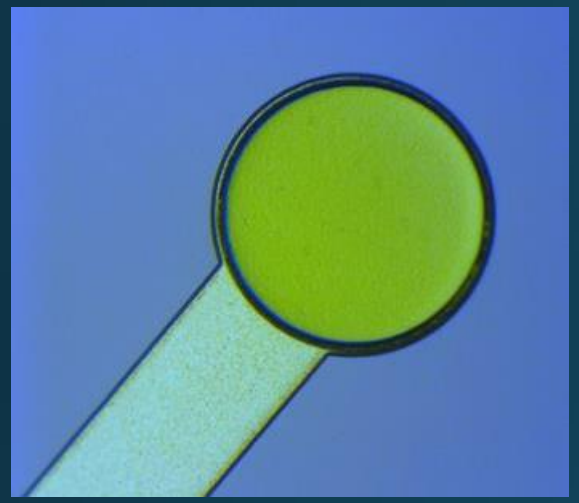


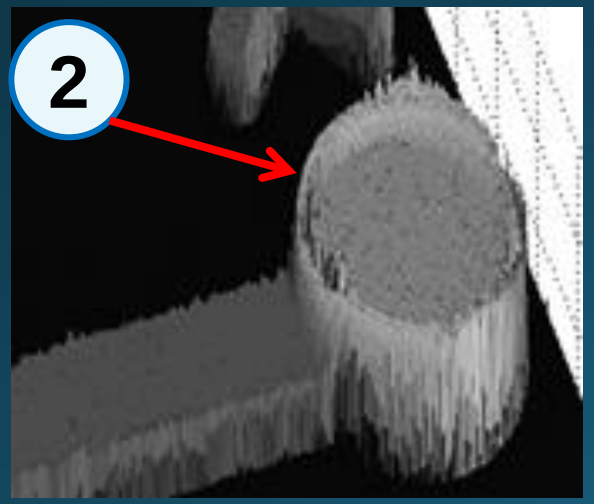


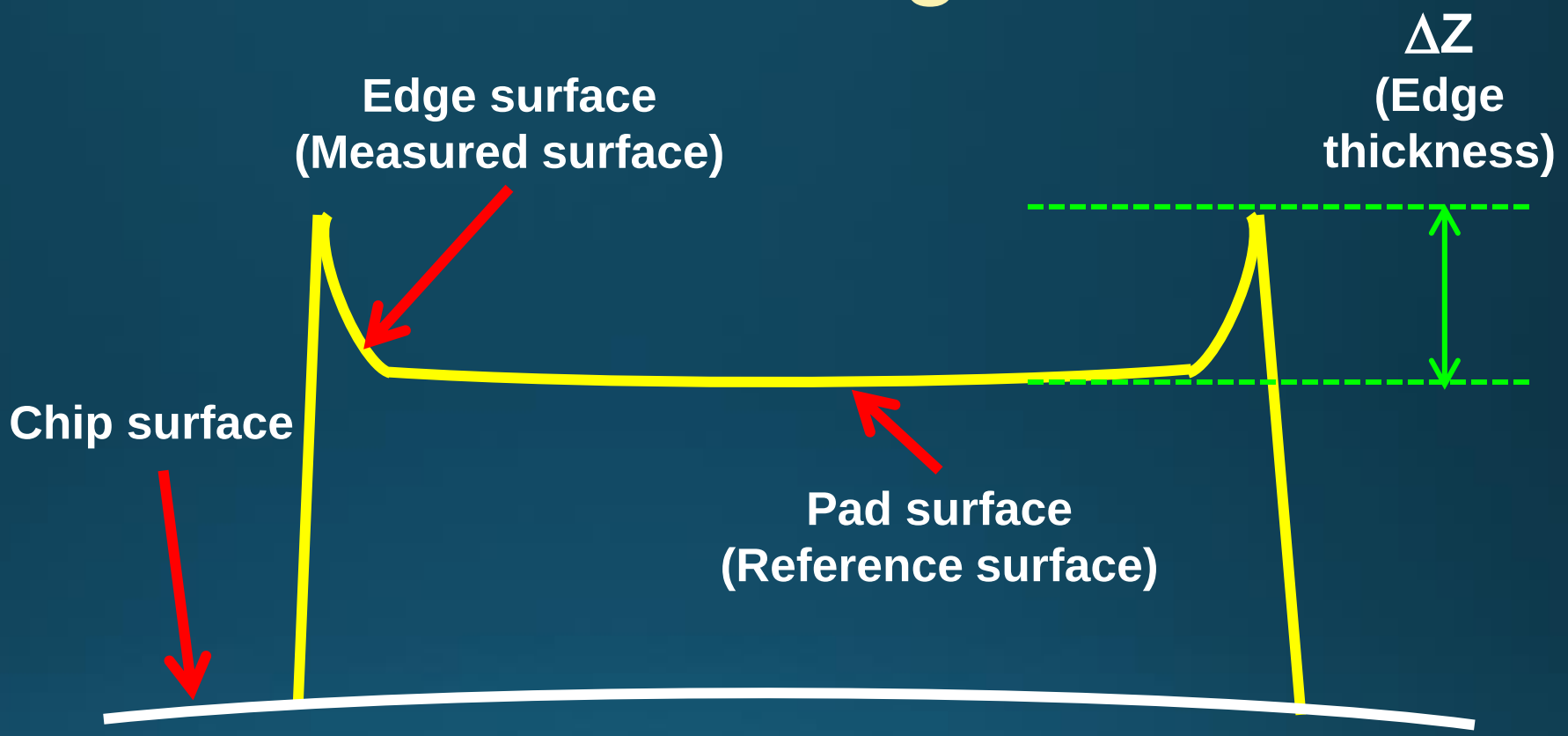


Sample No	Line thickness (mm)	Standard deviation (mm)
2	0.0069	4.5331×10^{-4}
3	0.0069	4.1794×10^{-4}
4	0.0069	3.6813×10^{-4}

Thickness of Pad Edge



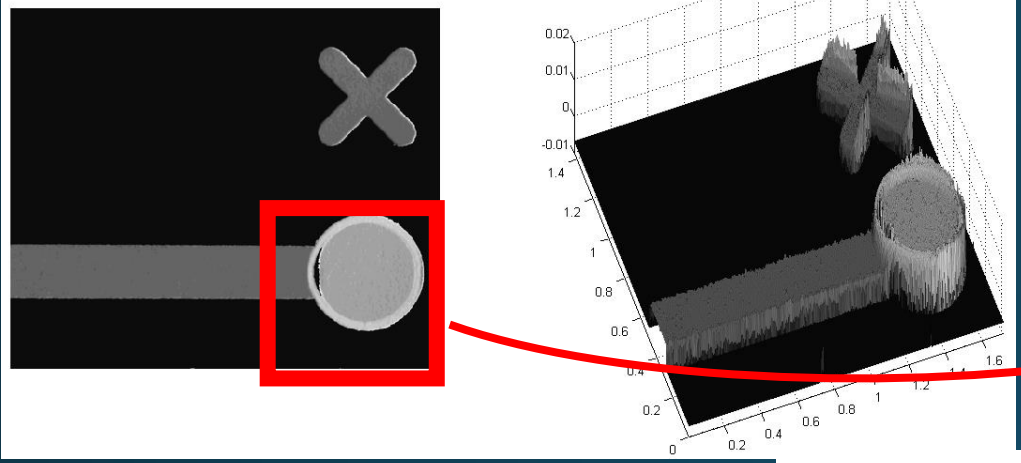


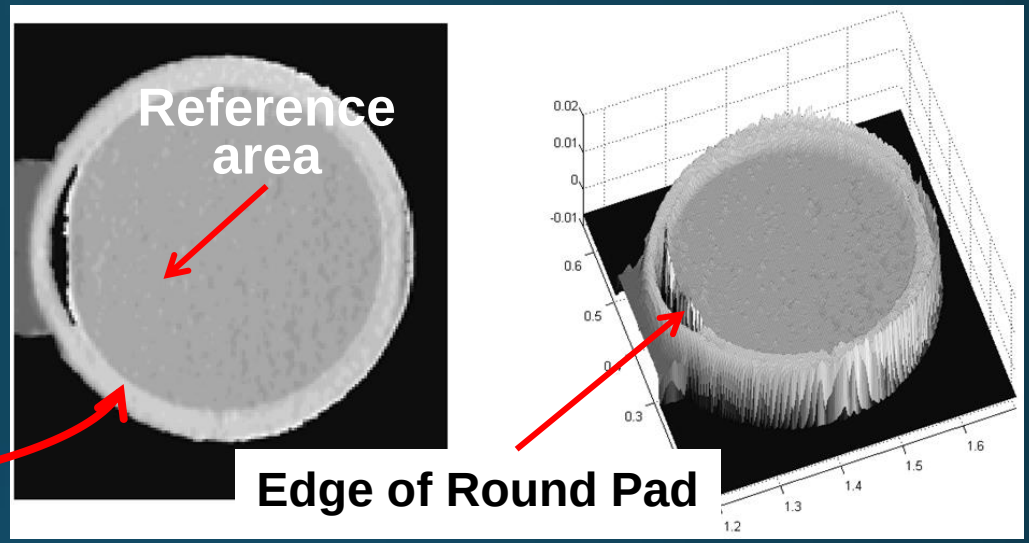


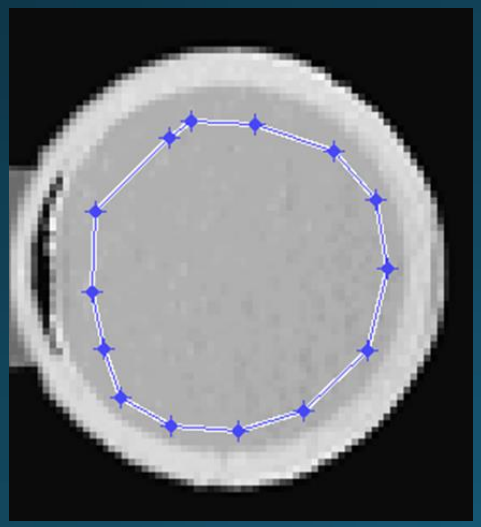
Edge surface (Measured surface) − Pad surface (Reference surface) = ΔZ (Edge thickness)

3D Measurement of Pad Edge

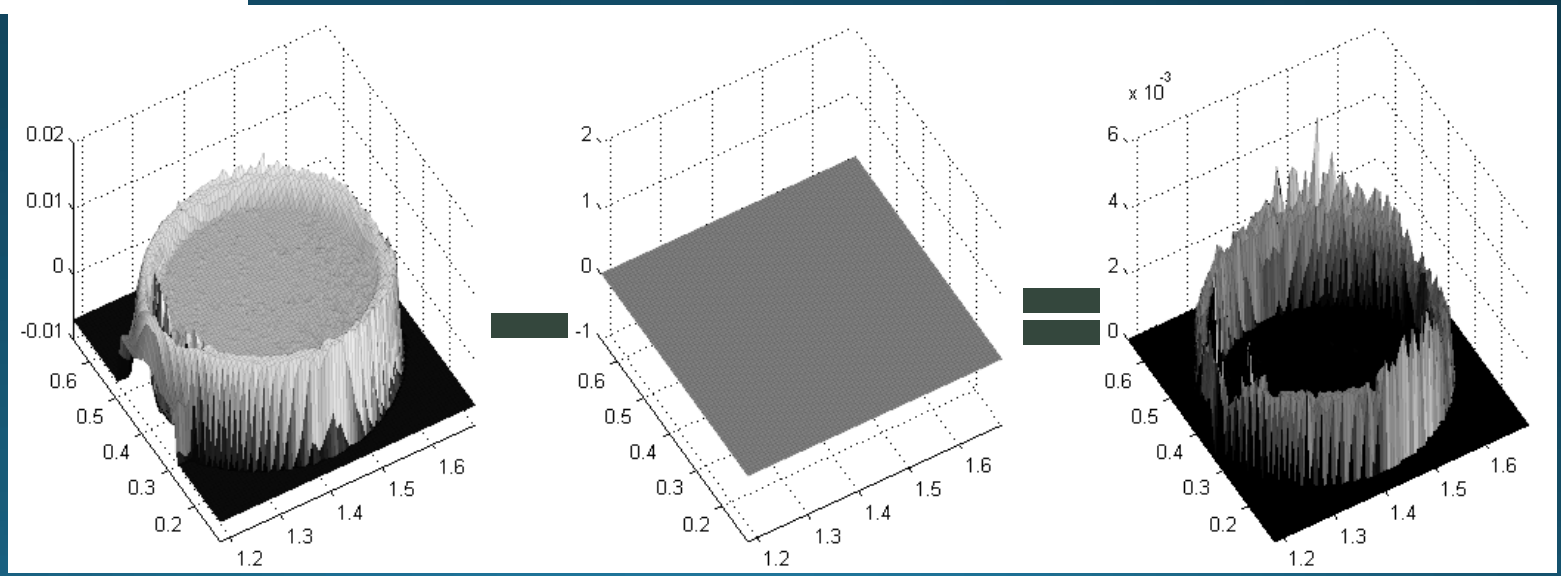
ROI of the round pad surface





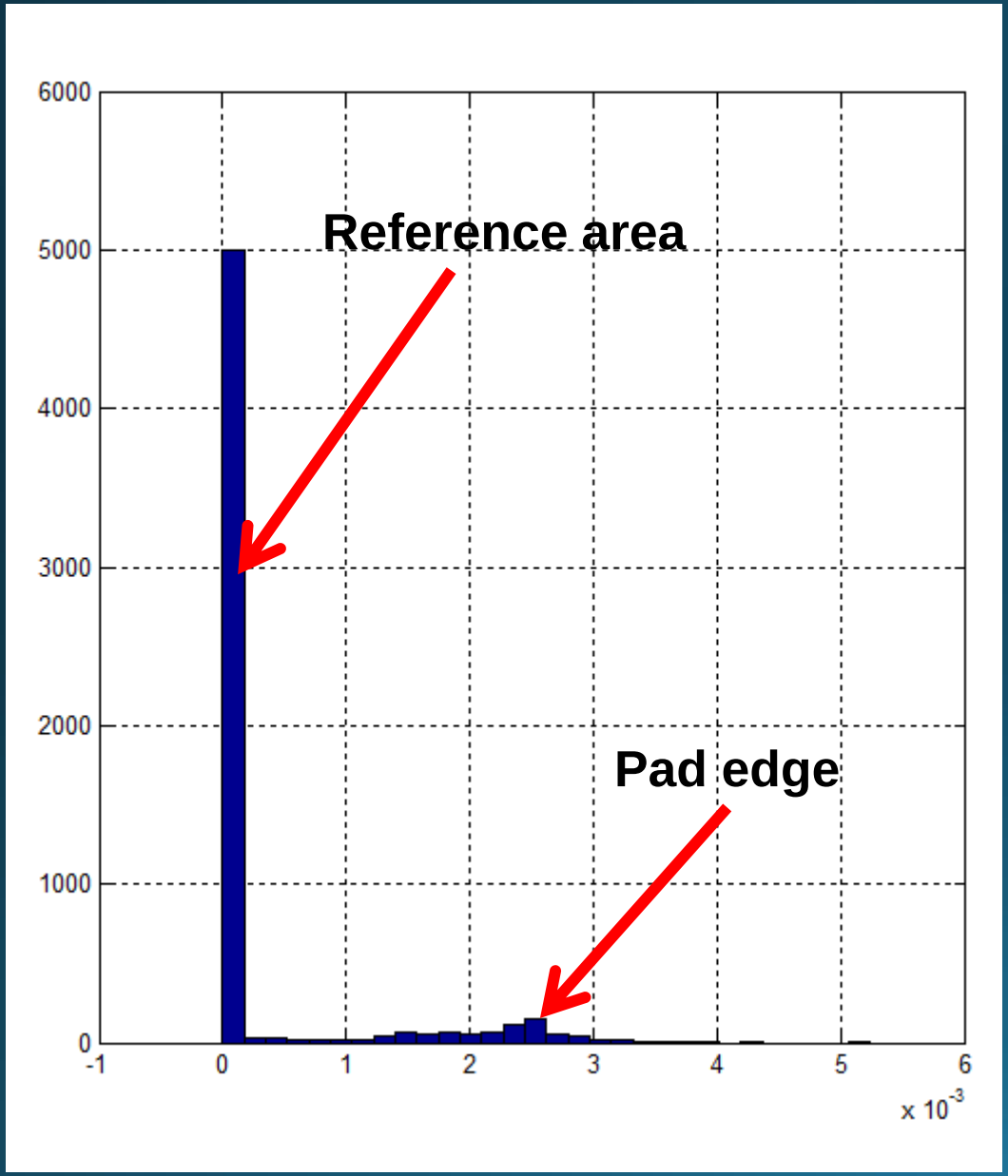


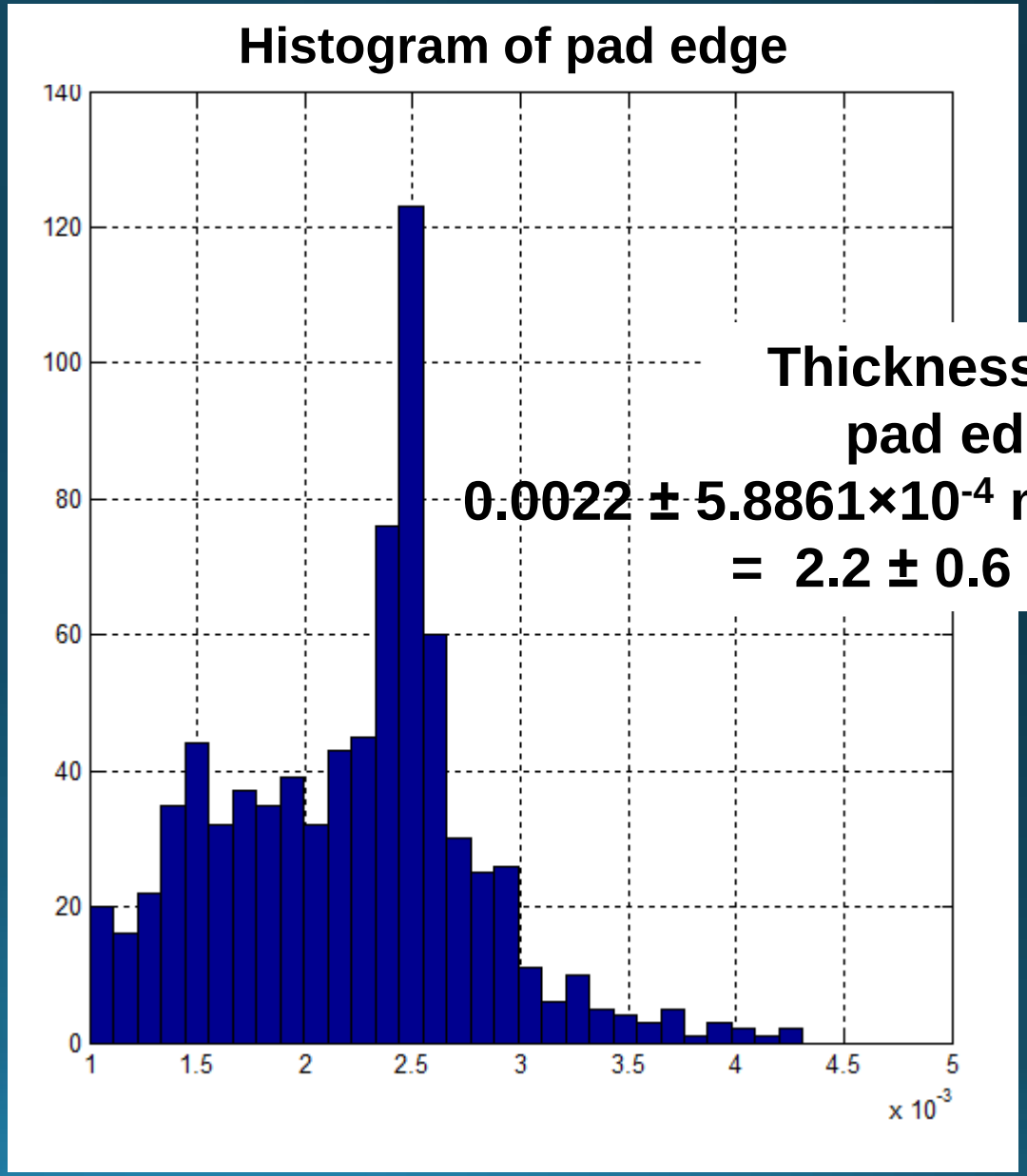
Sample for reference area



Measured area	Reference area	Deviation surface

Thickness of Pad Edge





Thickness of pad edge:
$0.0022 \pm 5.8861 \times 10^{-4}$ mm
= 2.2 ± 0.6 μm

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- **Chip Spacing Measurements**
- Surface Cracking Identification
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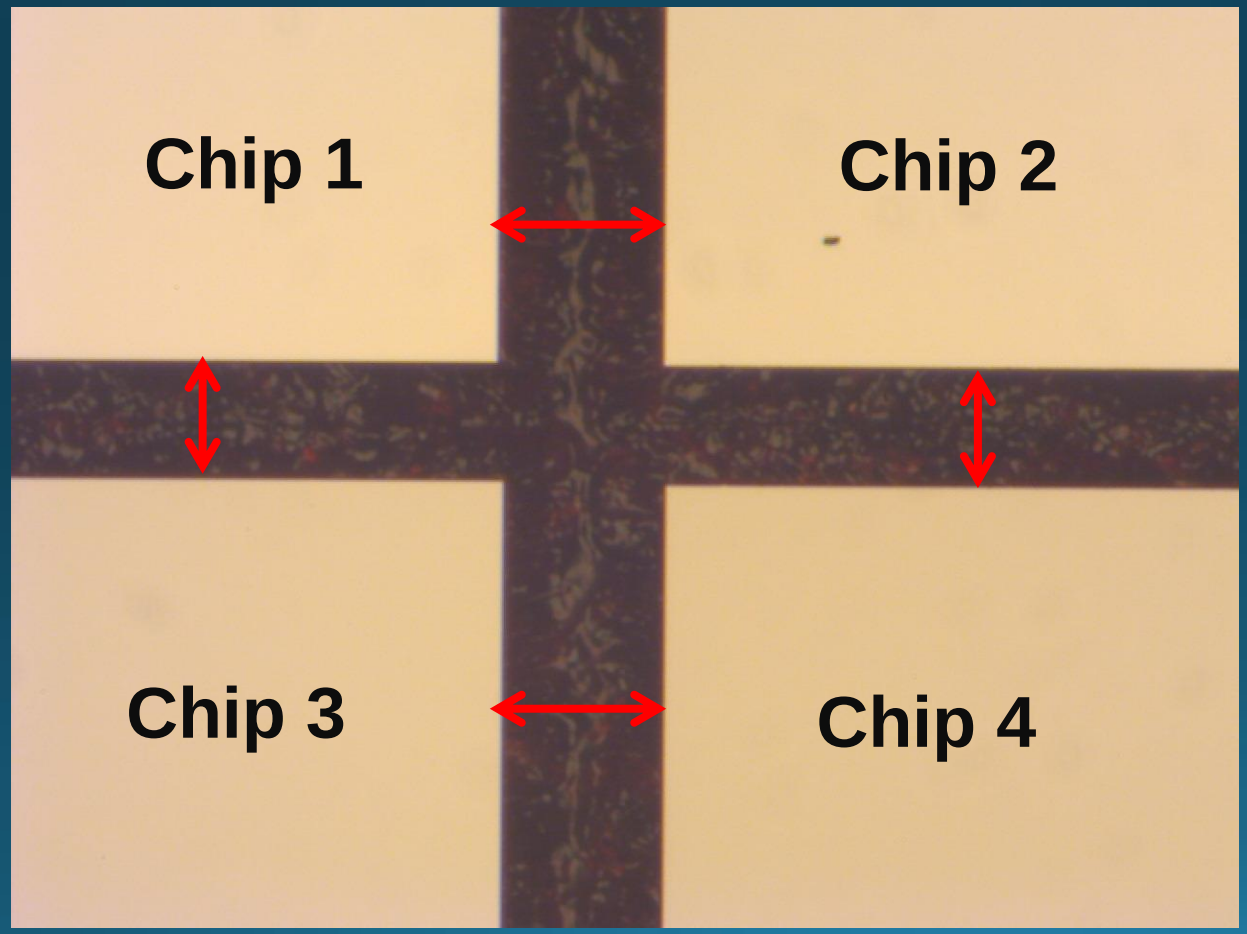
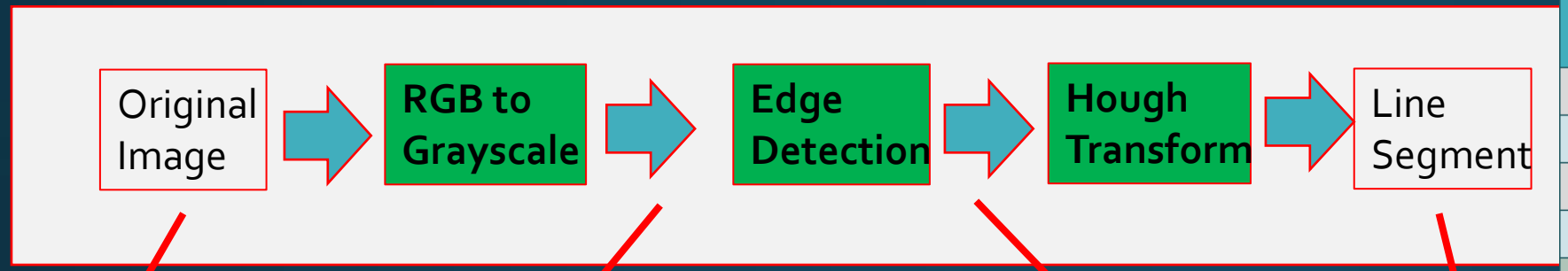
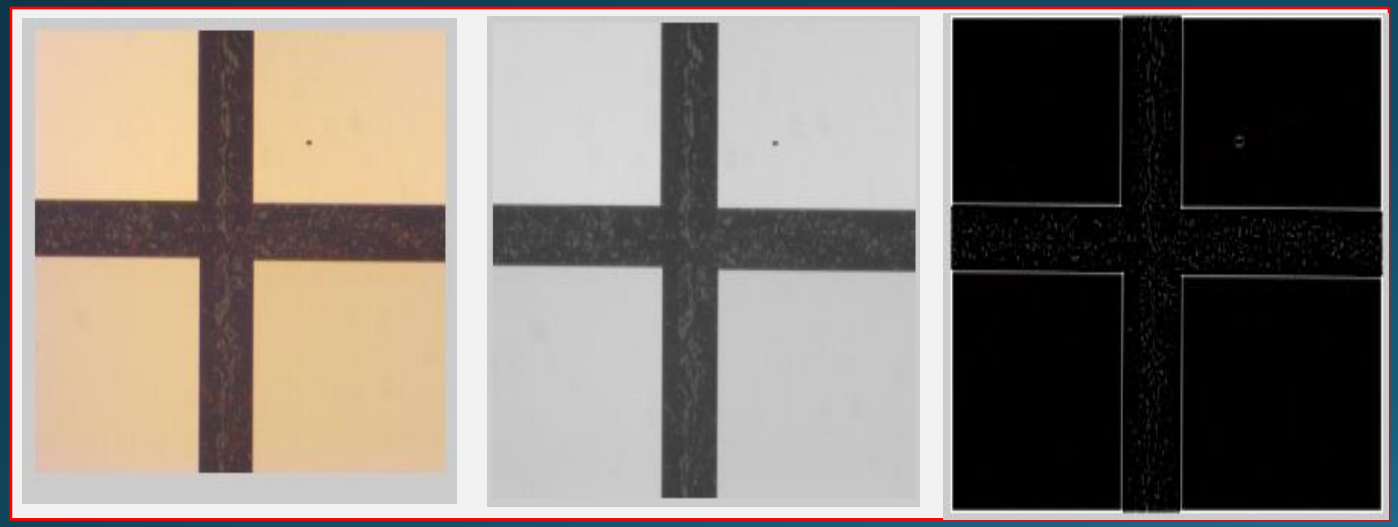
Chip Spacing Measurement - Motivation

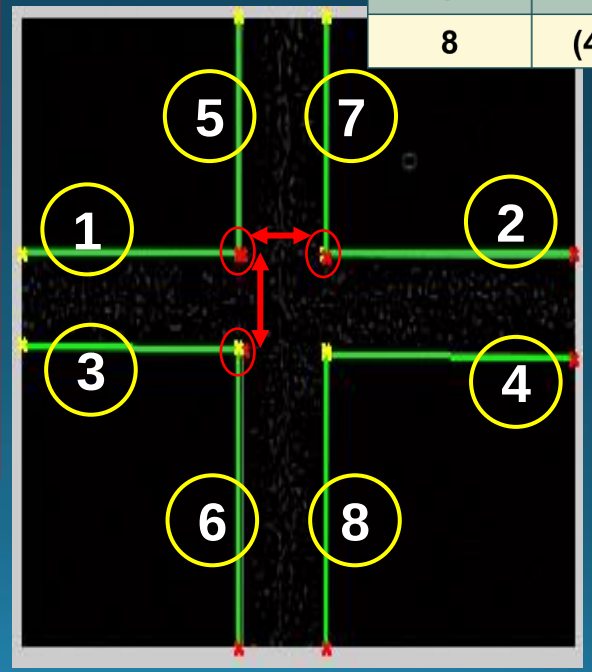
The distances of chip spacing (red arrows) should be less than the tolerable sizes (nominal gap : 100 μm)



Chip Spacing Measurement - Solution



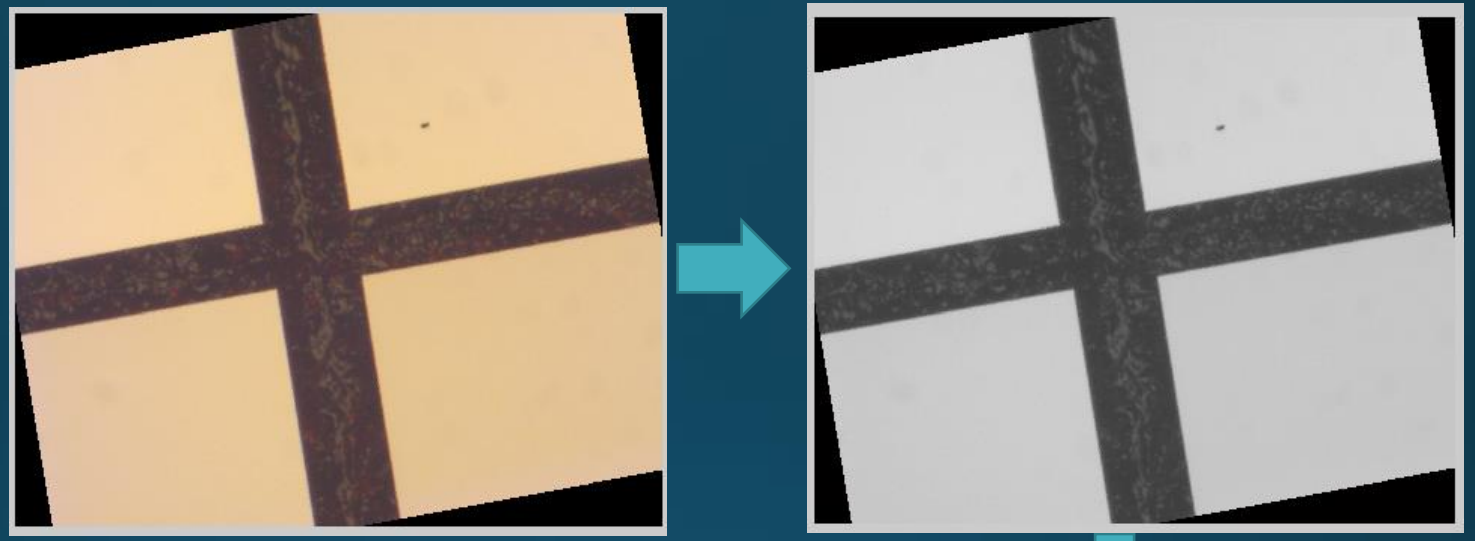




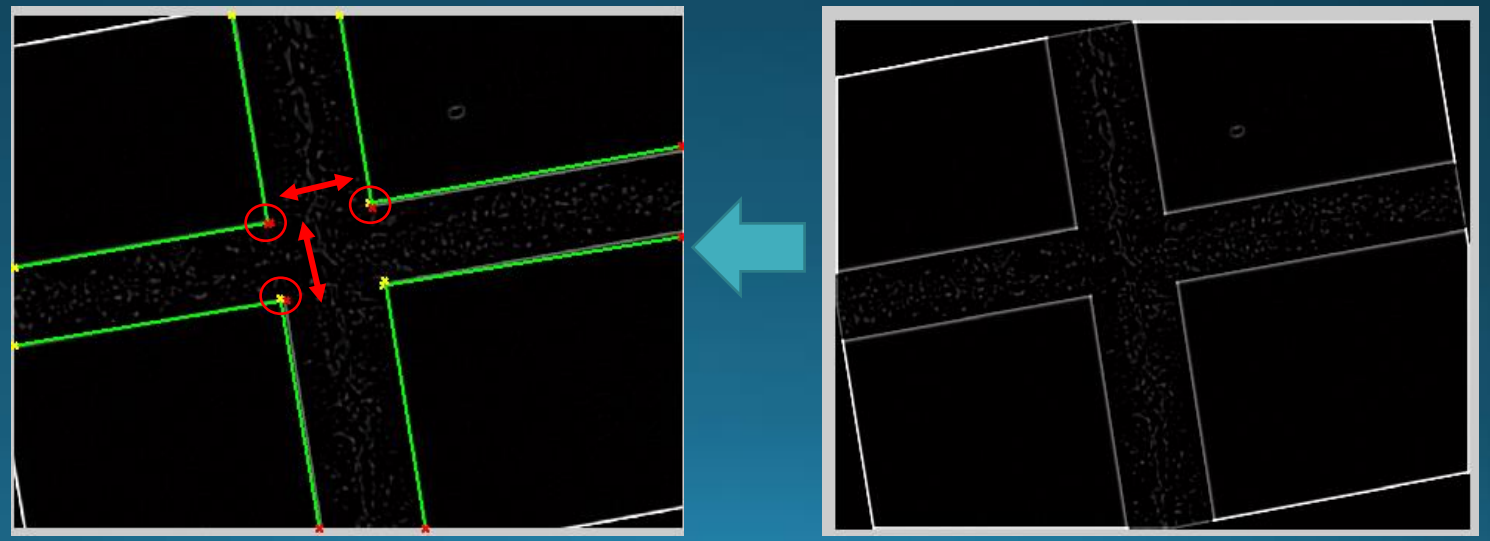
Line Segment	Pixel Coordinate X(row), Y(column)		Parallel with
	Start	End	
1	(319,1)	(319,459)	3
2	(319,632)	(319,1151)	4
3	(444,1)	(452,465)	1
4	(455,633)	(464,1151)	2
5	(1,453)	(322,453)	7
6	(466,453)	(851,453)	8
7	(1,636)	(326,636)	5
8	(450,636)	(851,636)	6

Rotation Testing

Captured image,
Not perpendicular
(rotated by 10º)



The spacing still can be measured as long as the coordinates of start and end of each line are marked



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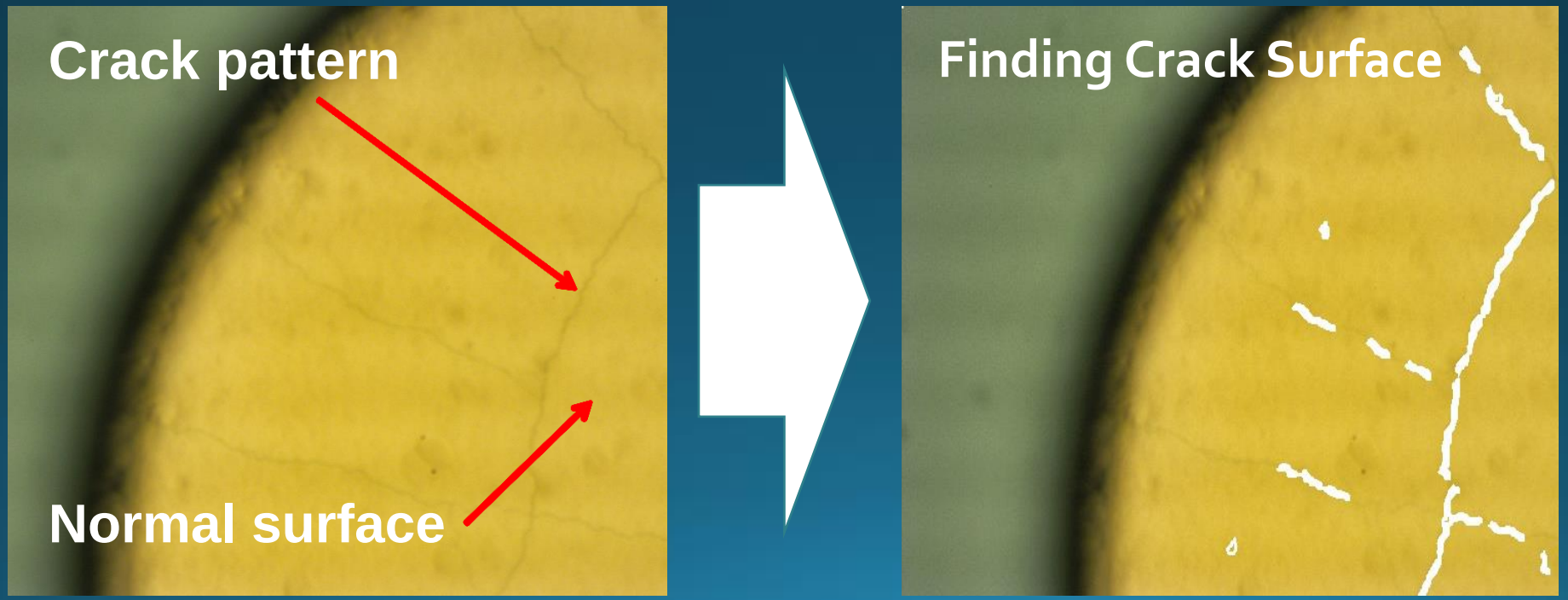
Problem, Objectives, and Proposed Method

Research Problem: How to find the cracks appeared on the chip surface?

Research Objectives:

- The crack can be identified from the chip surface.
- The crack type is able to be classified based on its pattern and size features



Problem, Objectives, and Proposed Method

Research Problem: How to find the cracks appeared on the chip surface?

Research Objectives:

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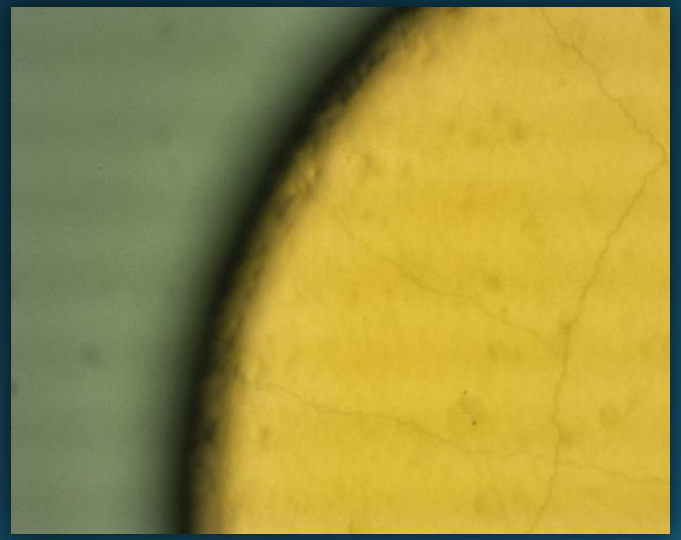
Surface Crack Identification - Solution

Original Image

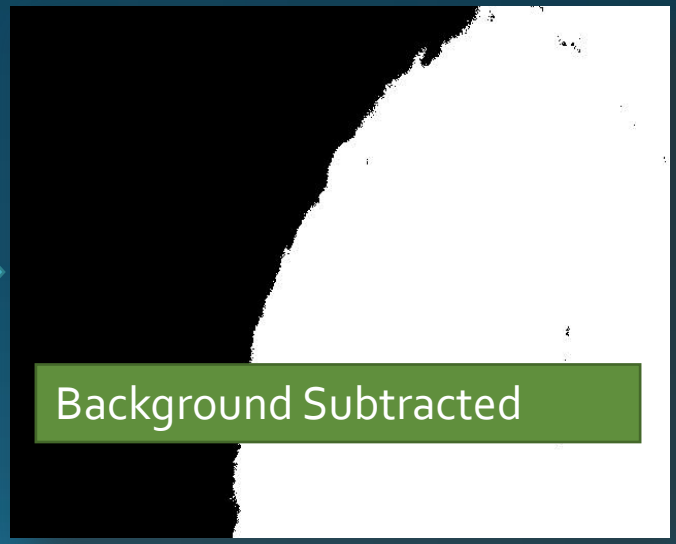


Original Image from Microscope:
W : 2560
H : 1920
Channel : RGB

Surface Crack Identification - Solution

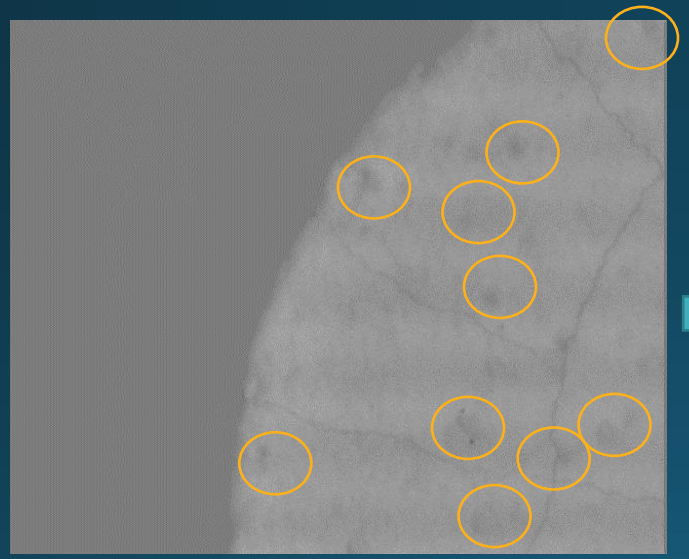
Original Image → Background Subtraction

Adjusting gold colour as an object (Region Of Interest). In this step, we Use HSV feature to distinguish gold with wafer. This step help us to reduce Spackle Noise



Surface Crack Identification - Solution

Original Image → Background Subtraction → Smoothing Process & Binarization



Gaussian Blur reduce spackle Noise, afterward we use binarization operation with thresholding.

Surface Crack Identification - Solution

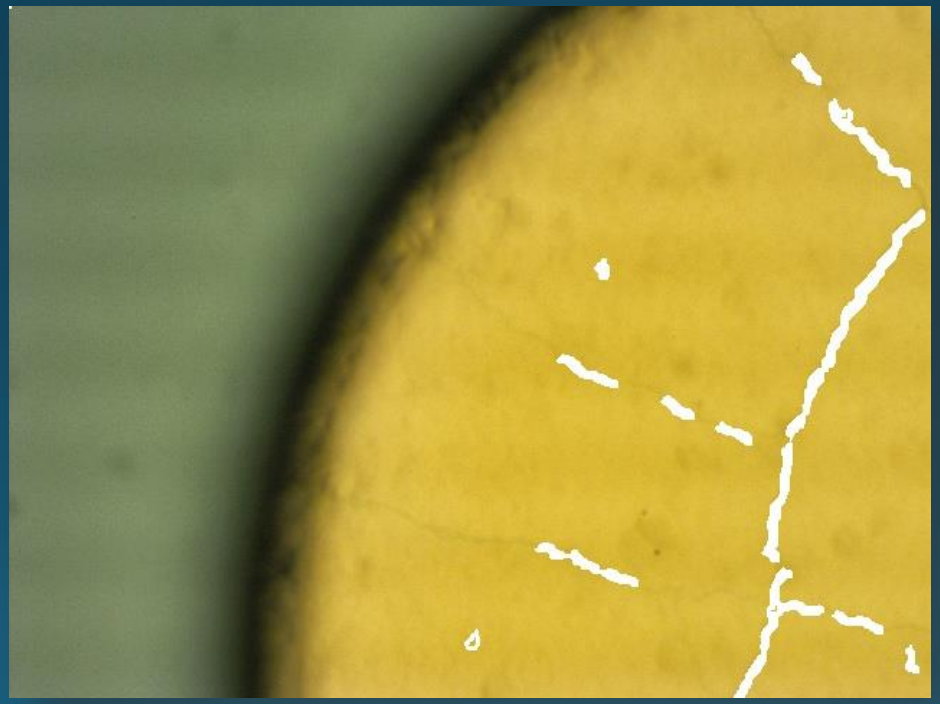
Original Image → Background Subtraction → Smoothing Process & Binarization → Canny Edge Detection

Surface Crack Identification - Solution

Original Image → Background Subtraction → Smoothing Process & Binarization → Canny Edge Detection → Contour Finding

Surface Crack Identification - Solution

Original Image → Background Subtraction → Smoothing Process & Binarization → Canny Edge Detection → Contour Finding → Output Image Original + Crack



Surface Crack Identification - Solution

Original Image → Background Subtraction → Smoothing Process & Binarization → Canny Edge Detection → Contour Finding → Output Image Original + Crack → Evaluation Process

Ground Truth

Comparing the manual groundtruth with crack detected

Crack Detected

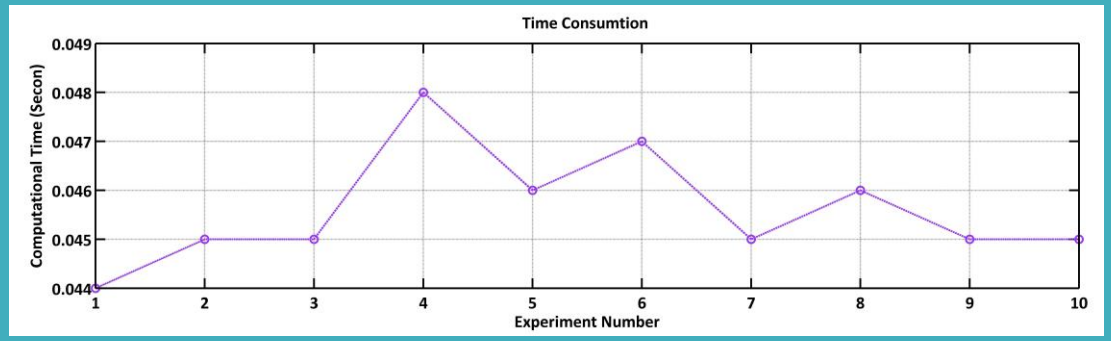
Surface Crack Identification - Solution

Original Image → Background Subtraction → Smoothing Process & Binarization → Canny Edge Detection → Contour Finding → Output Image Original + Crack → Evaluation Process

System Specification:

Processor	Intel Core i5 2,4 GHz (Quad Core)
Memory	4 GB
Operating System	Windows 7
IDE	CodeBlock
Programming Language	C++
Library	OpenCV 2.4
Running Operation	Real Time

Result:



Accuracy
51,23%

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Summary

- 3D scanner can be used to extract depth map of the chip surface. The 2nd order polynomial surface fitting is used to construct the reference surface for thickness determination. The thickness of the line connection (6.9 ± 0.4 µm) and pad edge (2.2 ± 0.6 µm) have been measured and computed by applying the algorithm of 3D surface measurement.
- Hough Transform can be used to detect all available connection lines. Spacing between two parallel lines can be calculated based on Pixel coordinates of the lines. The pixel distance is then converted to the real distance according the scaling factor of spatial resolution.
- Pre and post processing methods have been applied to reduce the image noises in surface cracking identification.

Issues

- Chip specifications (type, size, material, etc.) are required to validate measurement result of the proposed algorithm. Some chip samples are needed to be observed and studied in LIPI's lab.
- Need more picture of: chip, FPC, mounted chip of FPC, and the layout diagram as reference.
- Processing speed needs to be increased, e.g. the cracking identification algorithm => 0.05 s.
- The cracking identification algorithm will be improved to handle speckle noises on the image. Its appearance looks similar with the crack patterns.

Thank You