Current Activities I

• Busy with the preparation for Run2
  • New pixel detector (IBL) insertion. Yosuke Takubo
    \(\rightarrow\) See the talk of the CERN Fellow
  • End-cap Muon (TGC): Re-cabling after the repair works (of MDT/TGC),
  • Trigger improvements. Muon/ High Level trigger ...

• Some leading roles of KEK members in ATLAS
  • Trigger menu coodinator: Kunihiro Nagano
  • Muon trigger sigunature group convenor: Masato Aoki
  • K. Tokushuku will serve the deputy collaboration board chair from Jan 2015. (Then, the chair in 2016-2017 and the deputy in 2018)
ATLAS Detector: construction and commissioning

- Superconducting Central Solenoid (Japanese contribution: 100%)
- Time-to-digital conversion chips for muon drift tubes (100%)
- End-cap muon triggering system (TGC) (~30%)
- Silicon microstrip tracking system (SCT) (~20%)
- Lvl-2 muon trigger (Software)

2014/11/21
Current Activities II

- Still busy with physics analyses with the Run 1 data
  - H→ tau tau: Almost ready for the publish.

Other analyses KEK people are involved are
  - Top cross section
  - W + charm production...
  - etc.
LHC roadmap: schedule beyond LS1

LS2 starting in 2018 (July) => 18 months + 3 months BC
LS3 LHC: starting in 2023 => 30 months + 3 months BC
Injectors: in 2024 => 13 months + 3 months BC

(Extended) Year End Technical Stop: (E)YETS

Goal of 3’000 fb-1 by mid 2030ies
Detector Upgrade

- **Phase-1 upgrades** (for the shutdown in 2018-2019)
  - All ATLAS-Japan related MOUs were signed:
    (New small wheel, TDAQ(muon trigger), Liquid argon (mainly for U.Tokyo), Fast Tracker Trigger (mainly for Waseda U.)

- **R&D for Phase II**
  - Radiation hard, silicon detectors (Pixels and strips)
    - Beam test @ SLAC, DESY, CERN
  - Simulation for optimum layout of the inner tracker
    - New activity!
  - More sophisticated muon trigger
    - Inclusion of drift chamber (MDT) information in the LVL0 trigger.
Phase 1 Upgrade

- TDAQ: End-cap muon trigger Upgrade (electronics)
- New Small Wheel (NSW): Resistive foil for MicroMegas
- Lar-E: Liquid Argon trigger readout Data processing in FPGA
- FTK: Dedicated track trigger using Association memory

More focus on the trigger electronics
Inner Tracker

- Pixels/Strips: Sensors, Hybrids, Modules, DAQ, Software
International Review

- Japanese Participations on LHC upgrade (Accelerators + ALTAS) were reviewed on 21-22/Nov/2013 by following referees

Accelerator:
- Mike Lamont (CERN)
- Bruce Strauss (DOE)
- Lucio Rossi (CERN, HL-LHC head)
- Kaoru Yokoya (KEK)

Experiment:
- Jonathan Dorfan (OIST)
- Eckhard Elsen (DESY) – Chair person
- Fabiola Gianotti (CERN)
- Jordan Nash (IC London, CMS)
- Mihoko Nojiri (KEK, Theory)
- Andreas Schopper (CERN LHCb)

http://kds.kek.jp/conferenceDisplay.py?confld=13329

The Report was received in early 2014. The Japanese translation was also made. The reports were (informally) handed to the mext and the other relevant people.
Summary

• We are working hard (with fun!) in the difficult moment when we need to handle
  – Data analysis of Run1
  – Preparation of Run2
  – R&D of the upgrade
    at the same time.
Backup
ATLAS-Japan contribution plan

• Strategy:
  • Keep responsibilities on what we already committed but with some priorities.
    1. Muon:
      • The most responsible part is to generate the LVL1 muon trigger. --> Full responsibility on LVL1 Trigger electronics
      • R&D and component supply for chamber production. I.e. large-scale production at Japanese site is unlikely
      • Contribution to HLT, mainly on muon triggers but also on other objects such as taus depending on the physics interests
    2. Inner Tracker:
      • New contribution to pixel detectors. N-on-p planar type (with Hamamatsu)
      • Considering ‘fair share’, Japanese contributions on ~25% of overall pixel and ~10% of overall strip detectors are the targets. But it depends on how much our designs are adopted in the ATLAS collaboration.
      • Development of strip detectors with the alternative (back-up) option (super module configuration) for prototyping with new readout chips.

• Encourage new developments
  1. FTK: Main contribution on the input mezzanine boards: Waseda group, with (mostly) with their own JSPS fund.
  2. Liquid Argon: Readout signal processing (interests from the physics analysis (H-> gamma gamma, for example)

• Contribution to some common items, if necessary
  1. CPUs for trigger processing

Details will be discussed in the dedicated sessions. In this talk, one page summary for each project and summary of organization and cost are presented
The innermost station of the muon endcap
Located between endcap calo and toroid
Muon Trigger Phase-1/2 Upgrade

Precision Detector
\( \sigma < 100 \mu m \)
\( \phi \)-information

Level-0/1 Trigger
resolution of incidence angle
\(< 1 \) mrad
BCID, LVL0 latency

New Small Wheel

track fitting
track position \((R, \phi)\)
d\(\theta\) : deviation of incidence angle from infinite \(p_T\) muons
Coarse d\(\theta\) -cut

TGC1  MDT  TGC2  TGC3

\( \mu \)

BCID (40 MHz)
hit signal alignment
2 x 2/3 coin.
track position and deviation encoding

MDT

3/4 coin. track position and deviation
H-pT Board

BW-TGC + NSW
Track fitting and L0-seeds

BW-MDT + NSW : L0
Fine Track fitting
Endcap: crossing angle \(\beta\)
pT calculation

Other muon inner detectors

hit information \((R, \phi), d\theta\)
Inner Tracker

- Pixels/Strips: Sensors, Hybrids, Modules, DAQ...

Barrel Strips  Forward Strips

Barrel Pixel  Forward Pixel

LHC  HL-LHC  STRIPS

SCT barrel module

Hybrid

Microstrip sensor

PIXELS

- FE-I4 2-chip pixels
- FE-I4 1-chip pixels
- FE-I3 4-chip pixels
- FE-I3 1-chip pixels

LHC HL-LHC

2014/11/21
• Fast Tracker (FTK) : Online hardware tracking system for ATLAS upgrade.
• FTK reconstructs all tracks with PT>1 GeV/c for LVL1 accepted events and provides track information at the beginning of LVL2 trigger processing.
→ Allows to implement more efficient and complex algorithms at LVL2.

Japanese Participation:
- Waseda University
* responsible for Input mezzanine etc.

2014-2016:
- 2014: Production
- 2015: Installation & Commissioning
- 2016: Operation

R&D Global Test
Phase1 LAr readout scheme

- **Trigger upgrade** at Phase-I
  - Introduce new components with keeping Legacy electronics
- Introduce **Super-Cells** (10 times finer granularity)
  - \( \Delta \eta \times \Delta \phi = 0.1 \times 0.1 \rightarrow 4 \) layers with \( 0.025 \times 0.1 \) in middle layers.

New components:

- Summed signals are digitized at Front-End (FE).
- Converted to \( E_T \) by Digital signal processing at Back-End (BE) \( \rightarrow \) ATLAS-J contribution
- Send to Feature extractor (FEX) to make L1-Trigger.
- Fast data transfer is key
  - 25 Tbps (FE \( \rightarrow \) BE)
  - 41 Tbps (BE \( \rightarrow \) FEX)

Phase-1 components shown by the red dashed lines.