FPGA Use within the Detector Volume

Tullio Grassi (Univ. of Maryland)
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Disclaimer: difficult to cover all cases, this talk is a partial view.
What are FPGAs?

- A Field Programmable Gate Array (FPGA) is an integrated circuit which contains lots of logic blocks.
- Logic blocks can be connected together in a programmable way.
- Inputs and outputs are also programmable, in direction, strength and standard (CMOS, LVPECL, LVDS, etc).

Each logic block can be programmed to perform a boolean operation (in the LUT) and store a single bit in a Flip-Flop.

The data needed to set all programmable options of an FPGA is often called “Configuration data“.

The circuit realized with the Logic blocks and interconnects in an FPGA is called “User Logic“.
Why do we care about that?

In HEP detectors and accelerators, FPGAs have become extremely useful to build digital hardware tailored to specific requirements, including non-standard data processing and interfaces.

The advantages over traditional circuit boards with discrete components are that:
- FPGAs are denser, cheaper, faster.

The advantages over Application-Specific Integrated Circuits are that:
- part of the FPGA development is done by the vendor
- FPGAs often can be bought in small quantities
- FPGAs are programmable by the user

Being commercial circuits, they are not (necessarily) tolerant to ionizing radiations → this point is the focus of the talk.

Many detector and accelerator subsystems use or will use FPGAs in radiation areas (but not in extreme radiation areas like central trackers).
FPGAs in HEP: trends

- Initially FPGAs were simple boolean logic; later other blocks have been integrated: CPU, PLL, high-speed communication, etc.

- In the HEP Front-End Electronics installed around 2005, FPGAs were mostly used for control and readout logic with external high speed links.

- In recent FEE systems, FPGAs (will/could) take advantage of newer functions: high-speed links for increased data readout, PLLs for clock management related to synchronization with the accelerator clock, etc.

- Powering newer FPGAs becomes more compicate: need to provide higher currents at lower voltages.
FPGA types by market

- **Military and aerospace markets**: FPGAs designed explicitly for radiation hardness. HEP projects normally cannot (afford to) buy them. Not covered here.

- **Commercial markets**: all other applications. Accessible to HEP projects → covered in this talk.
### FPGA types by technology

**User Logic**: commonly built with CMOS fabrication processes (at least for commercial grade FPGAs).

**Configuration memory**: see table.

<table>
<thead>
<tr>
<th>Technology of the memory element</th>
<th>Main Vendors</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM (Static RAM)</td>
<td>Altera, Atmel, Lattice, Xilinx</td>
</tr>
<tr>
<td>Anti-fuse: one-time-programmable</td>
<td>MicroSemi, Aeroflex, Quicklogic</td>
</tr>
<tr>
<td>Flash memory cells</td>
<td>MicroSemi</td>
</tr>
</tbody>
</table>
Radiation effects on CMOS digital circuits (not limited to FPGAs)

1. **TID = Total Ionization Dose**. Measured in Grey = Gy (or in rad: 1 rad = 100 Gy)

2. **SEE = Single-Event Effects**:
   - **SEL** = Single-Event Latchup
   - **SEU** = Single-Event Upset
   - **SET** = Single-Event Transient
   - **SEFI** = Single-Event Functional Interrupt
   - **SEGR** = Single-Event Gate Rupture
   - **SEB** = Single-Event Burnout
Radiation effects on commercial FPGAs at LHC (LET $< 40\text{MeV}\cdot\text{cm}^2/\text{mg}$ [8])

**Memory cells**

<table>
<thead>
<tr>
<th></th>
<th>TID (degradation, then failure)</th>
<th>SEU on configuration</th>
<th>SET on configuration</th>
<th>SEL</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SRAM</strong></td>
<td>Virtex-6: $\sim 3.8$ kGy [1]. Arria GX: degrades from 1.7 kGy, still alive at 70 kGy [13]</td>
<td>Yes $\rightarrow$ need reconfiguration (partial or total)</td>
<td>Yes</td>
<td>No, on recent Xilinx families [12, 13]</td>
</tr>
<tr>
<td><strong>Anti-fuse</strong></td>
<td>Aeroflex Eclipse: 3 kGy [18]</td>
<td>No</td>
<td>Yes</td>
<td>No [12]</td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td>ProASIC3: fails at $\sim 300$ Gy. Igloo2: one sample failed at $\sim 1000$ Gy. SmartFusion2: one sample survived 380 Gy; reprogramming fails at $\sim 20$ Gy [10]</td>
<td>No</td>
<td>Yes</td>
<td>No on ProASIC3x [8]. Suspect non-destructive SELs on SmartFusion2 [10]</td>
</tr>
</tbody>
</table>

SEU and SET in the User Logic normally are mitigated by the user logic itself, not by the technology.
How to proceed?

FPGA are increasingly used in radiation areas. Their behavior under radiation has to be qualified, but this is difficult because:

1. Modern FPGAs have many different blocks (previously mentioned)
2. These blocks can have a wide range of programmable options
3. FPGAs keep evolving
4. Batch-to-batch variations
5. Each case of User Logic should be qualified (TMR, safe FSM, EDAC codes on RAM, etc).

We could benefit from:
• common qualification programs
• common procurement strategies

An initial attempt has been the “Workshop on FPGAs for High-Energy Physics” held at CERN on March 2014.

Results should be shared between our community, but preferably not with the general public because of: undesirable attention, vendors less likely to share internal data, etc. Initial attempt: https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/
Back-up slides
# FEE systems of CMS

<table>
<thead>
<tr>
<th>Sub-system</th>
<th>Approx radiation</th>
<th>FPGAs in 2008-2012</th>
<th>FPGAs after 2012 (radiation ~6x higher)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracker [2]</td>
<td>200 kGy. 10^{14} n/cm^{2}</td>
<td>No FPGAs (ASICs only)</td>
<td>No FPGAs (ASICs only)</td>
</tr>
<tr>
<td>ECAL [3,4]</td>
<td>25 kGy.</td>
<td>No FPGAs (ASICs only)</td>
<td>No FPGAs (ASICs only)</td>
</tr>
<tr>
<td>HCAL [5]</td>
<td>3 Gy. 10^{11} n/cm^{2}</td>
<td>Actel anti-fuse FPGA, for control only</td>
<td>igloo2 (flash) for control, data processing, TDC and transmission from 2016</td>
</tr>
<tr>
<td>Muon detectors</td>
<td>0.4 Gy. 5x10^{10} n/cm^{2}</td>
<td>SRAM FPGAs [6, 7].</td>
<td>igloo2 (flash) for control, data processing, TDC and transmission from 2014 [15]</td>
</tr>
<tr>
<td>CT-PPS</td>
<td>200 Gy, 2x10^{12} n/cm^{2} per 100/fb integrated lumin.</td>
<td>Did not exist</td>
<td>igloo2 (flash) for control, data processing, TDC and transmission from 2018 ?</td>
</tr>
</tbody>
</table>
# FEE systems of ATLAS

<table>
<thead>
<tr>
<th>Sub-system</th>
<th>Approx radiation</th>
<th>FPGAs in 2008-2023</th>
<th>FPGAs after 2023 (radiation ~6x higher)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracker</td>
<td>Xx kGy. $10^{14}$ n/cm²</td>
<td>No FPGAs (ASICs only)</td>
<td></td>
</tr>
<tr>
<td>Tile calorimeter [17]</td>
<td>15 Gy. $10^{11}$ n/cm²</td>
<td>640 Mb/s, severe errors in data transmission, loss of configurations</td>
<td>Demo project with xilinx for processing and 10 Gbps readout links</td>
</tr>
<tr>
<td>Muon detectors</td>
<td>xx Gy. $5\times10^{10}$ n/cm²</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


# FEE systems of LHCb

<table>
<thead>
<tr>
<th>Sub-system [9, 10]</th>
<th>Approx radiation in 2008-2018</th>
<th>FPGAs in 2008-2018</th>
<th>FPGAs after 2018 (radiation ~6x higher)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Tracker</td>
<td>60 kGy. $10^{14}$ n/cm²</td>
<td>No FPGAs in the hot zone (ASICs only)</td>
<td>Under study (probably not required)</td>
</tr>
<tr>
<td>RICH</td>
<td>240 Gy, $10^{12}$ n/cm²</td>
<td>Actel AX (antifuse) + Actel ProAsicPlus (flash) for controls</td>
<td>Xilinx Kintex7</td>
</tr>
<tr>
<td>Outer Tracker</td>
<td>70 Gy. $10^{12}$ n/cm²</td>
<td>No FPGAs in the hot zone (ASICs only)</td>
<td></td>
</tr>
<tr>
<td>SciFi Tracker</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Calorimeters</td>
<td>50 Gy. $10^{12}$ n/cm²</td>
<td>Actel AX (antifuse) for 80 MHz processing, Actel ProAsicPlus (flash) for 40MHz processing and control [9]</td>
<td>Under study (Microsemi Igloo2)</td>
</tr>
<tr>
<td>Muons [11]</td>
<td>80 Gy. $10^{12}$ n/cm²</td>
<td>Actel ProAsicPlus, for calibration system</td>
<td>Under study (Flash device)</td>
</tr>
</tbody>
</table>
## FEE systems of ALICE

<table>
<thead>
<tr>
<th>Sub-system</th>
<th>Approx radiation</th>
<th>FPGAs in 2008-2012</th>
<th>FPGAs after 2012 (radiation higher)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPC [20]</td>
<td>16 Gy. $10^{11} \text{n/cm}^2$ [21]</td>
<td>Virtex-II Pro (SRAM) for datapath, with its configuration verified and refreshed by an Actel ProASIC+ (flash)</td>
<td>Microsemi SmartFusion2 (flash). Links up to 5 Gbps. Problems observed. FPGA PLL loss of lock $\rightarrow$ use TTCrx instead [10]. ProASIC3 (flash) for radmon.</td>
</tr>
<tr>
<td>DDL (Detector Data Link, common to all subsystems)</td>
<td></td>
<td>Actel ProASIC+ (flash). 200 MB/s links</td>
<td></td>
</tr>
<tr>
<td>All others</td>
<td>$\sim0$ at the FPGA location</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SEU prevention in FPGAs

SEU on Flip-flops $\rightarrow$ TMR, fault-tolerant FSM.
There are two commercial synthesisers that can do automatic TMR of flip-flops, in order to prevent SEU:

1) Synplify:  
It is in use in Cern by a few groups, so far so good (circuits not yet deployed).

2) Precision RT:  
http://www.mentor.com/products/fpga/synthesis/precision-rad-tolerant/ (ITAR limited)

SEU on memory $\rightarrow$ encoding
SET prevention in FPGAs

Prevention of SETs:
• TMR that includes combinatorial logic
• filtering with guard-gate

Precision Rad-Tolerant can do TMR of combinatorial logic. Apparently this feature is not supported for Actel FPGA (as of today).

Commercially available tools are evolving rapidly wrt SEU and SET → keep watching.

In the Microelectronics Section of CERN, some designers have been using a custom script that generates automatically TMR on registers and combinatorial logic. The script supports only Verilog 1995 designs. The script is available to people registered on the CERN FPGARadTol web page.
SEL prevention

A SEL is a latch-up caused by a particle crossing the circuit. It can happen on the internal nodes (while normal latchups occur mostly on the I/Os due to ESD). Most modern FPGAs are immune from SEL. But other commercial components can be affected by SEL.

→ external SEL protection circuit.
SEL-protection circuits: a generic scheme

When a SEL-sensitive circuit develop a SEL, it draws more current. An external circuit can detected this situation and cycle the power.

Problem: also the protection circuit can be affected by radiation. But being a simpler circuit, it is possible to design it so that it is very unlikely that it develops a problem.
SEFI

SEFI = Single Event Functional Interrupt

The definition can vary according to the authors, but it normally indicates an SEE which affects the entire device, for instance:

• power-on reset
• global reset,
• global tristate
• problems in the circuit that program the rest of the FPGA

For an FPGA, it is difficult or impossible to mitigate SEFI within the FPGA design. SEFI could be mitigated at the system level.
References

[8] Private communication, Federico Faccio
[16] https://indico.cern.ch/event/300532/contribution/7/material/slides/1.pdf
[17] https://indico.cern.ch/event/299180/session/5/contribution/12/material/slides/0.pdf
[20] https://cds.cern.ch/record/921042/